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M73-SERIES
MODEL 7/32 C
MAINTENANCE MANUAL

INTERDATA®

Subsidiary of PERKIN-ELMER
Oceanport, New Jersey 07757, U.S.A.

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QUICK REFERENCE INDEX

To aid in quickly locating a particular section, the index marks on the edge of this page are aligned with similar marks at the beginning of each section.

GENERAL DESCRIPTION

[redacted]

3. DOCUMENTATION

This section describes the style and conventions used with INTERDATA documentation.

3.1 Number Notation

The most common form of number notation used in INTERDATA documentation is hexadecimal notation. In this system, groups of four binary digits are represented by a single hexadecimal digit. Table 2 lists the hexadecimal characters employed.

TABLE 2. HEXADECIMAL NOTATION DATA

Binary	Decimal	Hexadecimal	Binary	Decimal	Hexadecimal	Binary	Decimal	Hexadecimal
0000	0	0	0110	6	6	1100	12	C
0001	1	1	0111	7	7	1101	13	D
0010	2	2	1000	8	8	1110	14	E
0011	3	3	1001	9	9	1111	15	F
0100	4	4	1010	10	A			
0101	5	5	1011	11	B			

To differentitate between decimal and hexadecimal numbers, hexadecimal numbers are proceded by the letter "X", and the number is enclosed in single quotation marks. Examples of hexadecimal numbers are: X'1234', X'2EC6', X'A340', X'EEFA', and X'10B9'.

3.2 Part Numbering System

INTERDATA parts, drawings, and publications employ a common numbering system. The part number and drawing numbers for drawings which describe the part are related. The publication number is also often related to the part number of the device or program described. Figure 2 shows the format used for INTERDATA part numbers. The fields are described in the following paragraphs.

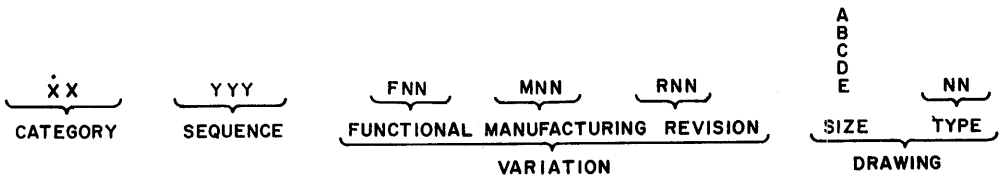


Figure 2. Part Number Format

3.2.1 Category Field. The two-digit Category number indicates the broad class or category to which a part belongs. Typical examples of category number assignments are:

01 - Basic Hardware Systems
02 - Basic Hardware Expansions
03 - Basic Software Systems
04 - Software Packages
05 - Micro-programs
06 - Test Programs
07 - Subroutines of General Utility
10 - Spare Parts Packages
12 - Card File Assemblies
13 - Panels
17 - Wire and Cables
19 - Integrated Circuits
20 - Transistors
27 - Peripheral Equipment
29 - Manuals
34 - Power Supplies
35 - Assembled Printed Circuit Boards
36 - Electro-Mechanical Devices

3.2.2 Sequence Field. The Sequence number identifies a particular item within the category. Sequence numbers are assigned serially, and have no other significance.

NOTE

The Sequence Field, like all other part number fields, may be lengthened as required. The field lengths shown on Figure 2 are minimum lengths (insignificant zeros must be added to maintain these minimums).

3.2.3 Functional Variation Field. The optional Functional Variation Field consists of the letter "F" followed by two digits. The F field is used to distinguish between parts which are not necessarily electrically or mechanically equivalent, but which are described by the same set of drawings. For examples, a power supply may be strapped internally to operate on either 110 VAC or 220 VAC. Except for this strap, all power supplies of this type are identical. The strapping option is easily described by a note on the assembly and test specification drawings. Therefore, this is a functional variation.

3.2.4 Manufacturing Variation Field. The optional Manufacturing Variation Field consists of the letter "M" followed by two digits.

The M Field is used to distinguish between parts which are electrically and mechanically equivalent (interchangeable), but which vary in method of manufacture. For example, if leads are welded instead of soldered on an assembly, the M Field changes.

An important exception to the meaning of the M Field exists for categories related to software. In software, the M Field number, when used, indicates the form in which a particular program is presented. For example, define a program as a set of machine instructions. These same identical instructions may be presented on punched cards, paper tape, or magnetic tape; and for any of these they could be in symbolic form or in relative or absolute binary form. Thus, there are many ways to present the same identical program.

The format for the M field and its meaning for software is:

Mxy

where x identifies the media selection (i.e., paper tape, mag tape, cassette, etc.) and
y identifies object or source and the format.

Meaning of x		Meaning of y
Conceptual Paper tape	0 1	1 Object program standard format 32 bit Processor
Cassette Magnetic tape (800 BPI)	2 3	4 Memory Image 6 Object program standard format 16 bit Processor
Cards Disc (2.5MB)	4 5	7 Object non-standard format 8 Object established task
Disc (10MB) Magnetic tape (1600 BPI)	6	9 Source program

The above numbers refer to the physical program placed on an approved media for INTERDATA Software.

A paper tape object program in standard format and for a 16 bit Processor has an M16 identifier.

A magnetic tape object program in standard format and for a 32 bit Processor has an M31 identifier.

In addition to the foregoing, there are three unique M numbers which have special meaning:

00	Conceptual Object
91	32 Bit Object Listing
92	Programming Specifications
95	Program Description
96	16 Bit Object Listing
98	Operating Procedures
99	Documentation and Manuals

3.2.5 Revision Field. The optional Revision Field consists of the letter "R" followed by two digits. The R Field is used to indicate minor electrical or mechanical changes to a part which do not change the part's original character. The R field changes often reflect improvements. A part with a revision level HIGHER than the one specified can be used; however, a part with a revision level LOWER than specified should not be used.

NOTE

A part number must contain a Category number and a Sequence number. All other fields are optional.

3.2.6 Drawing Field. The optional Drawing Field consists of a letter from "A" to "E" followed by two digits. The letter indicates the size of the original drawing. The sizes for each letter are:

A - $8\frac{1}{2}$" x 11"
B - 11" x 17"
C - 17" x 22"
D - 22" x 34"
E - 34" x 44"

The two digits indicate the drawing type as follows:

01 - Parts List	15 - Program Description
02 - Machine Details	16 - Operating Instructions
03 - Assembly Details	17 - Program Design Specification
05 - Art Details	18 - Flow Charts
06 - Wire Run List	19 - Product Specification
08 - Schematic	20 - Installation Specification
09 - Test Specification	21 - Maintenance Specification
10 - Purchase Specification	22 - Programming Specification
11 - Bill of Material	23 - Replaceable Parts List
12 - Information	24 - Application Information
13 - Program Listing	25 - Functional Specifications
14 - Abstracts	

3.2.7 Examples. The following list provides some examples of the part numbering system. The numbers were arbitrarily selected, and in most cases are fictitious.

35-060	The 60th printed circuit board assigned a part number under this system.
35-060M01	A printed circuit board electrically and mechanically interchangeable with the 35-060, but differing in method of manufacture.
35-060F01	A printed circuit board not electrically and mechanically interchangeable with the 35-060, but described by the same set of drawings.
35-060R01	A revised 35-060 printed circuit board which probably supercedes the 35-060.
35-060B01	The 11 by 17 inch parts list for a 35-060.

35-060B08 The 11 by 17 inch schematic for a 35-060.

06-72A13 An $8\frac{1}{2}$ by 11 inch listing of the 06-072 program.

06-072A12 An $8\frac{1}{2}$ by 11 inch information drawing on the 06-072 program. Probably a part of the program.

29-060 The 60th manual assigned a number under this system. Note that this number is not referenced in any way to the part number of equipment described in the manual.

3.3 Drawing System

This section describes the drawings provided with INTERDATA equipment. Drawings provided with peripheral devices and other purchased items may vary from the system described in this section.

A digital system may be divided into a collection of functionally independent circuits such as Memory, Processor, and I/O Device Controllers. These circuits may or may not be saleable units in their own right, but in the electrical sense they are essentially self contained and capable of performing their function with minimum dependence on other functional circuits in the system. Hence a functional circuit is treated as a building block. Each schematic contains a variety of information including type and location of discreet Integrated Circuits (IC's), pin connections, all interconnections within the schematic, connector pin numbers and connections to other schematics. Further, the schematics are drawn to reflect, in an orderly fashion, all logical operations performed by the circuits. Generally, symbols used on schematics conform to MIL-STD-806B.

Registers are named according to the following rules:

1. The register mnemonic name has a maximum of three letters, excluding "I, O, Q, and Z".
2. Each bit in the register is numbered, usually starting at 00 on the left, or most significant positions, and continuing to N-1 on the right, where N is the number of bits in the register.
3. The 00 bit is the Most Significant Bit and the N-1 is the Least Significant Bit.

The IC's mounted directly on the logic board are represented on the schematic drawings by logic symbols. Each symbol contains the reference designation, device part number (category and sequence), and symbol mnemonic designation. Refer to Figure 3.

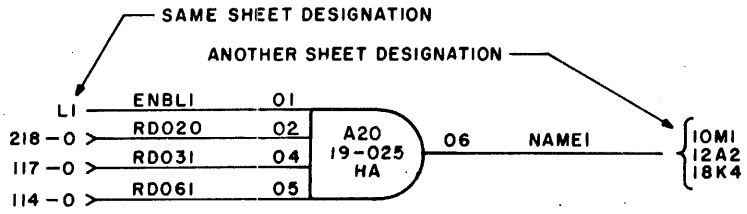


Figure 3. Example of a High Speed AND Gate

The designations, numbers, and references shown in Figure 3 are:

A20 This shows the components location on the logic board. Figure 4 illustrates the method generally used to determine component location on a logic board. With the logic board oriented so that the header connectors (Conn 0 and Conn 1) are on the right, the components are numbered from left to right starting in the upper left corner. That is, the first IC in the upper left corner is 01 and the first capacitor is C1.

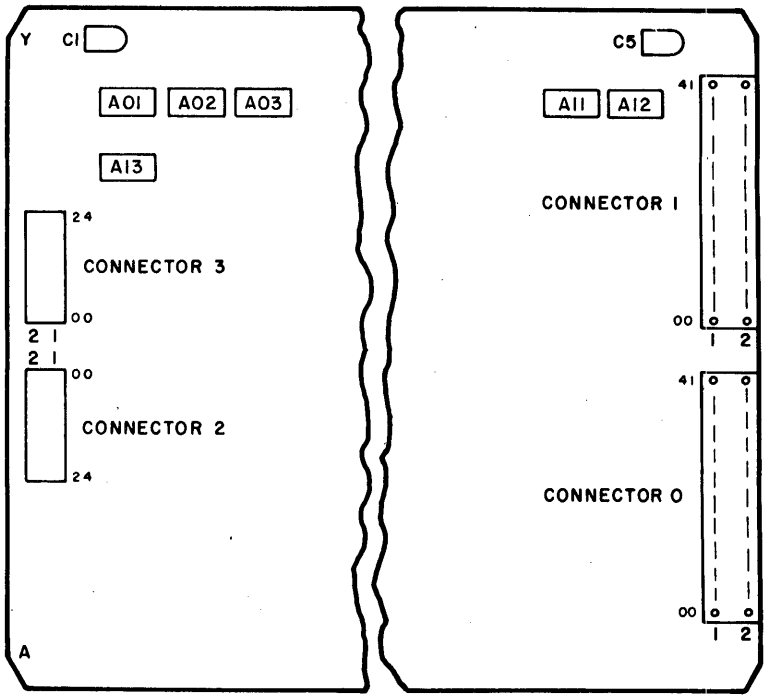


Figure 4. Example of a Logic Board Layout

19-025 The number 19 is the category number of ICs, and the 025 is the sequence number of the component.

HA Designates that this component is a high speed AND gate. Some other common designators used are:

P	- Power Gate
SB	- Schottky High Speed Power Gate
SG	- Schottky Gate
SGO	- Schottky High Speed Gate, Open Collector
SO	- Schottky High Speed Gate, Open Collector
B	- Buffer
SB	- Schottky High Speed Buffer
LOR	- Low Power Schottky OR
LN	- Low Power Schottky NOR

L1 - This input lead is from area L1 on the same schematic sheet.
10M1, 1242, 18K4 - Designate outputs to another logic schematic sheet.
218-0, 117-0, 114-0 - Designate inputs from Connector 0.
Pin numbers (01, 02, 04, 05 and 06) correspond directly to the actual IC pin numbers.

Figure 4 also shows the locations of the header connectors (Conn 0 and Conn 1) and the cable connectors (Conn 2 and Conn 3). All logic boards always contain Header Connectors 0 and 1, however, any combination (either, both, or none) of cable connectors (Conn 2 and Conn 3) may be provided.

Whenever possible, the immediate output from a flip-flop (1 or 0 side) has a mnemonic name preceded by an F. A flip-flop whose name is PSEL (Processor selected) has an output mnemonic, on the 0 side, FPSEL0 (see Figure 5). This provides the digital technician with an indication, when observing a mnemonic at the terminal end of a net, that the signal is the output of a flip-flop rather than a decoded function.

Clocked devices, flip-flops, and counters in particular, are drawn in a manner which indicates information concerning their inputs. An input which has a circle adjacent to the pin designation implies a low active signal is required to perform the specified operation. In addition, an inverted V at the clock input shows that the device changes state on an edge. Thus, if no circle is present the chip is positive edge triggered. Refer to Figure 5 for examples.

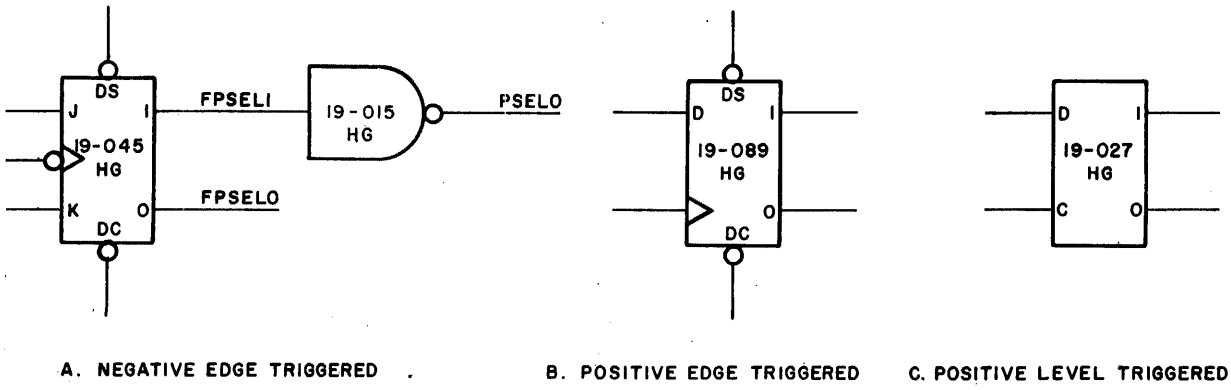


Figure 5. Examples of Clocked Devices

Figure 6 shows the pin numbering scheme for the header and cable connectors. Header connectors always have 2 rows of pins and 42 positions. Cable connectors always have 2 rows of pins but may vary in the number of positions. The number of positions may only vary in increments of five positions (10 contacts). For instance, if 24 positions are desired, five blocks of five positions each (25 positions) must be used.

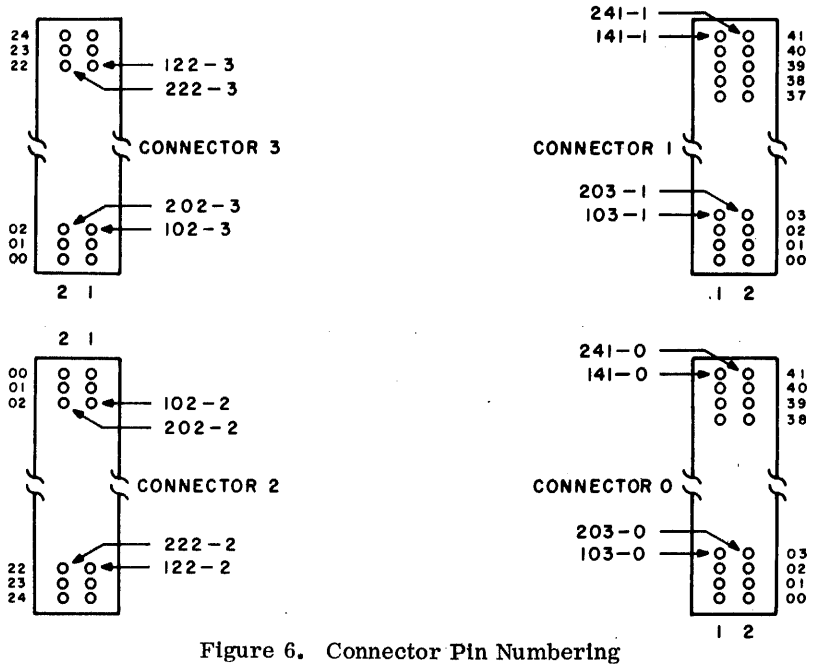


Figure 6. Connector Pin Numbering

A net is defined as an electrical connection between two or more points in a circuit. Ordinarily, a net has an originating end (usually a collector where the signal is generated) and one or more terminating ends. Often it is convenient to assign descriptive mnemonic names to nets as a way of identifying them on schematics. Whether a net is named or not is sometimes arbitrary. However, a net is always assigned a name if:

1. The net is contained on one drawing sheet but is not shown as a complete solid line on that sheet.
2. Part of the net appears on more than one sheet.
3. Part of the net connects with a different schematic.
4. Part of the net leaves a logic board.

If a net is named, the following rules are observed.

1. All mnemonic names are a maximum of six characters.

2. All decimal digits and upper case letters except the letters "I, O, Q, and Z" are permitted.

3. No other characters are permitted.

4. Where possible, mnemonics are descriptive. However, it should be recognized that descriptive names are not always possible and a danger of misinterpreting a mnemonic exists.

5. Mnemonic names are not repeated within a schematic.

6. Every mnemonic is suffixed by a state indicator. This indicator consists of the digit "1" for the logically true state, or the digit "0" for the logically false state. For example, the set side of a flip-flop has the "1" state indicator, while the reset side has the "0" state indicator. The state indicator for a function changes each time that function is inverted. Thus, the same indicator permits assigning the same mnemonic to functions that are identical except for an inversion. Logic 0=0.5VDC or less, Logic 1 = 2.4VDC or more.

7. When a logical function is inverted, an inversion indicator is added after the state indicator. This allows for functionally equivalent, but electrically different nets to have the same mnemonic name. For example, assume a signal NAME1 which may be inverted to produce NAME0. If NAME0 is then inverted, NAME1A is produced. NAME1 and NAME1A are functionally equivalent, but physically different nets.

There are times when a net fans-out to many sheets of a schematic. It is also possible for a net to fan-out to sheets on different schematics. In such situations, the net is assigned a mnemonic name. The net is also "zoned" from sheet to sheet to allow for properly identifying the originating and terminating ends of the net. The originating end of a net is defined as the collector at which a signal is generated. All other points to which the net connects are called terminating ends. When a lead leaves a sheet at the originating end, it is zoned to each and every sheet on which the net reappears, by indicating first the page number, followed by the schematic number that contains the page. For example, assume that the gate shown on Figure 3 is on a schematic, Sheet 20. The output NAME0, appears on Sheets 10, 12 and 18 of the schematic. Note that the schematic number is implied. When a net enters a sheet from another sheet, it is labeled with the same mnemonic name, and is zoned back to the originating end of the net only. Thus, on Figure 3, the ENABL1 may have many other terminations in addition to the one shown. Generally, when a net leaves the sheet where it originates, it is zoned to every other sheet where the net terminates, while the terminating end is zoned only to the originating sheet. Note that on schematics, signals are coordinated between sheets only when the sheets are related to the same board. When a signal leaves a board, the Back Panel Map must be used.

When a lead leaves a logic board, it usually does so through a logic board back panel connector pin. These connector pins must be shown on the schematic even if the complete net is shown on one drawing sheet. Only the connector pin number need be indicated under the pin symbol, since the connector number itself is implied by the logic board location number in the logic symbol or in the footnote. Thus, on Figure 3, RD061 enters the logic board on Pin 114 of Header Connector 0.

Figure 7 is a typical schematic sheet with call-outs illustrating many of the conventions described in this section.

The schematic drawings for the basic Digital System and some of the more common expansions are commonly included in the rear of the appropriate Digital System Maintenance Manual. Schematic drawings for other expansions are included with the expansion or with the publications that describe the expansion.

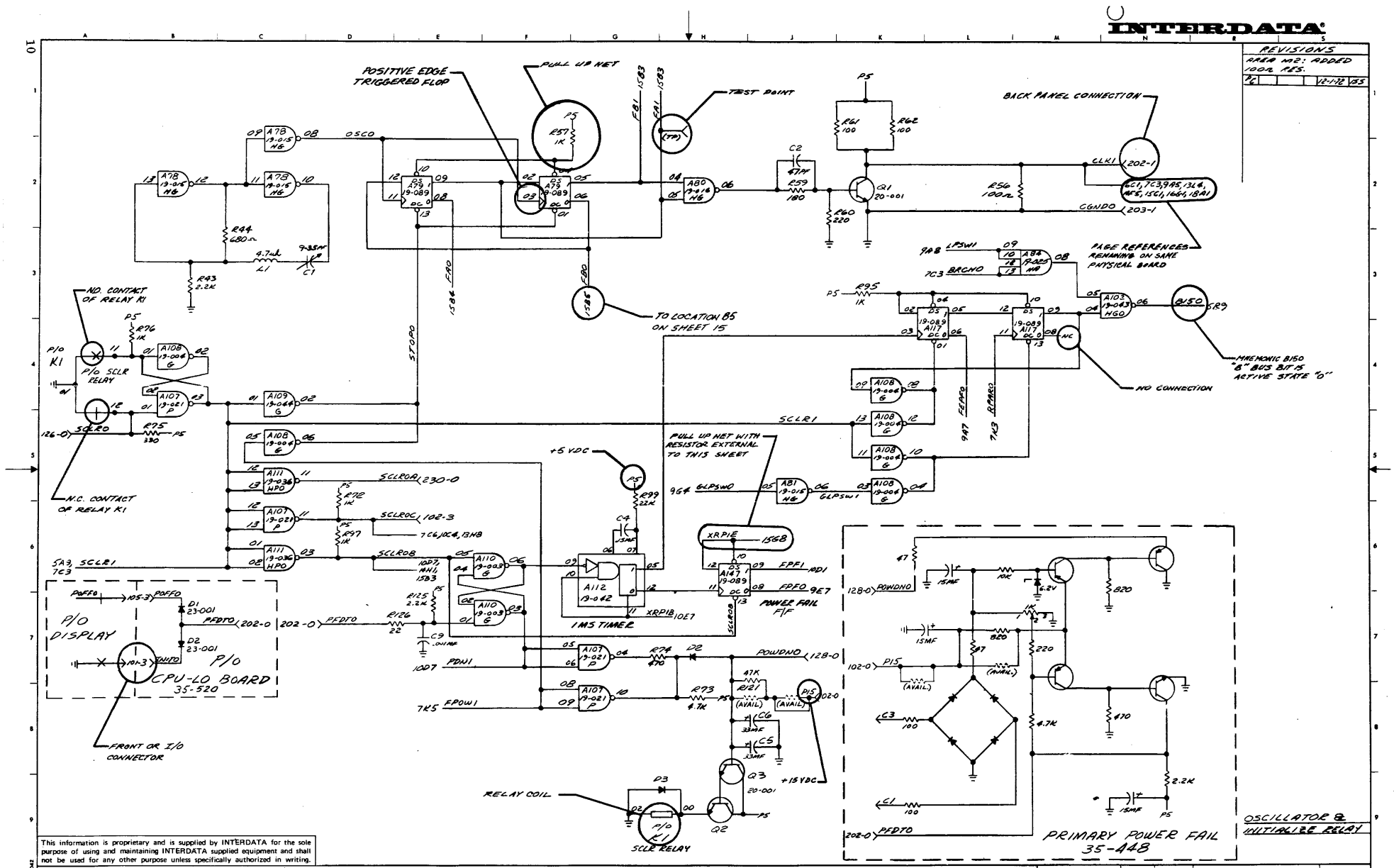


Figure 7. Functional Schematic Format Drawing

APPENDIX 1

PART NUMBER CROSS REFERENCE TABLE

INTERDATA Part Number	Type	JEDIC Number
19-001	Dual 4 Input NAND DTL	15861
19-002	Triple 3 Input NAND DTL	15863
19-003	Quad 2 Input NAND DTL	15849N
19-004	Hex 1 Input NAND DTL	15837N
19-005	Dual Power Gate DOC	8633N
19-006	Dual Buffer DTL	1582N
19-007	Flip-Flop DTL	15848N
19-008	Gate Expander Dual 4 Input DTL	15833N
19-009	8 Bit Stack DTL	903059 (Fairchild)
19-010	Differential Comparator LIN	72710L
19-012	Dual 4 Input Buffer TTL	74H40H
19-013	Quad 2 Input NAND DTL	15846
19-014	Dual J-K Flip-Flop DTL	158097N
19-015	Hex Inverter 1 Input	74110411
19-016	Quad 2 Input TTL	741100N
19-017	Triple 3 Input TTL	74H10N
19-018	Dual 4 Input TTL	74H20N
19-019	Single 8 Input TTL	MC3015 (Motorola)
19-020	Operational Amplifier LIN	MC1709C (Motorola)
19-021	Quad 2 Input Power DOC	15858N
19-022	Dual J–K Flip-Flop TTL	MC3061P (Motorola)
19-023	Selected Dual Buffer 19-006 with 20-30 nanosecond delay DTL	15832N
19-024	Triple 3 Input AND TTL	74H11N
19-025	Dual 4 Input AND TTL	74H21N
19-026	2-2-2-3 Input AND-OR TTL	74H52
19-027	4 Bit Latch TTL	7475N
19-028	4 Bit Adder TTL	7483N
19-029	Quad Exclusive – OR TTL	7486N
19-030	4 Bit Shift Register TTL	7495N
19-031	One Shot TTL	7412N
19-032	1 out of 10 Decoder TOC	74145N 5445 7445
19-033	Sense Amplifier LIN	7524N
19-034	Retriggerable One Shot TTL	74122N
19-035	4 Bit Counter TTL	74193N
19-036	Quad 2 Input Open Collector TTL	7438N
19-037	High Performance Operational Amp	7748393 (Fairchild)
19-038	Dual 4 line to 1 line Mux TTL	74153
19-039	4 Bit ALU TTL	74181
19-040	Look Ahead Carry TTL	74182
19-041	4 x 4 Register Stack TTL	74170
19-042	Dual Retriggerable One Shot TTL	74123N
19-043	Quad 2 Input Open Collector TTL	74H01N
19-044	Hexadecimal Inverter Open Collector TTL	74H05N
19-045	Dual J-K Flip-Flop TTL	74H106
19-046	Quad RS-232C Line Driver	MC1488L (Motorola)
19-047	Quad RS-232C Line Receiver	MC1489AL (Motorola)
19-048	8 Bit Shifter	74198N
19-050	8 Input NAND TTL	74H30
19-051	1024 Bit PROM TTL	74187 (Fairchild)
19-055	Quad 2 Input NAND STTL	74S00
19-056	Quad 2 Input NAND Open Collector STTL	74S03
19-057	Hex 1 Input Inverter STTL	74S04
19-058	Triple 3 Input NAND STTL	74S10
19-059	Triple 3 Input AND STTL	74S11
19-060	Dual 4 Input NAND STTL	74S20
19-061	Dual 4 Input Buffer STTL	74S40
19-062	2-2-3-4- Input AND-OR Inverter STTL	74S64
19-063	Dual D Edge Triggered Flip-Flop STTL	74874

INTERDATA Part Number	Type	JEDIC Number
19-064	Dual J-K Flip-Flop STTL	74S112
19-065	Quad 2:1 Mux Non-Inverting STTL	74S157
19-066	Quad 2:1 Mux Inverting STTL	74S158
19-067	4 Bit ALU STTL	74S181
19-068	Carry Look Ahead STTL	74S182
19-069	8 line to 1 line Mux STTL	74151
19-070	4 Bit Synchronous Counter TTL	74161
19-071	Quad D Edge Triggered Flip-Flop	74175
19-072	4 Bit Left/Right Shift Register TTL	74194
19-073	Dual 4:1 Mux Tri-State TTL	8214 (National)
19-074	8 Bit Priority Encoder TTL	9318 (Fairchild)
19-075	16 x 4 Register Stack TTL	3101A (Intel)
19-076	1024 Bit Memory MOS	TM54062
19-077	256 Bit Memory TTL	6531 (Monolithic Memories)
19-078	Dual 4 Input NAND-OC	74S22
19-080	High-Speed PROM	82S29 (Signetics)
19-081	Univ. Asynchronous Receiver/Transmitters	TR1042A (Western Digital)
19-082	2-3-4 Input AND-OR Invert Open Collector STTL	74S65
19-083	9 Bit Parity Generator/Checker STTL	82S62 (Signetics)
19-085	Monolithic Timing Circuit	MC1555 (Motorola) NE55V (Signetics)
19-086	741 C DIP Operational Amplifier	U6A7741393 (Fairchild)
19-087	747 DIP Operational Amplifier	U7A774 (Fairchild)
19-088	737 C DIP Operational Amplifier	U6A773393 (Fairchild)
19-089	Dual D Edge Triggered Flip-Flop	741174
19-090	High Speed (710) Differential Comparator DIP	U6A771093 (Fairchild)
19-091	Retriggerable Single One Shot	9600 (Fairchild)
19-092	Negative Voltage Regulator	MU1463R (Motorola)
19-093	Positive Voltage Regulator	MC1469R (Motorola)
19-094	Voltage Regulator	U6A7723393 (Fairchild) MC1723CL (Motorola)
19-095	Linear Positive Voltage Regulator	U9H7805393 (Fairchild)
19-096	First In – First Out Serial Memory 64 Word 4 Bit	3341 (Fairchild)
19-097	Amplifier	L110002H (National)
19-098	Quad 2:1 Multiplexer Non-Inverting	74157
19-099	Dual Sense Amplifier	75234N
19-100	Driver	75452N
19-101	4-2 Input Buffer	7437N
19-102	6-1 Input Buffer OC	7407N
19-103	1 out of 10 Decoder	7442N
19-104	Current Switch	75325N
19-105	Dual Differential Driver	9614 (Fairchild)
19-106	Dual Differential Receiver	9615 (Fairchild)
19-107	Sense Amplifier	SN7520N
19-108	Quad 2 Input NAND	SN7400N
19-109	Hex Inverter Open Collector	SN7406N
19-110	Inverter	SN7404N
19-111	Dual 4 Input NAND	SN7440N
19-112	Optically Coupled Isolator	TIL-111 4N25
19-113	360 Dual Transmitter	TI 75123
19-114	360 Triple Receiver	TI 75124
19-115	Quad 2 Input AND	741108
19-116	Dual 4:2 Multiplexer STTL	74S153
19-117	4 Bit Magnitude Comparator STTL	74858
19-118	Quad Bus Transceiver TTL	26S12A
19-119	Expandable AND-OR Invert TTL	74455
19-120	Dual Timer	NE556 (Signetics)
19-121	Matched Pair 19-085 (P. S. Timing)	SEE 19-085
19-122	ROM	
19-123	Dual Voltage Controlled Oscillator	TI 74S124
19-123	V.C. Dual Oscilliscope	74S124 (T.I.)
19-124	4-21 NAND Buf STTL	74S37 (T.I.)
19-125	D.C. 4-21 NAND Buf STTL	74S38 (T.I.)
19-126	2-2W-2IN AIO STTL	74S51 (T.I.)

INTERDATA Part Number	Type	JEDIC Number
19-127	4-Exclusive OR STTL	74S86 (T.I.)
19-128	12I NAND, 3-State STTL	74S124 (T.I.)
19-129	3/8 Decoder STTL	74S128 (T.I.)
19-130	2-41 NAND 50 Dri STTL	74S140 (T.I.)
19-131	4D FF STTL	74S175 (T.I.)
19-132	4 2/1 Mux 3-State STTL	74S258 (T.I.)
19-133	4 Bit Bi Adder TTL	74283 (T.I.)
19-134	Hexadecimal Buffer /Inv TTL	8T98
19-135	4 Bit Bi Count STTL	93516
19-136	1/10 Decoder HS & HV	74145
19-137	Dual Periph Pos or Dr	75453B
19-140	8 Bit Latch	8334 (Fairchild)
19-141	Multi-Port Reg	9338 (Fairchild)
19-143	4K x 1 N Mos RAM	TMS4050 SP-3801
19-144	4-Hystersic Rec	DM8836 BT-3801
19-145	Voltage Regulator +15	79M15
19-145F01	Voltage Regulator +12	78M12
19-146	Volt Reg -15	LM340T-15/78 Mis Avc
19-146F01	Voltage Regulator -12	79M12
19-146F02	Voltage Regulator -5	79M5
19-147F01	8 Channel Analog Mux	Harris HA1818-5
19-147F02	7 Channel Analog Mux	Analog Devices A07503JN
19-148	Voltage Follower	Nat. LM310D, AMD LM 310D
19-149	High Speed Op Amp	Analog Devices A0509J Harris HA 2525
19-150	2 Channel Analog Sw	Siliconix DG1928A, Intersel IH5048 CTW
19-151	LL Inst Amp	AMD AD521
19-152	LL Inst Amp	Harris 3660
19-153	4-21 NAND LPTTL	9S/74LS00
19-154	Inverter LPTTL	9S/74LS04
19-155	3-31 NAND LPTTL	9S/54LS10
19-156	2-41 NAND LPTTL	9S/74LS20
19-157	8I NAND LPTTL	9S/74LS30
19-158	4-2I NOR LPTTL	9S/74LS02
19-159	4-2I OR LPTTL	9S/74LS32
19-160	4-2I AND LPTTL	74LS08
19-161	3-3I AND LPTTL	74LS11
19-162	2-4I AND LPTTL	74LS21
19-163	4-2I Hyst NAND LPTTL	74LS132
19-164	4-2I Buff NAND LPTTL	74LS37
19-165	2-D FF LPTTL	74LS74
19-166	2-JK FF LPTTL	74LS112
19-167	4-D FF LPTTL	74LS175
19-168	3/8 Decoder LPTTG	74LS138
19-169	Hex Inverter OC LPTTG	74LS05
19-170	4-2 I NAND O.C. LPTTG	74LS03
19-172	4-2I Exclusive OR LPTTG	74LS86
19-173	8/1 AIO Mux LPTTG	74LS151
19-174	4-2/1 AO 3-State Mux LPTTG	74LS257
19-175	4-2/1 AO Mux LPTTG	74LS157
19-176	4-2/1 3-State Mux LPTTG	74LS258
19-177	2-4/1AO Mux LPTTG	74LS153
19-178	2-2 Wide AIO LPTTG	74LS51
19-179	4/3/3/2 AIO LPTTG	74LS64
19-180	Syn 4 Bit Count LPTTG	74LS161
19-181	Asyn 4 Bit Up/Down Count LPTTG	74LS193
19-182	Bi-direct 4 Bit S.R.	74LS194
19-183	2-Line Driver	75110
19-184	4 Bit Micro Controller	Am2901 (AMD)
19-185	4K-Bit PROM	82S115 (Signetics)
19-186	4K-Bit ROM	82S114 (Signetics)

INTERDATA Part Number	Type	JEDIC Number
19-187	Quad 2:1 Mux with Storage LPTTL	742S298
20-001	Transistor NPN High Speed Switch	2N3646
20-002	Transistor PNP 500 MA	MPS6534 (Motorola)
20-003	Transistor	2N3902
20-004	Transistor NPN	2N5189
20-006	Transistor NPN 15 Amps 100W TO3 case	2N3055 (RCA)
20-007	Transistor NPN 3 Amps	TIP31A
20-008	Transistor PNP 3 Amps	TIP32A
20-009	Transistor Triac 2 Amps 100V	A03001 (Electronic Control Corp.)
20-010	Transistor NPN 500 MA Code Driver	2N5845
20-011	Transistor Photo	2N5777
20-012	Transistor PNP High Current Switch	2N2907
20-013	Transistor NPN	2N3303
20-014	Transistor NPN	2N4238
20-015	Transistor PNP	2N4235
20-016	Transistor PNP	2N3740
20-017	Transistor NPN	2N3766
20-018	Transistor, Power Silicon NPN	2N3054
20-020	Transistor Switching 1 Amp T05 can	2N3725
20-021	Transistor NPN Silicon	MPS3646 (Motorola)
20-022	Transistor NPN	1N1711
20-023	Transistor PNP	2N2905A
20-024	Transistor Switch	2N3776
20-025	PNP HI SPEED Switch	2N3467
20-026	Transistor Module, Quad	MPQ3725
20-027	Transistor	2N2369
20-029	Transistor	
21-025F01	1K ohm-15 to Common DIP	898-1-1K ohm (Beckman)
21-025F02	470 ohm-15 to Common DIP	898-1-470 ohm (Beckman)
21-025F03	330 ohm-15 to Common DIP	898-1-330 ohm (Beckman)
23-001	Diode High Speed-High Current	1N914
23-002	Diode 5.1 V Zener	1M5. 1ZS5 (Motorola
23-003	Diode 10V Zener	1M10ZS5 (Motorola)
23-004	Diode 6.1 V Zener	1M6.1ZS5 (Motorola)
23-007	Diode Mot Bridge	MDA962-2 (Motorola)
23-008	Diode Int. Rectifier	40HF-5R
23-009	Diode	1N4735
23-010	Diode Int. Rectifier	S1Y1P
23-011	Diode Rectifier	2N681
23-012	Diode Thermistor	KA31J1 (Fenwall)
23-013	Diode 9.4V	1N2163
23-014	Diode	1N3880
23-015	Diode	1N3889
23-016	Diode Bridge Rectifier	VS448 (Varo)
23-017	Diode	1N2070
23-018	Diode 18 V Zener	1N4746A
23-019	Diode	1N3615
23-020	Diode 8.2V Zener	1N756A
23-021	Diode 9.1 V Zener	1N757A
23-022	Diode 3.3V Zener	1N746A
23-023	Diode Bridge Rectifier	KDH2506 (General Instruments)
23-024	Diode, Power Fast Rec. 30 Amps	1N3909
23-025	Diode, Power Fast Rec. 3 Amps	A115A (General Electric)
23-026	Triac 600V 30 Amps	2N6162
23-027	Diac 32V	1N5761
23-028	Power SCR Thyristor	2N4441
23-029	Diode	1N4607
23-030	Diode	1N4156
23-031	Diode 6.6 V Zener	1N4736
23-032	Diode 8.8 V. Zener	1N4739
23-033	16 Diode Array	45190 (Litton)
30-018	100 nanoseconds Delay Line 10 taps	30-018 (Princeton Advanced Eng.)
30-019	50 nanoseconds Delay Line 10 Taps	30-018 (Princeton Advanced Eng.)

PROCESSOR

[redacted]

01-097A20
February 1976

M73-SERIES
MODEL 7/32 C
INSTALLATION SPECIFICATION

1. INTRODUCTION

The INTERDATA Model 7/32 C Digital System features a highly modular structure which permits configurations to suit the user's exact needs. It provides the means for convenient expansion as the user's requirements grow. This document describes the Processor, System Expansion Chassis, and Power Supply Mounting. Filler and Display Panel mounting, and the interconnecting cables. Printed circuit boards are discussed with respect to cabling and location only. Circuit descriptions of these boards are provided in the appropriate maintenance or instruction manuals. Note that the following discussion assumes that the equipment is mounted in standard INTERDATA cabinets. In addition, this specification covers the installation of the Turnkey Console.

2. MECHANICAL COMPONENTS

This section is intended to familiarize the reader with the mechanical components that are discussed here (i.e., Cabinet Uprights, Chassis Support Rails, Filler Panels). Figures 1 through 4 provide the dimensions and mounting configurations for the Rack, Chassis Support Rails, and Filler/Display Panels. Note in Figure 4, that while $3\frac{1}{4}$", 7", and $10\frac{1}{2}$" Filler Panels and the Display Panel mount the same way (via retaining brackets), the smaller 1 3/4" Filler Panel mounts with spring clips.

3. PROCESSOR AND EXPANSION CHASSIS MOUNTING

Two Expansion Chassis (10 inch and 15 inch) are available for expanding the Model 7/32 C Digital System. The (15 inch) Expansion Chassis has the same over-all dimensions as the Processor Chassis. See Section 8 on Configuration.

The Expansion or Processor Chassis slides into the rack on the two Chassis support rails (see Figures 2 and 3) from the front of the rack.

CAUTION

NO CHASSIS SHOULD BE MOUNTED IN CANTILEVER FASHION. CHASSIS SUPPORT RAILS MUST BE USED. IF A RACK CABINET OTHER THAN AN INTERDATA CABINET IS USED, CONSULT RACK MANUFACTURER FOR PROPER SUPPORT RAILS.

The chassis support rails are fastened to the mounting uprights at the front and rear of the rack. Slots are provided in the rails to allow vertical adjustment. The Expansion or Processor Chassis are screwed in place at the mounting uprights in front of the rack. All Expansion Chassis mount below the Processor Chassis. Expansion Chassis cabling is discussed later in this document. Figure 13 shows Expansion Chassis location with respect to the filler panel and power supply.

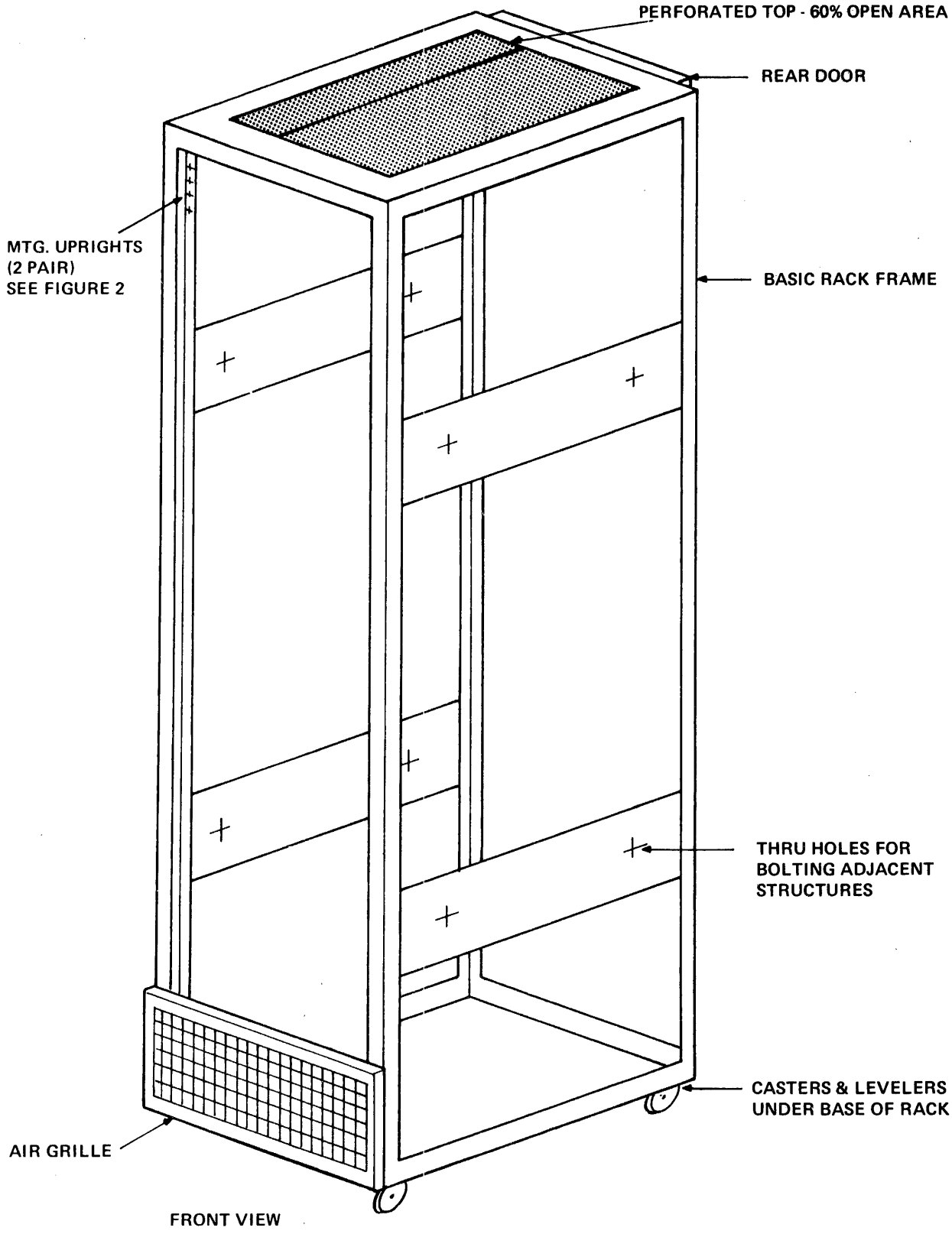


Figure 1. Basic Cabinet

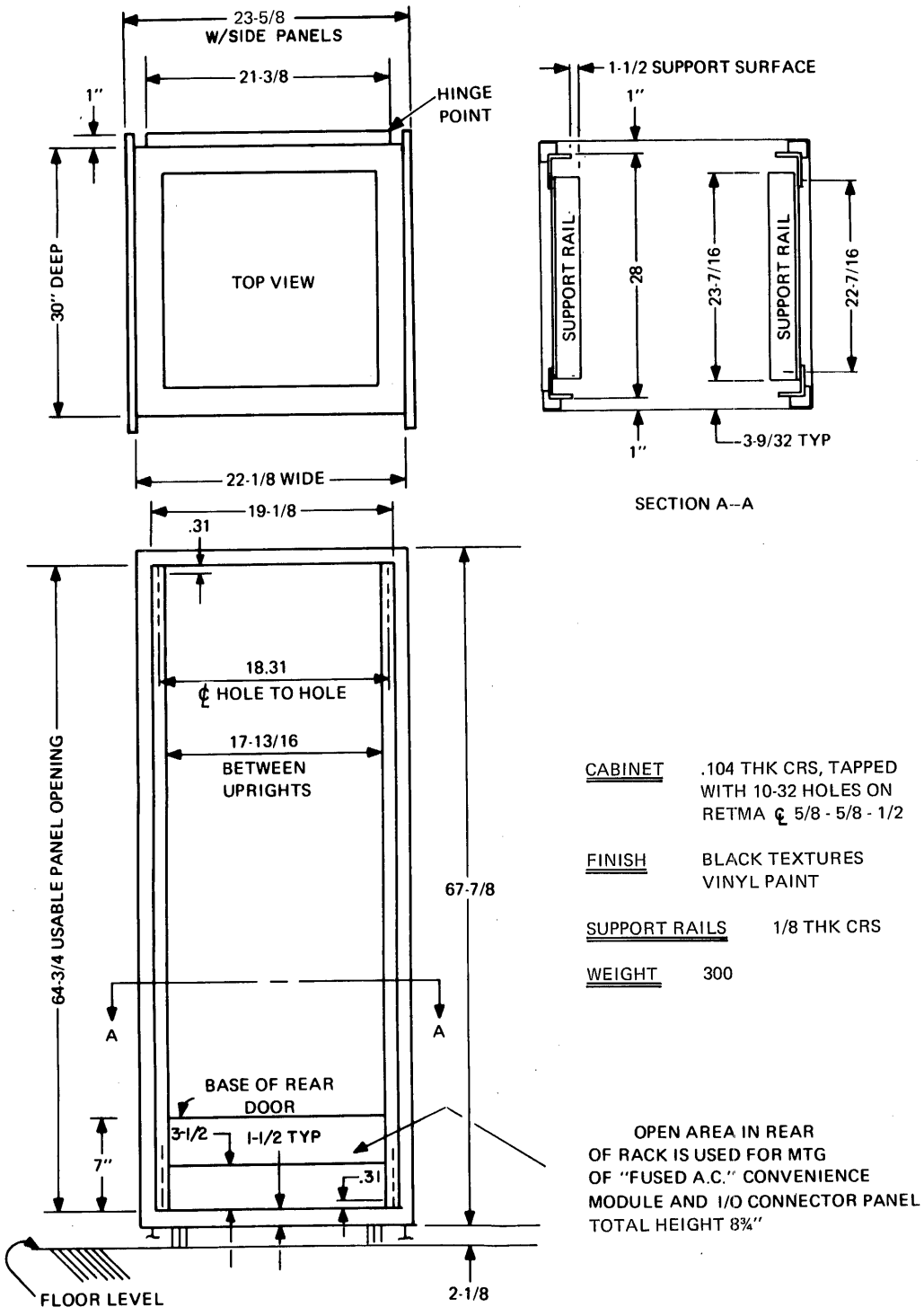


Figure 2. Basic Cabinet Physical Dimensions

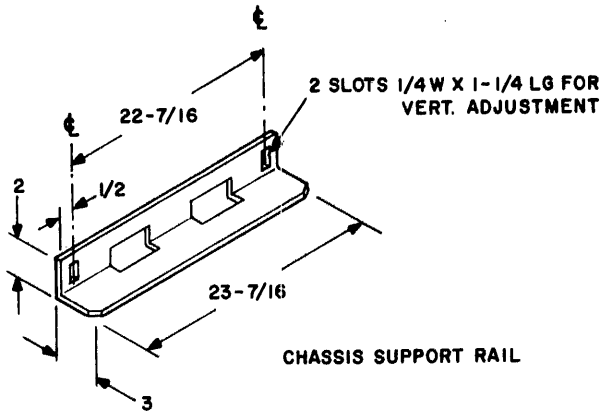


Figure 3. Chassis Support Rail

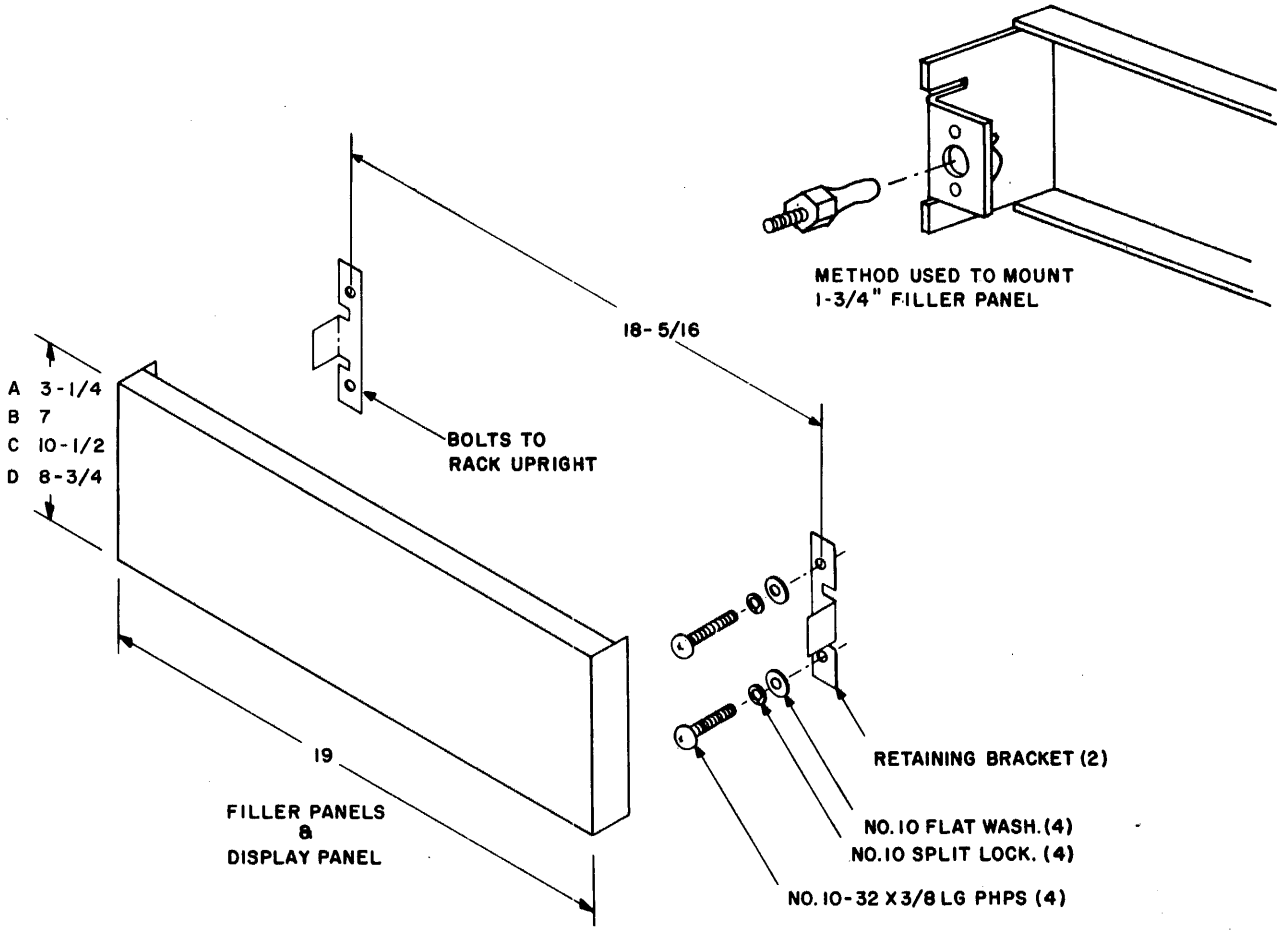


Figure 4. Typical Mounting Configuration for Display and Filler Panels

3.1 15 Inch Expansion Chassis

The 15 inch Expansion Chassis contains eight universal expansion slots which can accept combinations of memory modules, single board peripheral controllers, system modules, Selector Channel, or user designed interfaces. Included with this chassis are the cooling fans and interconnecting cables. The chassis may be ordered with or without a power supply.

3.1.1 7 and 10 Inch Boards in a 15 Inch Chassis. A 10 inch I/O Controller (provided it does not use Connector 1) may be inserted in a 15 inch chassis via the 02-234 I/O Adapter Kit (see Figure 5). One or two 7 inch boards (half boards) may be inserted into a 15" chassis via the 16-398 Half Board Adapter Kit (see Figure 6). The Half Board Adapter Kit may hold two active 7" boards or one active and one blank 7" board, depending on requirements. No wiring takes place between the boards and the adapters. The adapters are designed such that the connectors on the boards plug directly into the Expansion Chassis.

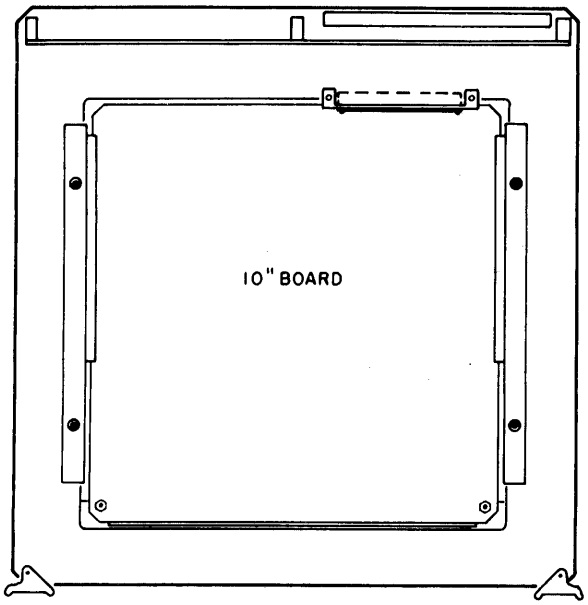


Figure 5. 02-234 I/O Adapter (Top View)

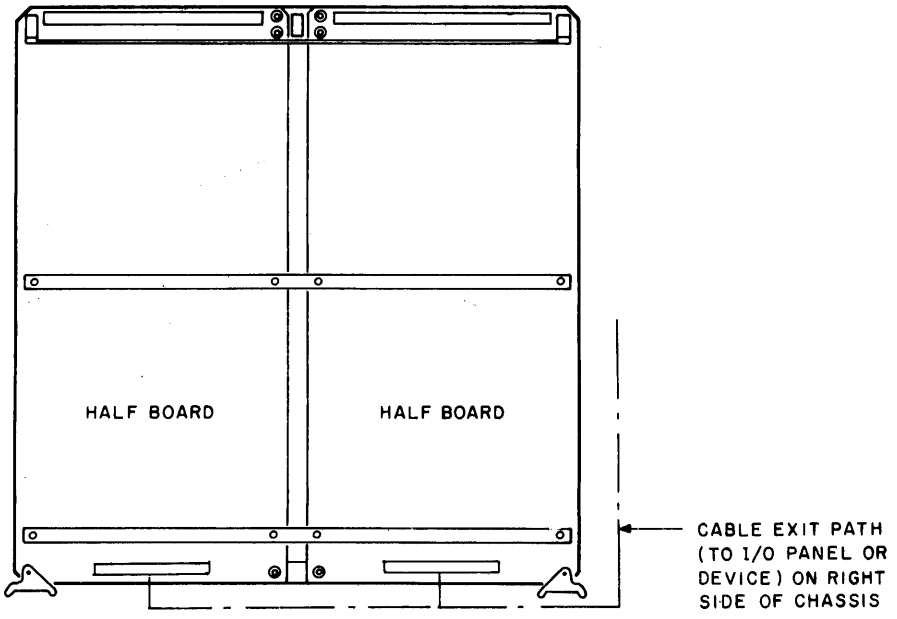


Figure 6. 16-398 Half Board Adapter

No wiring takes place between the boards and the adapters. The adapters are designed such that the connectors on the board plug directly into the Expansion Chassis.

The Expansion Chassis for 10 inch controllers contains six 10 inch I/O expansion slots which can accept any combination of up to six 10 inch wire-wrap or copper peripheral controllers, systems, modules, or user designed interfaces. Included with the Chassis are the cooling fans and system interconnecting cables. The Power Supply is separate.

4. POWER SUPPLY MOUNTING

The Power Supply mounts in the rear of the cabinet, behind the Processor or Expansion Chassis. It is attached to the right mounting upright (looking from the rear). One of three Power Supplies may be supplied with the Model 7/32 C System.

These Power Supplies attach to the mounting upright via four 10-32 x $\frac{1}{2}$lg PHPS screws (refer to Figure 7).

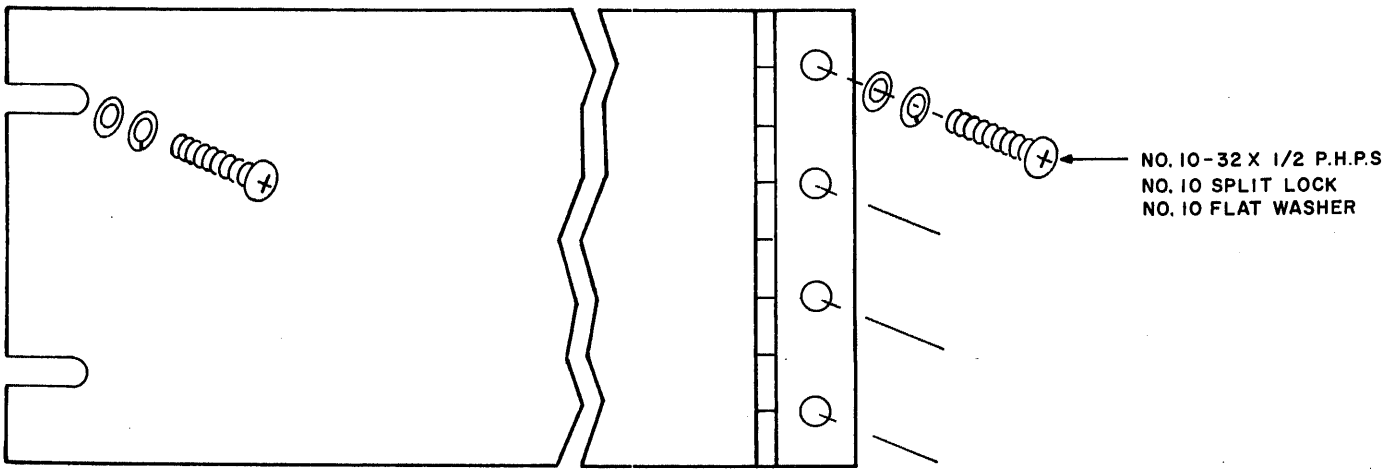


Figure 7. 34-017 and 34-020 Power Supply Mounting

WARNING

BEFORE HINGING OUT THE POWER SUPPLIES, THE RACK LEVELLING FEET SHOULD BE LOWERED. AFTER THE LEVELLERS ARE IN CONTACT WITH THE FLOOR SURFACE, UP TO THREE POWER SUPPLIES MAY BE HINGED OUT AT ONE TIME. IF THE LEVELLERS ARE NOT DOWN, AND THREE POWER SUPPLIES ARE HINGED OUT, THE RACK MAY TIP DUE TO THE WEIGHT OF THE POWER SUPPLIES.

When any Power Supply is in the installed operating position, it is secured to the left rear upright by two 10-32 screws. The power supply cable connects to terminal lugs at the right rear (looking from the rear) of its respective Processor or Expansion Chassis via Faston lugs and a connector for AC fan power (refer to Figure 8).

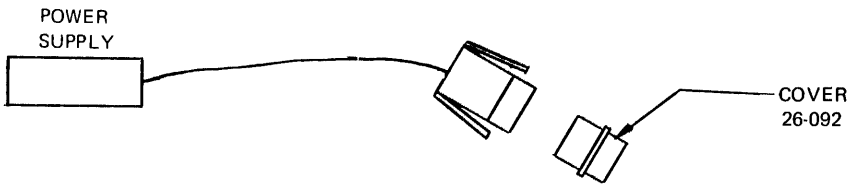


Figure 8. Fan Connector Caps

There is adequate slack provided in the cable to allow the Power Supply to hinge out freely. In order to prevent the cable from being pinched between the Power Supply and Chassis Support Rails, a service loop is required. A maximum of five Power Supplies may be mounted in one rack.

WARNING

ALL AC FAN CONNECTORS ON POWER SUPPLIES WHICH ARE NOT CONNECTED TO MATING RECEPTACLES MUST REMAIN COVERED OR SHORTING MAY OCCUR. SEE FIGURE 8.

The 115/230 volt fan switch on the chassis must be matched with the 115 volt or 230 volt strapping on the Power Supply (refer to Figure 9).

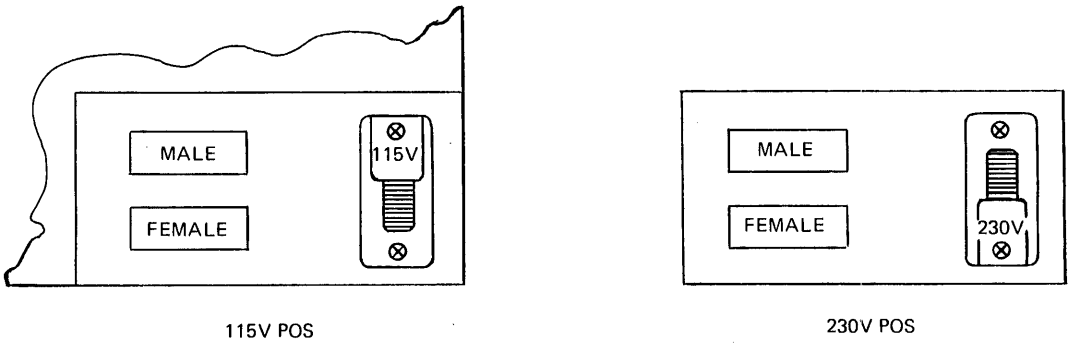


Figure 9. Fan Power Switch Match

Exhaust fan plates are equipped with a switch to provide either 115 volt or 230 volt AC operation as shown in Figure 10.

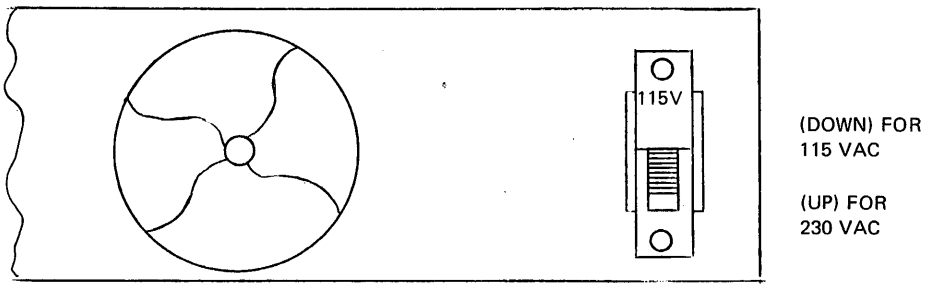


Figure 10. Exhaust Fan Switch Setting

A third supply (34-023) designed to meet VDE specifications required by some International installations, is also available. The mounting procedure for this power supply is different than the procedure for the standard supplies. Refer to Power Supply Maintenance Manual, Publication Number 29-452, for installation information.

5. DISPLAY PANEL INSTALLATION

The optional Model 7/32 C Hexadecimal Display Panel is electrically tied to the Processor via one connector and seven Faston lugs. The connector is installed on Connector 3 of the 35-624 CPU-A board and the seven terminal lugs mate into a terminal strip on the left side of the Processor Chassis. The terminal lugs are identified at the Faston connector and are mated to their corresponding terminal pin (C1, C2, etc.) on the chassis. See Figure 11.

The Hexadecimal Display Panel is physically mounted to the brackets provided on the Processor Chassis. The ten inch Filler Panel is mounted directly below the Hexadecimal Display Panel on this same chassis. Refer to Figure 12.

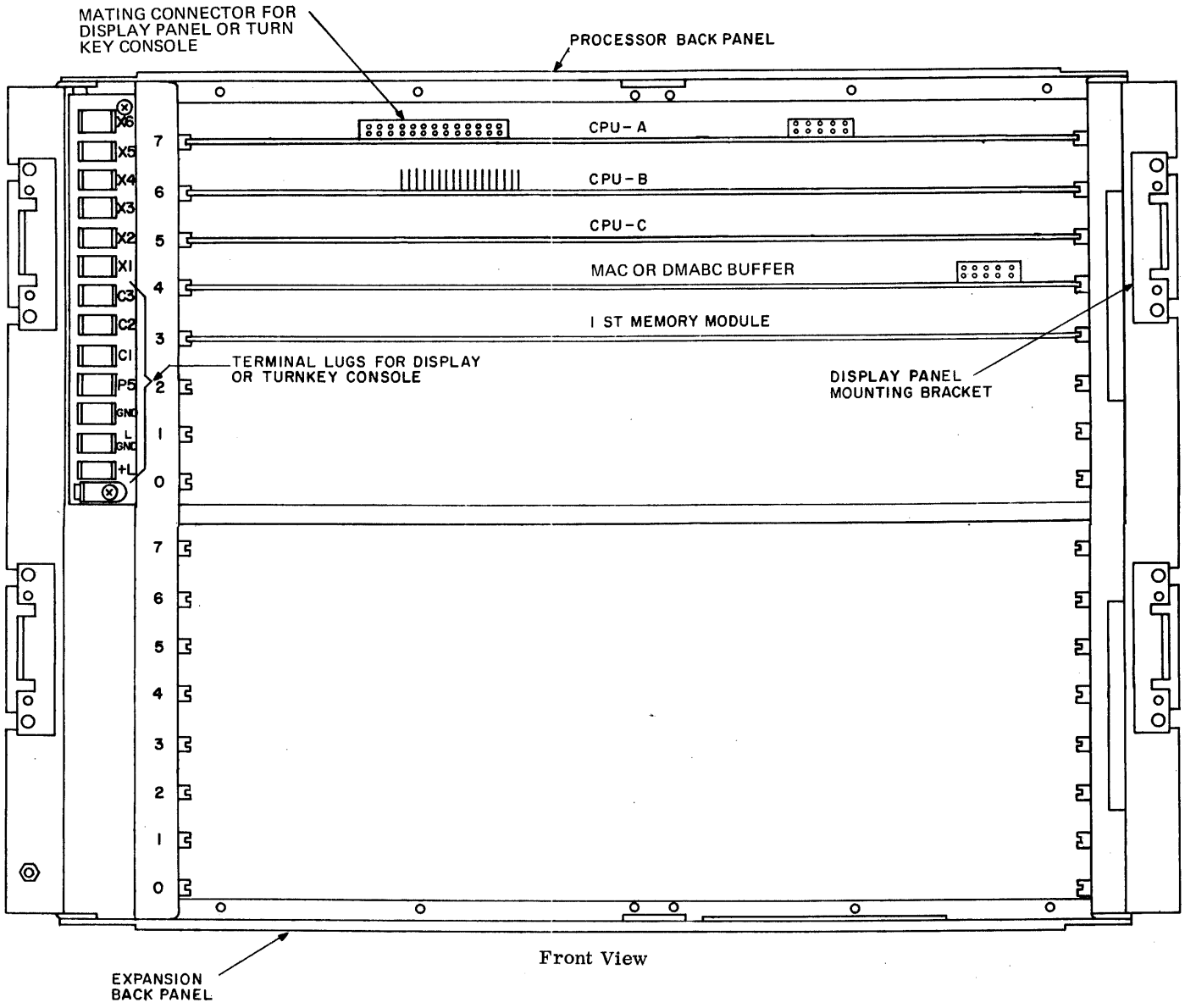


Figure 11. Front View of the 7/32 C Twin Chassis

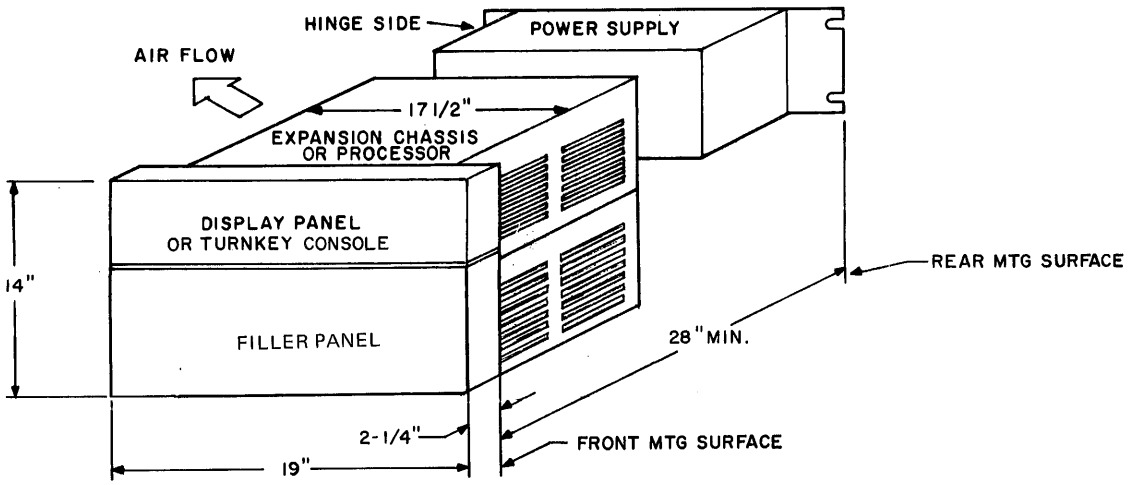


Figure 12. Processor Chassis Location

6. TURNKEY CONSOLE PANEL INSTALLATION

The Turnkey Console is connected to the Processor in the same manner as the Hexadecimal Display Panel discussed previously. Only two Faston connectors are provided with this assembly, but their installation is the same.

The panel on which the switches are installed may be mounted in the same manner as the display panel.

The Hexadecimal Display Panel option, and the Turnkey Console option may not be installed together on the same Processor.

7. MEMORY INSTALLATION AND EXPANSION

The following rules must be adhered to when configuring memory in the Model 7/32 C Processor. Refer to Figure 13.

1. Parity and non-parity memory modules may not be mixed in a memory system.
2. If 1 microsecond and 750 nanosecond memories are both present in the configured memory system, the entire memory system will operate at a 1 microsecond per memory cycle.
3. Memory must be installed into adjacent descending slots in a given memory bank.
4. The first memory module must be installed in Slot 3 of the Processor back panel.

7.1 32KB Memory Module

Refer to the appropriate 32KB Memory Module Maintenance Manual for address strapping information of the 35-347 32KB Memory Module. The 32KB Memory Module may be used anywhere in a 256KB Memory Module block. The 32KB Memory Module may be used in a fast or slow memory system.

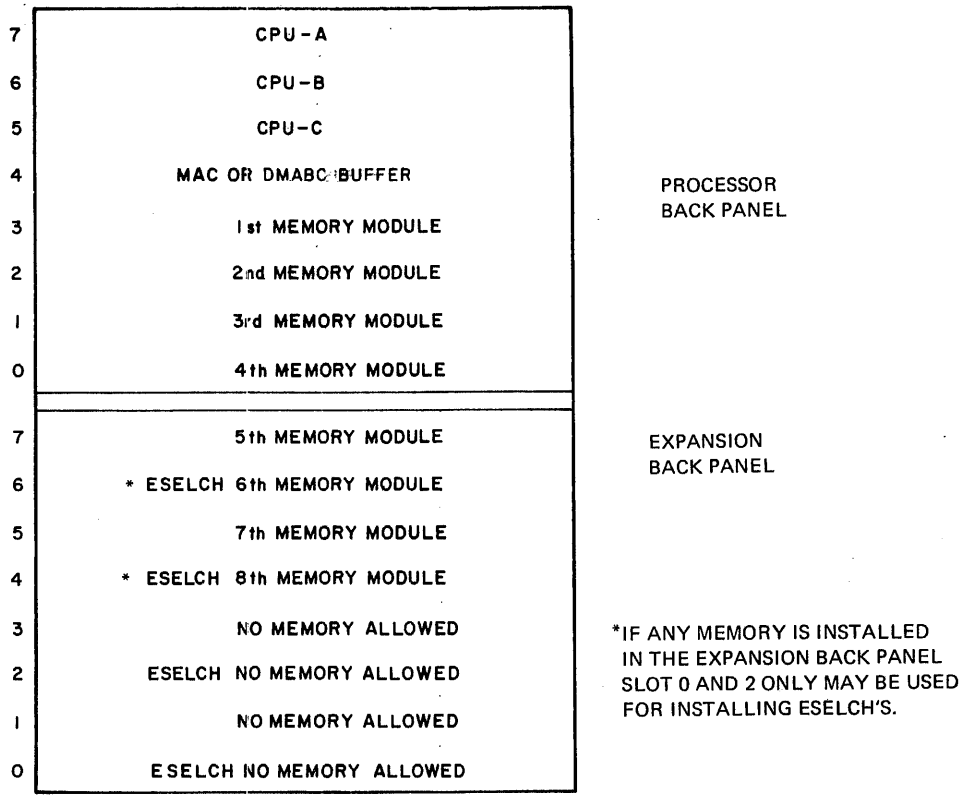


Figure 13. Model 7/32 C Memory Configuration

8. INSTALLATION OF PPF/AUTO-RESTART, MAC, DMABC BUFFER, ESELCH, AND MEMORY PARITY OPTION LOGIC CARD

8.1 Primary Power Fail/Auto-Restart Installation

Install the 35-448 logic card for the Primary Power Fail/Auto-Restart option on the wire wrap side of the Processor back panel at Slot 7, Connector 0 with the apparatus side up. The 17-182F01 and 17-182F02 cables which supply 12VAC on the Processor back panel, as indicated on the cables. Refer to Figure 14. The Primary Power Fail option card is adjusted at the factory.

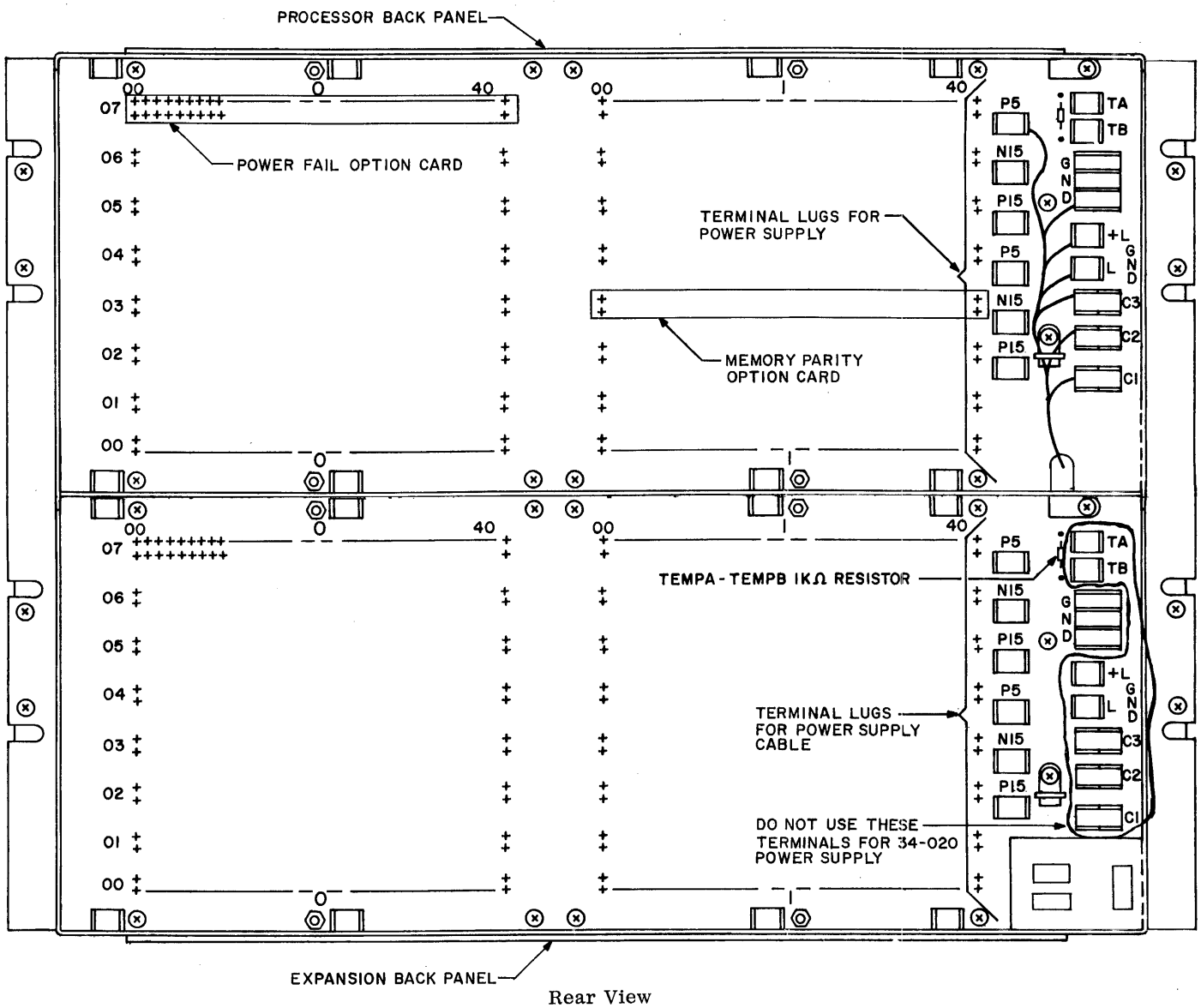
8.2 Memory Access Controller or Direct Memory Access Bus Controller Installation

The 35-527 Memory Access Controller (MAC) or 35-528 Direct Memory Access Bus Controller (DMABC) is installed in Slot 4 of the Processor back panel. The 17-311 MAC to Processor cable connects between Connector 2 of the 35-522 CPU-A board and Connector 2 of the 35-527 MAC or 35-528 DMABC. Refer to 02-348A20 DMABC and MAC Installation Specification for detailed installation instructions.

When installing the 35-527 Memory Access Control board add a wire from 235-0400 to 241-0400.

The following wires must be removed from the Processor back panel Slot 4, Connector 0.

Between	Between
221-0400 and 208-0400-XMA150	207-0400 and 207-0500-MA011
222-0400 and 108-0400-XMA140	206-0400 and 206-0500-MA001
228-0400 and 205-0400-XMA141	107-0400 and 122-0400-MA010
121-0400 and 106-0400-MA000	209-0400 and 209-0500-MA021
123-0400 and 109-0400-MA020	135-0400 and 129-0400-MA050
127-0400 and 110-0400-MA030	136-0400 and 229-0400-MA060
134-0400 and 210-0400-MA040	137-0400 and 130-0400-MA070



Rear View

Figure 14. Rear View Model 7/32 C Twin Chassis

The following jumpers must be changed on the 35-625 CPU-B and the 35-524M01 CPU-C boards.

On the 35-625 CPU-B board

Remove	Add
X to Y	A1 to A3
A2 to A3	B1 to B3
B2 to B3	C1 to C3
C2 to C3	D1 to D3
D2 to D3	

On the 35-524 M01 CPU-C board

Remove	Add
JUMPER J	A1 to A3
A2 to A3	B1 to B3
B2 to B3	C1 to C3
C2 to C3	D1 to D3
D2 to D3	E1 to E3
E2 to E3	F1 to F3
F2 to F3	G1 to G3
G2 to G3	H1 to H3
H2 to H3	

8.3 Extended Selector Channel (ESELCH) Installation

The 35-508 ESELCH board may be installed in Slot 6, 4, 2, 0 of the Expansion back panel. For detailed installation instructions refer to 02-328A20 Extended Selector Channel Installation Specification.

8.4 Memory Parity Option Card

The 35-568 Memory Parity option card must be used with parity memory modules. Parity memory modules and non-parity must not be intermixed on a given processor. The Memory Parity option card mounts on the wire-wrap side of the Processor back panel, slot position 3, connector 1. Refer to Figure 15. When the Processor contains a 35-527 MAC or a 35-528 EDMABC a wire jumper from slot 4, pin 105, connector 0 to ground must be removed when installing the Parity Option card.

9. CONFIGURATION

9.1 System Expansion Chassis

When configuring a multi-chassis system there are four rules that must be followed:

1. The system Expansion chassis must be mounted below the basic Processor chassis.
2. All chassis must be contiguous.
3. All 15 inch system expansion chassis must be mounted above any 10 inch system Expansion chassis.
4. Multiboard peripheral device controllers (on 10 inch circuit boards) can only be used in the 10 inch system Expansion chassis.

9.2 Circuit Board Distribution

Model 7/32 Digital Systems may be configured in a variety of ways. However, the following factors must be considered when determining circuit board distribution within the basic Processor and the system Expansion Chassis.

1. The Extended Selector Channel can be placed in Slots 6, 4, 2, or 0 of the system Expansion back panel.
2. All slots on Connector 1 below the position where the ESELCH is inserted become ESELCH Bus slots. (This only applies within the back panel containing the ESELCH.) The ESELCH Bus extends down the right side connectors (rear view). Note that all device controllers on 10" adapter boards connect to the Multiplexor Bus from the left side connectors (rear view). Therefore, these device controllers may be inserted in vacant ESELCH Bus slots, but will not be on the ESELCH Bus. This also applies to all 7" boards on adapters, installed on the left side.
3. The ESELCH Bus can be extended by cable to any even numbered slot in an I/O chassis. In this case, the I/O Multiplexor Bus must be cut between the even numbered slot and the slot above it.
4. All device addresses are hard-wired on the device controller cards, (device addresses may be changed at option) so that the distribution of I/O device controllers in the chassis normally need be considered as a matter of priority in the RACK0/TACK0 "daisy-chain" and convenience.
5. The 15 inch system Expansion Chassis, and the basic Processor Chassis may only be used for single board I/O device controllers unless the interconnection between boards takes place via cables installed on the outer edge of the board. For multi-board 10 inch device controllers, the 10 inch system Expansion Chassis must be used.
6. The interrupt priority of a given device controller is determined by its physical location on the serial RACK0/TACK0 line. Refer to 9.3 Interrupt Priority Back Panel Wiring to determine which physical location has what priority. When deciding which devices should have a higher or lower priority, devices that must be serviced in a certain amount of time or loss of data access should be given a higher priority than a device with a high interrupt rate and no data loss if not serviced.

9.3 Interrupt Priority Back Panel Wiring

The Acknowledge Control line from the Processor carries the Interrupt Acknowledge (ACK) signal. This line breaks up into a series of short lines to form the "daisy-chain" priority system. The ACK signal must pass through every controller that is equipped with Interrupt Control circuits. Refer to Figure 16 to determine order of priority.

Back panel wiring for interrupt control at a given position is: The Received ACK (RACK0) at Pin 122-0 or 1 and the Transmitted ACK (TACK0) at Pin 222-1 or 0. The daisy-chain bus is formed by a series of isolated lines which connect Terminal 222-1 or 0 of a given position to Terminal 122-1 or 0 of the next position (lower priority). On unequipped positions, a jumper shorts 122-1 or 0 and 222-1 or 0 of the same connector to complete the bus. Back panels are wired with jumpers on all positions. Whenever a card chassis position is equipped with a controller that has a interrupt capability, the jumper from 122-1 or 0 and 222-1 or 0 must be removed from the back panel at that position.

Figure 15, showing the standard interrupt priority wiring, assumes a Model 7/32 C Processor and one memory module. The arrows indicate the direction of priority from the highest priority to the lowest. By changing the wires crossing from Side 0 to Side 1 of the PROC and/or Expansion panels, interrupt priorities may be rearranged. An example of this is shown in Figure 16, Modified Interrupt Priority. Slot 3 on Side 1 of the CPU panel has the highest priority. When Extended Selector Channels (ESELCHs) are installed, the standard interrupt priority must be modified. Refer to Figure 17, Interrupt Priority with ESELCH Installed. Note that if it is decided to install a ESELCH in slot 6 of the Expansion panel, it is necessary to remove the wires connecting the CPU and Expansion panels together, in addition to the wires called out by the ESELCH document number installation procedure. The Multiplexor Bus may be restored to the remaining slots on Side 1 that are not used for private ESELCH Bus. This may be accomplished by the use of a 17-183 cable. To prevent this, install the ESELCH as low as possible in the chassis. This same situation exists when installing a bus buffer into the chassis.

For controllers that occupy several positions, the jumper is removed only at the position where the controller board has ATN/ACK circuits. For details on the various devices, see the appropriate installation specification.

9.4 Terminators

The termination end of both legs, Connector 0 and 1, of the Multiplexor Bus must have a standard INTERDATA termination card (35-433) installed. These cards are installed, on the back panel at the lowest numbered slot of both connectors on the Multiplexor Bus that exists, e.g. If an Extended Selector Channel or bus buffer is installed in Slot 4 on the first expansion chassis and only the Processor Chassis and one Expansion Chassis is used in the system, the Multiplexor Bus must be terminated at Slot 0, Connector 0, and Slot 5, Connector 1 of the Expansion Chassis. In addition, the buffered bus or the ESELCH private I/O Bus should be terminated at Slot 0, Connector 1 of this chassis.

Depending upon system configuration, any ESELCH private I/O Bus or buffered bus may be terminated by a 15" Terminator (35-433) or a 10" Terminator (35-434). The choice of terminators depends on the type of chassis in which the last slot of the bus is present.

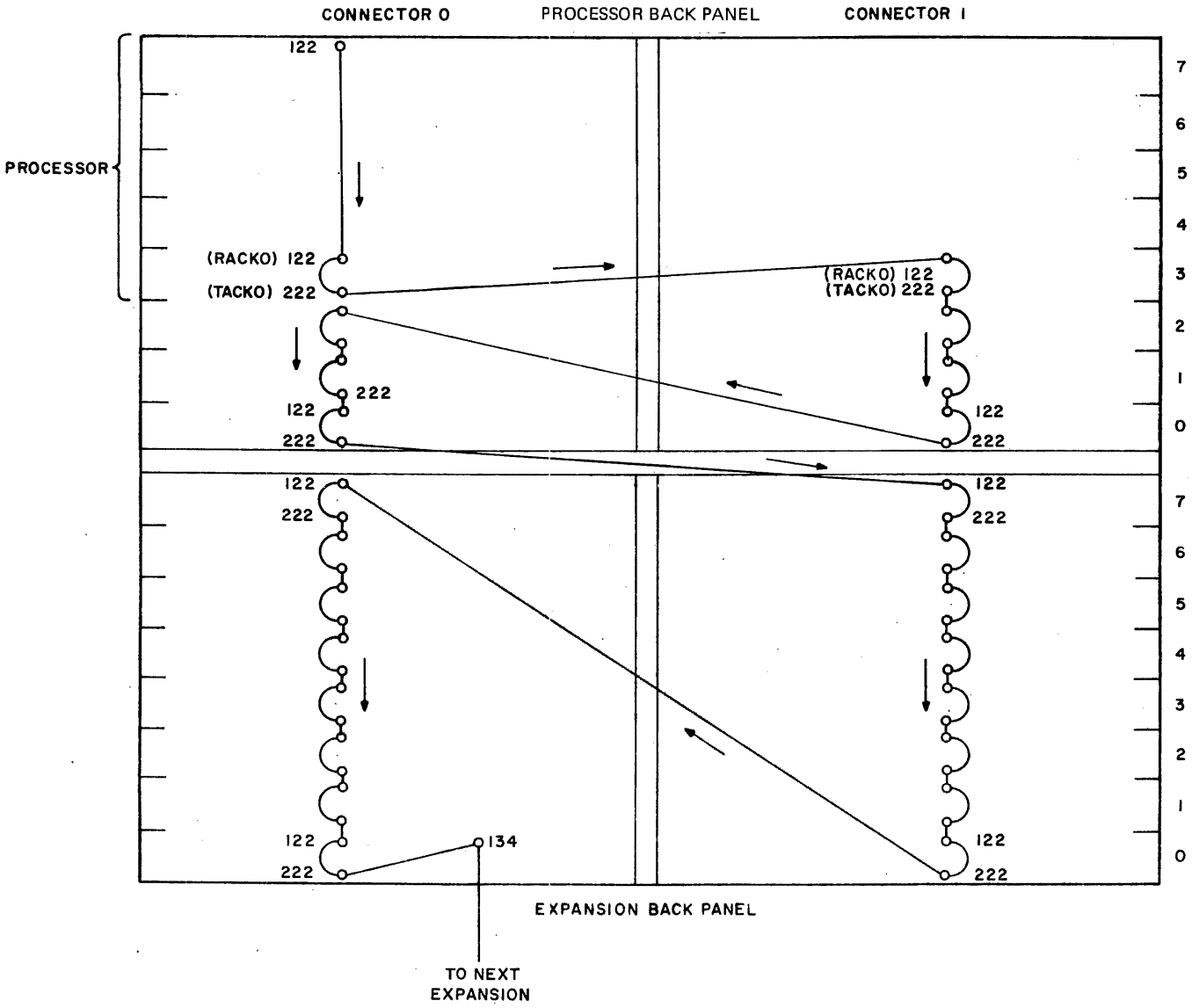


Figure 15. Standard Interrupt Policy

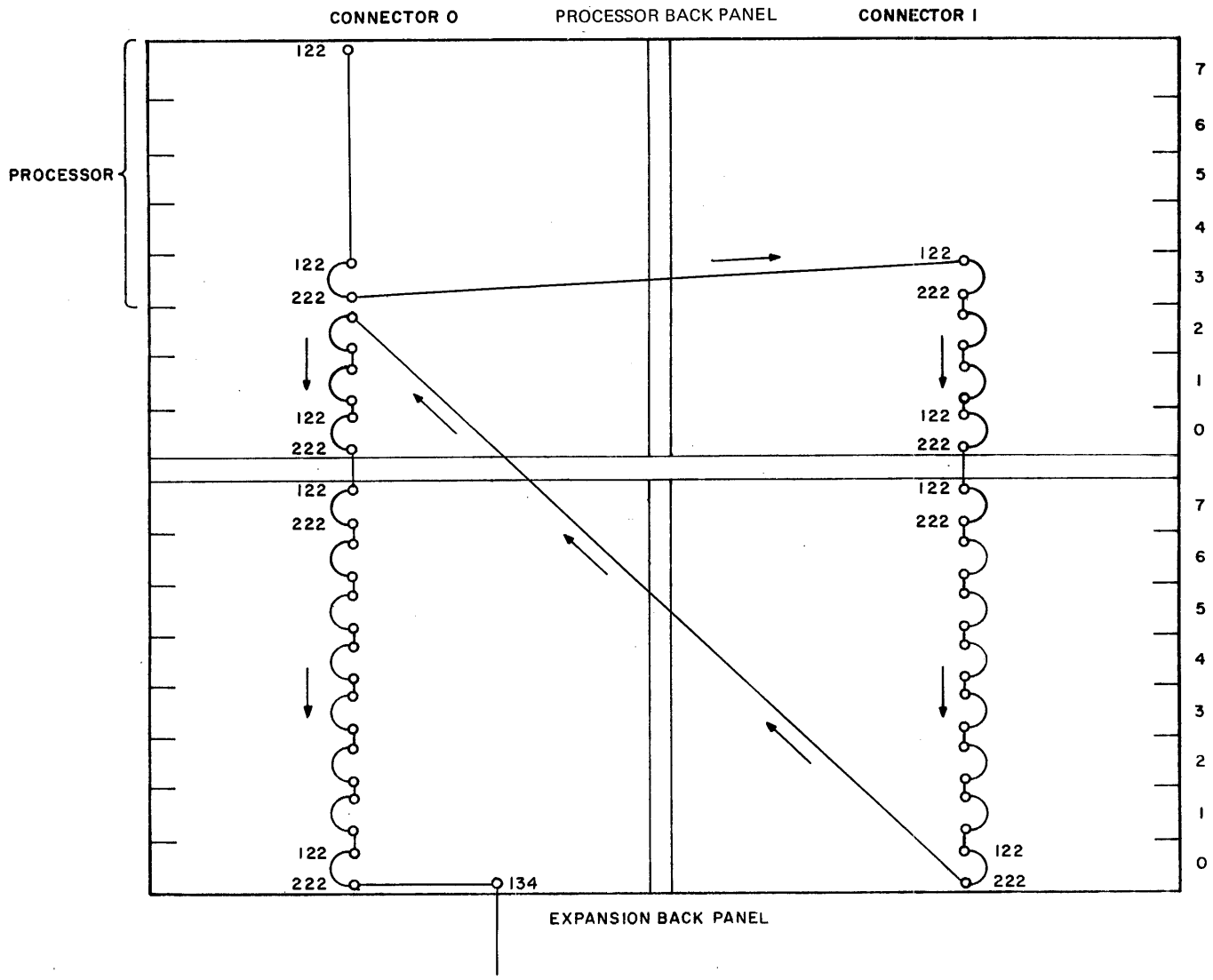


Figure 16. Modified Interrupt Priority

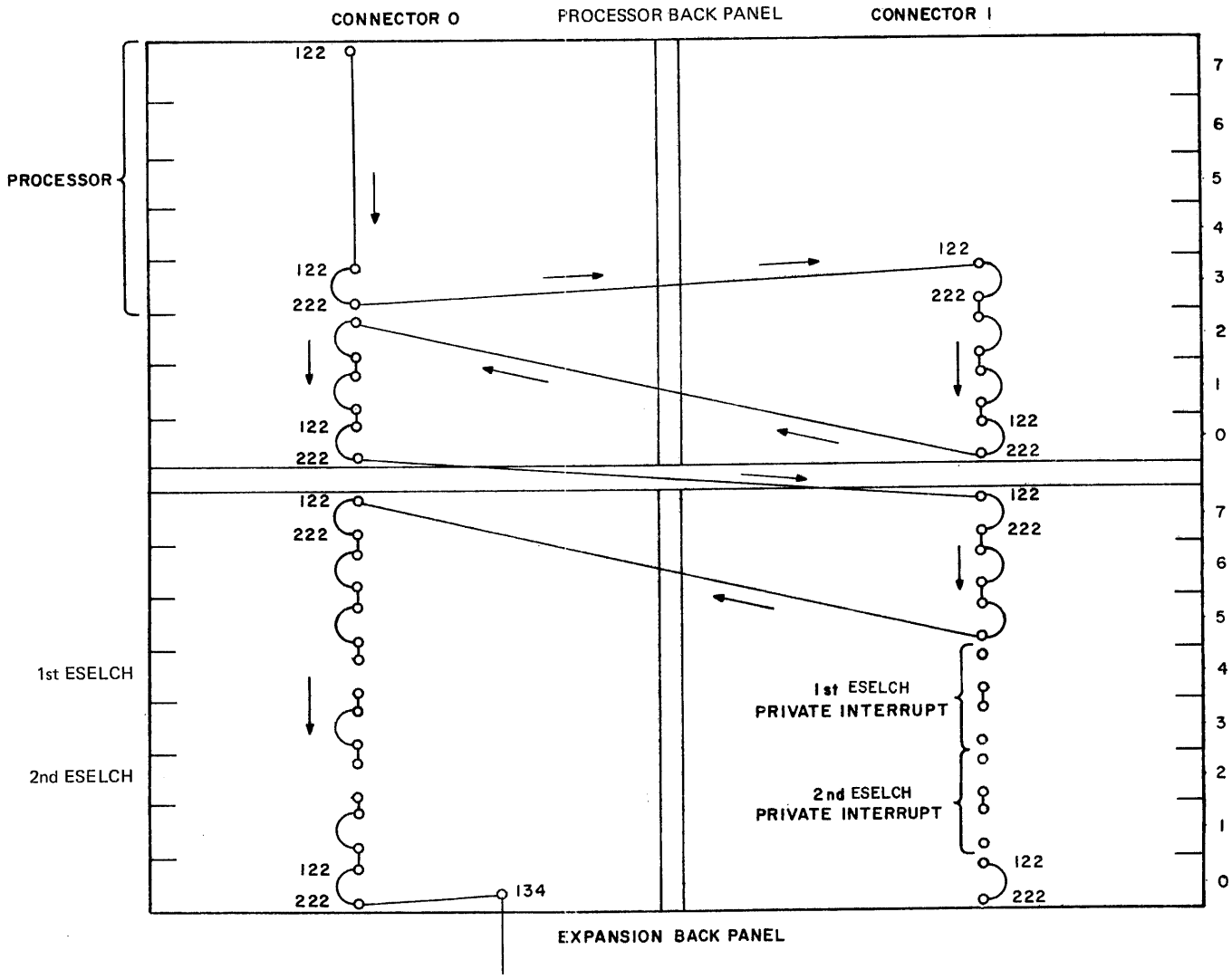


Figure 17. Interrupt Priority with ESELCH Installed.

10. CABLES

10.1 Power Cable

The standard INTERDATA Cabinet is wired for 30 Ampere service. On the main power cable (part of the AC Distribution Panel), there is a three wire, twist lock, grounding, 125VAC, 30 Ampere, UL, (Hubbel #2610) plug. A three wire grounding, 30 Ampere, 125 VAC receptacle (Hubbel #2611 or equivalent) is required to accept this plug.

10.2 System Expansion Cable

A number of standard cables are available for configuring systems made up of the INTERDATA Expansion Chassis discussed in Section 4. The choice of cables is dependent upon system configuration. The following cables are available:

These cables are always used in pairs.

1. 17-193: I/O Expansion Cable, Connector "0"

This cable is used to connect the "0" connector field between two adjacent 15" card files.

2. 17-194: I/O Expansion Cable (see note)

This cable is used to connect the "1" connector I/O fields between two adjacent 15" card files.

3. 17-216: I/O Expansion Cable, 36 Inch Long

This is a 36" long cable. It can be used to connect two 15" files that are not adjacent.

It must not be used to extend the basic Processor Mutiplexor Bus.

It can be used to extend a buffered bus or a ESELCH Bus. It plugs into a "1" side connector. The "receiving" end can plug into the "0" or "1" side of the expansion file.

4. 17-214: 15" to 10" Expansion Cable

This cable is used to connect the "0" connector field of a 15" card file to a lower adjacent 10" card file. It provides an 8 bit I/O bus to the 10" card file.

5. 17-166: 15" to 10" I/O Expansion Cable, 36 Inch Long

This cable is used to connect the "1" side of a 15" expansion file to a 10" expansion file. It provides an 8 bit I/O bus to a 10" card file.

It must not be connected to the basic Processor Multiplexor Bus.

It may be driven either by a Extended Selector Channel or a bus buffer.

It can be used on the older 10" card file (13 I/O slot).

6. 17-183: "0" to "1" Connector

This cable can be used to interconnect the I/O Multiplexor Bus of the "0" field and the "1" field within a 15" card file. There is no RACK0/TACK0 wire in this cable.
It can also be used to connect a "0" side (Slot 0) of a file, to the "1" side (Slot 7) of the next adjacent file, or vice versa.

7. 17-215: 10" to 10" I/O Expansion Cable

This cable is used to connect two adjacent 10" card files.

8. 17-326: EDMA/I/O Connector 0

9. 17-327: EDMA/I/O Connector 1

10. 17-328: EDMA only Connector 0 36-inches

11. 17-329: EDMA only Connector 1 36-inches

12. 17-311: MAC to Processor cable

13. 17-312: MAC to EDMA cable

NOTE

On the receive end of either a 17-327 or 17-194 cable, a strap is installed in the factory. This strap must be removed unless the cable is being used to jumper a private I/O Bus (ESELCH or bus buffer). This strap jumpers Pin 222-0001 of the upper chassis to Pin 122-0701 of the first expansion chassis. If these cables are used to extend an ESELCH or bus buffer, the following wiring changes are required on the lower chassis:

Remove the strap from Pin 134-0700 to Pin 122-0701

Add the strap from Pin 134-0700 to Pin 122-0700

11. CONFIGURATION RULES

1. A maximum of 15 device controllers may be installed on the Multiplexor Bus of the Model 7/32 C or 7/16 HSALU. This assumes a driver capable of sinking 48 ma or greater and no more than one TTL load (2 ma max) on any Control Line or Data Line per device controller.

2. The Multiplexor Bus must be contained within the CPU chassis and two adjacent 7" Expansion Chassis. (Three adjacent chassis if the CPU chassis is a single chassis.) The Multiplexor Bus must be buffered by a Bus Buffer or the equivalent for systems which require the Multiplexor Bus to be extended beyond two Expansion Chassis or in any case where the bus must be extended by any cable greater than 5" in length.

01-097A21
February, 1976

M-71 SERIES MODEL 7/16 HSALU
M-73 SERIES MODEL 7/32 C
MAINTENANCE SPECIFICATION

1. INTRODUCTION

A family of Processors are represented by the 7/16 and 7/32 C model numbers. This family covers the entire spectrum of performance levels from the 16-bit basic, Model 7/16 Basic, to the faster and more powerful 16-bit Model 7/16 HSALU (High Speed Arithmetic Logic Unit) and finally to the maxi-mini Model 7/32 C which is a 32 bit Processor with the capability of directly addressing one million bytes of main memory.

Each machine is a fourth generation Processor suitable for use in data communications, process control, or stand-alone scientific applications. These Processors are modularly constructed for ease of maintenance and are compatable with all building blocks in the INTERDATA product line.

2. SCOPE

This specification describes the functional operation of both the Model 7/16 HSALU and the Model 7/32 C Processors and provides maintenance information useful to the digital technician in maintaining these Processors. A block diagram analysis; a micro-program description, and functional analysis of major Processor areas are included.

3. BLOCK DIAGRAM ANALYSIS

Refer to the Block Diagram in Figure 1.

3.1 System Organization

The Model 7/16 HSALU and 7/32 C Processors are organized between two 16-bit buses. The B Bus is used to present data to the Arithmetic Logic Unit (ALU). The S Bus then transfers the ALU output to the appropriate destination. The source and destination of data on the B Bus and S Bus, as well as the function performed by the ALU is controlled by micro-instructions contained in the Read-Only-Memory (ROM) In the 7/32 C Processor an extension of four bits as appended to the B and S Busses which is used for address manipulation by the micro-program. This extension provides a 20-bit path in the machine for calculating an address.

3.2 Read-Only-Memory (ROM)

The Read-Only-Memory is a high speed, solid-state, non-destructive memory organized into five, six or seven pages of 256 words each depending on the Processor. Each word in ROM is 24 bits long and represents one micro-instruction. Each micro-instruction read out of ROM is placed in the 24 bit ROM Data Register (RD). **RD is the Instruction Register for the micro-Processor. Most micro-instructions** are executed in one machine cycle of 250 nanoseconds. RD bits are decoded to select a Source to be statically unloaded to the B Bus. The ALU then forms a result on the S Bus. This result becomes available some time before the end of the machine cycle. At the start of the next machine cycle the appropriate destination register is loaded and the next micro-instruction is fetched. The meaning of the micro-instruction word bits is explained later.

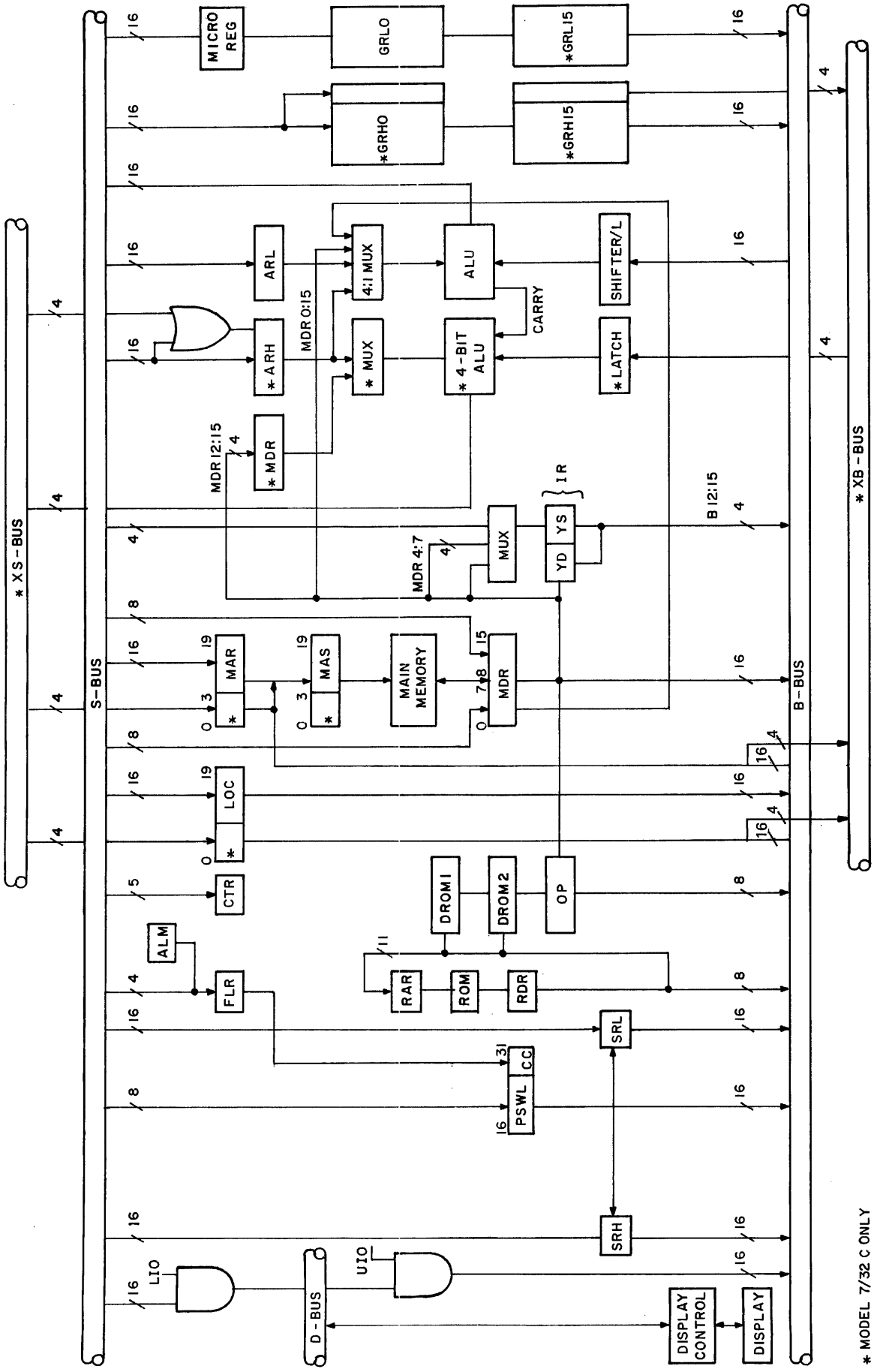


Figure 1. Block Diagram, 7/16 HSALU and 7/32 C PROCESSOR

* MODEL 7/32 C ONLY

Locations in the ROM are addressed by the 11 bit ROM Address Register (RAR). Micro-instructions are normally located at sequential addresses in the ROM. The RAR is an up/down counter which increments by one as each new micro-instruction is read into RD. The RAR therefore holds the address of the next micro-instruction to be executed. When it becomes necessary to jump out of sequence, RAR can be loaded with a new address from the RD register, from the Decoder Read-Only-Memories, or it can be preset by the hardware.

3.3 Flag Register (FLR)

The Flag Register (FLR) is a four-bit register containing the following flags: Carry (C), Overflow (V), Greater than Zero (G), and Less than Zero (L). These flags are modified at the conclusion of arithmetic and logical micro-operations to reflect the result of the operation. The FLR is loaded from Bits 12 through 15 of the S Bus when either the FLR or the Program Status Word (PSW) is the specified Destination Register. The Flag Register may also be loaded from the Alarm Register (ALM). The ALM is a three bit register which is used to indicate the following: Parity Fail on a Data Read, Parity Fail on an Instruction Fetch and an Early Power Failure.

3.4 Program Status Word (PSW)

The Model 7/16 HSALU Program Status Word (PSW) is a 16-bit register used to indicate the system status relative to the user program being emulated. Bits 0 through 16 of the PSW define enabled interrupts and the operational status or mode of the user level Processor. Some of the PSW bits have hardware significance while others are of significance only to the micro-program. Bits 12 through 15 of the PSW make up the Condition Code field (CC) which reflects the result of the previous user instruction.

The Status portion of the Model 7/32 C PSW is 32 bits long. Only 16 bits, however, are implemented in the hardware of this machine. For this Processor, Bits 16 through 27 represent the present state of the machine and Bits 28 through 31 make up the Condition Code field which reflects the result of the previous user instruction.

The Condition Code may only be updated from the FLR. When PSW is the specified Destination Register, Bits 0 through 11 of the S Bus are loaded into Bits 0 through 11 of the PSW and S Bus Bits 12 through 15 are captured in the FLR. The Condition Code field remains unchanged until the micro-program causes it to be updated from the FLR or when the hardware, in the case of an instruction read, copies the contents of the FLR into the Condition Code.

The Location Counter (LOC) is a 16-bit (20-bit for the Model 7/32 C) appendum to PSW which holds the main memory address of the next user instruction to be performed.

3.5 Main Memory

The Main Memory consists of random access memory providing storage for user instructions and data. The Memory Address Register (MAR) is a 16-bit register (20 bit for the Model 7/32 C) which is loaded with the address of main memory locations. Memory is actually addressed by the Memory Access Slave Register (MAS). MAS is automatically updated from MAR at the start of each memory cycle. Data read from or written into memory is buffered in the Memory Data Register.(MDR). The micro-program initiates a main memory cycle by issuing a memory read, memory write, privileged write, or instruction read command. After issuing a memory command, the micro-program is free to do other instructions. The memory cycle is accomplished asynchronous of other Processor activity. If the micro-program, however, attempts to use the contents of MDR after a memory read or instruction read before memory data becomes available, or attempts to load MDR or issue another memory command before the current memory cycle is complete, the Processor stops until the desired function can be performed.

With core memory, a memory cycle consists of two phases. First, the contents of the specified location are read out and placed into the MDR. The location is set to zeros (destructive read-out). The contents of MDR are then written into the specified location. A memory read consists of a read cycle that saves the contents of the specified location in MDR. The contents of the MDR are then written back to the specified location on the write cycle. A memory write does not save the read-out so that the specified location is written with the contents of MDR. An instruction read differs from a memory read in that after the data becomes available in MDR, it is automatically transferred to the user's Instruction Register.

3.6 Instruction Register (IR)

After an instruction read has been issued, when the read-out is available in MDR, MDR Bits 0 through 7 are placed in the register labeled OP, Bits 8 through 11 are placed in the register labeled YD, and Bits 12 through 15 are placed in the register labeled YS. These three registers (OP, YD, and YS) comprise the user's Instruction Register.

3.7 Decoder Read-Only Memory (DROM)

The OP Register is used to address locations in the pair of Decoder Read-Only-Memories (DROM1 and DROM2). Each DROM contains 256 12-bit words. The micro-program can interrogate either DROM1 or DROM2 at anytime other than on a Branch or Input/Output micro-instruction. The least significant 11 bits of the resulting read-out are jammed into the RAR, resulting in an automatic branch to an address that is related to the user's operation code. Bit 4 of DROM1 is used to indicate priviledged instructions.

3.8 General Registers (GR)

The micro-program accesses the user's General Registers without caring which of the 16 General Registers the user instruction has specified. It matters that when the micro-program accesses a GeneralRegister for emulating a user instruction that it be the General Register specified in that user instruction. Since after instruction read, the register address or addresses specified by the user are in the YD and YS Register, the micro-program can access the appropriate General Register by specifying the YD or YS Instruction Register. The hardware then selects the General Register whose number is in the YD or YS Register.

The YD Register is an up/down counter so that sequential General Registers can be accessed. The micro-program can also clear the YD Register when it needs to access specific General Registers. The YS Register, in addition to being loaded at the time of an instruction fetch, may also be loaded by the micro-program from the S Bus.

In the Model 7/16, sixteen 16-bit General Registers are provided for the user programs while in the 7/32 C two sets of sixteen 32-bit General Registers are provided. These registers are labeled GRH0 and GRL0 which is Set 0 and GRH15 and GRL15 which is Set 15.

3.9 Micro-Registers (MR)

The seven 16-bit registers MR0 through MR6 are available to the micro-program for general purpose use.

3.10 Arithmetic Registers High and Low (ARH and ARL)

Two 16-bit A Registers are used to hold the second operand for arithmetic and logical micro-operations. These registers plus the Memory Data Register (MDR) and the sign of MDR (Bit 0) are used as the 'B' input to the Arithmetic Logic Unit (ALU). The other input, input 'A', to the ALU is the output of the Shifter/Latch. The Shifter can Shift B Bus data left or right one bit position, do an eight-bit rotate, or gate the B Bus data directly into the ALU.

3.11 Arithmetic Logic Unit (ALU)

The ALU comprises a 16-bit parallel arithmetic/logic network with look-ahead carry. The arithmetic or logical result is formed on the 16-bit S bus. On the Model 7/32 C a four-bit extension to the ALU is used which forms its result on the four-bit XS Bus.

3.12 Data Output (for special hardware features)

Data Output operations for special hardware features are achieved by gating S Bus data onto the D Bus and activating special control and address lines.

3.13 Input/Output (I/O)

Input/Output operations are achieved by gating S Bus data onto the D Bus and activating an I/O Control line, or by activating an I/O Control line and gating the D Bus data onto the B Bus.

3.14 Shift Register High (SRH) and Shift Register Low (SRL)

These two registers, SRH and SRL, **are 16-bit general purpose micro-registers which can also be** used in combination as a 32-bit shift register. The extended shift capability is used in multiply, divide, and other 32-bit operations.

3.15 Counter

The Counter (CTR) is a five-bit decrementing register used on multiply, divide, repeat operations, and on the Branch on Counter micro-instruction. The counter is loaded by the micro-program from the S Bus with any value from 0 to 31. The state of this register, zero or non-zero, may be tested by the micro-program when a Branch on Counter is specified by the instruction.

4. MICRO PROGRAM DESCRIPTION

4.1 Introduction

Micro-programming is a means for implementing the control logic of a digital computer. At INTERDATA, micro-programming has been effectively used to maintain upward compatibility in a family of Processors whose internal hardware varies from one member to the next.

The Models 7/16 HSALU and 7/32 C are designed to execute micro-instructions stored in a Read-Only Memory (ROM). Each micro-instruction causes one or more hardware functions to be performed, such as transferring the contents of one register to another, arithmetic or Boolean operations between registers, controlling input/output operations, or initiating main memory accesses.

A series of micro-instructions is called a micro-program. The complete micro-program for each machine is by definition, an emulator, causing the hardware to react to a user program in main memory and to external events as would the Processor described in the User's Manual, Publication Number 29-261 or 32 Bit Series Reference Manual, Publication Number 29-365. Every user instruction, interrupt handling feature, and Hexadecimal Display Panel function is simulated by some portion of the micro-program.

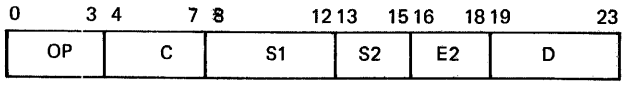
This section describes the micro-program for the Model 7/16 HSALU and 7/32 C Processors. The microprocessor of the two machines are identical but the compliment of hardware available in these two Processors vary. For example; all references to 20 bit registers in this description are implemented as 16 bit registers in the Model 7/16 HSALU. In addition, only one set of 16 bit General Registers is equipped on the 7/16 while two sets of 32 bit General Registers are available on the Model 7/32 C.

4.2 Micro-Instruction Formats and Modifiers

Micro-instructions for the Models 7/16 HSALU and 7/32 C have fixed length but their format is variable. All micro-instructions are 24 bits long and are highly encoded. The Processor has six basic micro-instruction formats. The operation code is found in the first four bits of every instruction format, but the interpretation of other bits varies from one format to the other.

4.2.1 Register to Retister (RR) Format.

RR FORMAT



OP	Operation Code
C	Control Modifier
S1	First Source Operand
S2	Second Source Operand
D	Destination Register
E2	Opcode Extension Two Modifiers

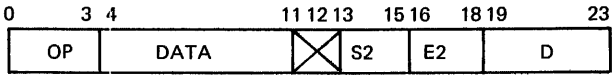
The following six micro-instructions use this RR format.

AND	(N)
OR	(O)
XOR	(X)
ADD	(A)
SUBTRACT	(S)
CALCULATE ADDRESS	(CA)

All instructions with this format contain a four bit operation code, a four bit control modifier, a five bit first operand specification, a three bit second source specification, a five bit destination specification, and three bit opcode extension modifiers. These six micro-instructions are described in Section 4.3, and a detailed description of instruction modifiers appears in Section 4.2.8. Section 4.2.7 describes all addressable sources and destinations.

4.2.2 Register Immediate (RI) Format.

RI FORMAT



OP	Operation Code
DATA	The least significant eight bits of the first operand.
S2	Second Source
D	Destination Register
E2	Opcode Extension Two Modifiers

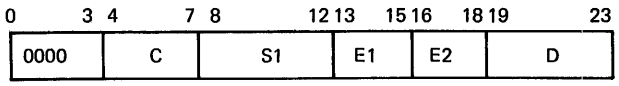
There are five micro-instructions with this format.

AND Immediate	(NI)
OR Immediate	(OI)
Exclusive OR Immediate	(XI)
Add Immediate	(AI)
Subtract Immediate	(SI)

All of the previous instructions contain a four bit operation code and eight bits of immediate data. The eight bit immediate field is expanded to a 20 bit value with the high order 12 bits forced to zero. This 20 bit value forms the first operand. The second operand source and the destination register are specified by the S2 and D fields. The E2 field specifies opcode extension modifiers (see Section 4.2.8). Bit 12 is not used in this format.

4.2.3 Load (L) Format.

L FORMAT



C Control Field

S1 First Operand

D Destination Register

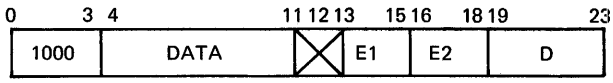
E2 Opcode Extension Two Modifiers

E1 Opcode Extension One Modifier

This format is used only by the Load micro-instruction. This micro-instruction does not require any second operand. Bits 13 through 15 of the micro-instruction, are therefore, used for specifying additional modifiers (see Section 4.2.8 for description of opcode Extension One modifiers).

4.2.4 Load Immediate (LI) Format.

LI FORMAT



DATA Least Significant Eight Bits of Source Operand

D Destination Register

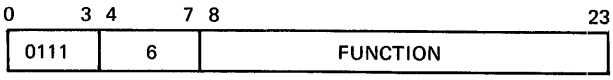
E1 Opcode Extension One Modifier

E2 Opcode Extension Two Modifiers

This format is used by the Load Immediate micro-instruction. The eight bit immediate field is expanded to a 20 bit value with the high order 12 bits forced to zero. This 20 bit value forms the source operand for the load operation. Bit 12 of the micro-instruction is not used by this format.

4.2.5 Command Format (C).

C FORMAT



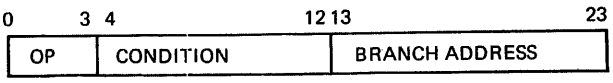
C Control Modifier

FUNCTION Function Field

The Command micro-instruction uses this format. The four-bit C field specifies the control modifier, and a 16 bit function field specifies various functions to be performed by the Command micro-instruction.

4.2.6 Branch (BR) Format.

BR FORMAT



OP Operation Code

CONDITION Condition to be Tested

BRANCH ADDRESS Address of the next micro-instruction if branch is taken

This format is used by two Branch micro-instructions (Branch on True Bit 3 reset and Branch on False Bit 3 set).

4.2.7 Source and Destination Registers. There are several general purpose and special purpose micro-registers which can be used for sources and destinations. These sections describe addressable sources and destinations.

First Operand Source Registers

The sources that may be used as the first operand are shown in Table 1.

MR0, MR1, MR2, MR3, MR4, MR5, and MR6 are seven general purpose micro-registers. They can be used freely as 16 bit sources.

PSWL is a 16 bit register which is used to hold the Program Status Word. This register can be used as a 16 bit source.

Location Counter is a special micro-register which can be used as a 20 bit source. The most significant four bits of the Location Counter can be accessed separately by specifying LOCH as the first source. Specifying LOCH as the first source causes the most significant four bits of LOC to be gated on to the B Bus, Bits 12 through 15.

SRH and SRL are two special purpose shift registers which can be used as 16 bit sources.

Memory Address Register holds the address of the main memory location to be accessed. This register can be used as a 20 bit source register.

TABLE 1. ADDRESSABLE FIRST OPERAND SOURCES

RD BITS					SYMBOLIC REGISTER	MEANING
8	9	10	11	12		
0	0	0	0	0	MR0	Micro-register 0
0	0	0	0	1	MR1	Micro-register 1
0	0	0	1	0	MR2	Micro-register 2
0	0	0	1	1	MR3	Micro-register 3
0	0	1	0	0	MR4	Micro-register 4
0	0	1	0	1	MR5	Micro-register 5
0	0	1	1	0	MR6	Micro-register 6
0	0	1	1	1	PSWL	Program Status Word Low
0	1	0	0	1		
0	1	0	1	0		
0	1	0	1	1		
0	1	1	0	0	YSI	YS Field
0	1	1	0	1	YDI	YD Field
0	1	1	1	0		
0	1	1	1	1	OP	Operation Code
1	0	0	0	0	NULL	NULL Source
1	0	0	0	1	LOCH	Location Counter High
1	0	0	1	0	SRL	Shift Register Low
1	0	0	1	1	SRH	Shift Register High
1	0	1	0	0	LOC	Location Counter
1	0	1	0	1	IO	Input (D Bus to B Bus)
1	0	1	1	0	MDR	Memory Data Register
1	0	1	1	1	MAR	Memory Address Register
1	1	0	0	0	YDH	MS 16 bits of reg. specified by YD
1	1	0	0	1	YDL	LS 20 bits of reg. specified by YD
1	1	0	1	0	YDLP1	LS 20 bits of reg. specified by YD
1	1	0	1	1	YDLM1	LS 20 bits of reg. specified by YD
1	1	1	0	0	YSH	MS 16 bits of reg. specified by YS
1	1	1	0	1	YSL	LS 20 bits of reg. specified by YS
1	1	1	1	0	YSLX	LS bits of reg. specified by YS
1	1	1	1	1	YSHX	MS 16 bits of reg. specified by YS

Memory Data Register is available as a 20 bit first operand source. If MDR is specified as the source and the memory data is not available (after a memory read operation), execution of that micro-instruction is suspended until memory data is available.

The user's 16 general purpose registers do not have individual addresses. The General Registers are accessed indirectly through the YD or YS field. If YDL is specified as the first source, the least significant 20 bits of the General Register whose number is contained in the YD field (Bits 8:11 of the user instruction) are selected as the source value. Specifying YDLP1 (YDLM1) is the same as specifying YDL except that the YD field is incremented (or decremented) by one after the execution of the micro-instruction. If the current micro-instruction uses YDLP1 or YDLM1 as the source, the next micro-instruction cannot specify YD for the source operand. Specifying YDH selects the most significant 16 bits of the General Register specified by the YD field (Model 7/32 only).

YSL, when used as a source, selects the least significant 20 bits of the General Register specified by the YS field. If YSH is used as the source operand, the most significant 16 bits of the General Register are used as the source value (Model 7/32 C only). Specifying YSLX or YSHX is the same as specifying YSL or YSH except that the source value is force to zero if the YS field (Bits 12 through 15 of the user instruction) is zero.

If YDI or YSI is specified as the source, the YD field (Bits 8 through 11 of user instruction) or the YS field (Bits 12 through 15 of user instruction) is gated onto B Bus Bits 12 through 15.

When I/O appears as the source operand, an input operation is performed. Only in a Load micro-instruction can I/O be a source. The nature of the input request is specified by Bits 16 through 18 of the micro-instruction. When the device responds, the data is gated on to the B Bus. Completion of the micro-instruction is suspended until the device responds or a false sync occurs (14 microsecond time set).

When OP is specified as the first source operand, the operation code (Bits 0 through 7) of the user instruction is gated onto the B Bus Bits 0 through 7.

If the first operand is NULL all the bits on B and XB Busses are forced to zero.

NOTE

If the selected source has a 20 bit value the most significant four bits are gated onto the XB Bus and the least significant 16 bits are gated onto the B Bus. If the selected source has less than 20 bits, it is expanded to a 20 bit value by forcing high order bits to zero. The most significant four bits of this expanded value are gated to the XB Bus and the least significant 16 bits are gated to the B Bus.

Second Operand Sources

The sources that may be used as the second operand are shown in Table 2.

TABLE 2. ADDRESSABLE SECOND SOURCES

RD BITS			SYMBOLIC	MEANING
13	14	15		
0	0	0	NULL	NULL Value (ZERO)
0	0	1	ONE	Constant ONE
0	1	0	ARL	Arithmetic Register Low
0	1	1	TWO	Constant TWO
1	0	0	MDR	Memory Data Register
1	0	1	SIGN	SIGN of MDR
1	1	0	AR	Arithmetic Register
1	1	1	ARH	Arithmetic Register High

Specifying NULL for the second source forces the second operand value to zero.

If ONE or TWO is specified as the second operand, a constant value of 1 or 2 is used as the second operand value.

If ARL is specified as the second source, the least significant 16 bits of the 32 bit Arithmetic Register (ARH, ARL) are used as the second source operand. If ARH is specified as the second source, the most significant 16 bits of the 32 bit Arithmetic Register are used as the second operand value. If AR is specified as the second source, the least significant 20 bits of AR are used as the second operand.

Memory Data Register can be used as a 20 bit second operand. If the MDR has been used as the second source, and data is not available, execution of the micro-instruction is suspended until data is available. MDR should not be used as the second operand by a micro-instruction which specifies a Memory Read operation or Instruction Read operation in the control field.

If SIGN is specified as the second operand and MDR Bit 4 (sign of 16 bit value) is zero, the second operand value is forced to zero. If SIGN is specified as the second source and MDR Bit 4 (Sign of 16 bit value) is 1, the second operand is forced to all 1s. SIGN should not be used as the second operand by a microinstruction which specifies memory read or instruction read.

Destination Registers

The registers which can be used for the destinations are shown in Table 3. Some of the destinations are 20 bit destinations and others are 16 bit destinations. If a 20 bit destination is specified, the most significant four bits of the destination register are loaded from the XS Bus and the least significant 16 bits of the destination register are loaded from the S Bus. If the specified register is 16 bits long, the destination register is loaded from the S Bus and the data on the XS Bus is ignored.

General purpose micro-registers MR0 through MR6 and shift registers SRH and SRL can be used as 16 bit destination registers in any arithmetic and logic micro-instruction.

TABLE 3. ADDRESSABLE DESTINATIONS

RD BITS					SYMBOLIC REGISTER	MEANING
19	20	21	22	23		
0	0	0	0	0	MR0	Micro-register 0
0	0	0	0	1	MR1	Micro-register 1
0	0	0	1	0	MR2	Micro-register 2
0	0	0	1	1	MR3	Micro-register 3
0	0	1	0	0	MR4	Micro-register 4
0	0	1	0	1	MR5	Micro-register 5
0	0	1	1	0	MR6	Micro-register 6
0	0	1	1	1	PSWL	Program Status Word Low
0	1	0	0	0	CTR	Counter
0	1	0	0	1	ARL	Arithmetic Register Low
0	1	0	1	0	ARH	Arithmetic Register High
0	1	0	1	1	AR	Arithmetic Register
0	1	1	0	0	YSI	YS Immediate
0	1	1	0	1	HWA	OUTPUT (S BUS TO D BUS)
0	1	1	1	0	PSWH	Program Status Word High
0	1	1	1	1	FLR	Flag Register
1	0	0	0	0	NULL	NULL Destination
1	0	0	0	1		
1	0	0	1	0	SRL	Shift Register Low
1	0	0	1	1	SRH	Shift Register High
1	0	1	0	0	LOC	Location Counter
1	0	1	0	1	IO	Output (S Bus to D Bus)
1	0	1	1	0	MDR	Memory Data Register
1	0	1	1	1	MAR	Memory Address Register
1	1	0	0	0	YDH	MS 16 bits of reg. specified by YD
1	1	0	0	1	YDL	LS 16 bits of reg. specified by YD
1	1	0	1	0	YDLP1	LS 16 bits of reg. specified by YD
1	1	0	1	1	YDLM1	LS 16 bits of reg. specified by YD
1	1	1	0	0	YSH	MS 16 bits of reg. specified by YS
1	1	1	0	1	YSL	LS 16 bits of reg. specified by YS
1	1	1	1	0		
1	1	1	1	1		

PSWH and PSWL are 16 bit destination registers. When PSWH or PSWL is specified as the destination, the least significant four bits from the S Bus are captured in the Flag Register (FLR). The least significant four bits of PSWL (Condition Code) can only be loaded from FLR by specifying the proper control modifier or by a command instruction.

The Location Counter is a 20 bit destination register. When LOC is loaded with a 20 bit value, MAR is loaded simultaneously with the same 20 bit value.

Memory Address Register (MAR) is a 20 bit destination register. If a micro-instruction specifies a main memory operation and uses MAR as the destination, the memory operation is started before changing the Memory Address Register.

Memory Data Register is available as a 16 bit destination (Bits 4:19 of MDR). If the MDR is specified as the destination, and memory is still busy (because of a previous memory read or write operation), execution of that micro-instruction is suspended until memory is not busy.

General Registers can be specified as destination registers indirectly through the YD and YS fields. Specifying YDH destination causes the most significant 16 bits of the General Register (specified by the YD field) to be loaded from the S Bus (Model 7/32 C only). If YDL is specified as the destination the least significant 16 bits of the General Register (specified by YD field) are loaded from the S Bus. Specifying YDLP1 (or YDLM1) is the same as specifying YDL except that the YD field is incremented (or decremented) by one. If the current micro-instruction specifies YDLP1 or YDLM1 as the destination, the next micro-instruction cannot specify YD as the source operand.

If YSH (Model 7/32 C only) or YSL is used for the destination, the most significant (or least significant) 16 bits of the General Register (specified by YS field) are loaded from the S Bus.

When the Counter is used as the destination register, the least significant five bits of the S Bus are loaded into the Counter Register.

If FLR is specified as the destination register, the least signficant four bits of the S Bus are loaded into the Flag Register. Loading the Flag Register in an instruction that normally sets flags causes an ORing of the resulting flags and S Bus data.
specifies flags causes ORing of the resulting C, V, and G flags and an ANDing of the L flag and the S Bus Data.

When YSI is the destination, the YS field of the Instruction Register is loaded from the least significant four bits of the S Bus.

ARL and ARH are two 16 bit destinations. AR is a 20 bit destination. When AR is specified as the destination, the least significant four bits of ARH are loaded from the XS Bus and ARL is loaded from the S Bus.

When I/O appears as the destination an I/O operation is performed. Only a Load or Load Immediate Micro-instruction can specify I/O as the destination. The nature of the output operation is encoded into the Operation Extension One Modifier Field.

4.2.8 Instruction Modifiers. Instruction modifiers can modify the function specified by the operation code. Modifiers are grouped into three categories as follows:

1. Control Modifiers (C)
2. Opcode Extension One Modifiers (E1)
3. Opcode Extension Two Modifiers (E2)

1. Control Modifiers (C)

These modifiers control the memory operations, DROM operations, and modification of the Condition Code. A micro-instruction can specify only one of these modifiers since they are mutually exclusive. The control modifier is specified by the C field of the micro-instruction. The following paragraphs of this section describe various control modifiers.

No Action

C Field	Symbolic
0000	

No control function is performed.

Memory Read and Increment LOC

C Field	Symbolic
0001	MRI

A memory read operation is started using the contents of MAR prior to execution of this micro-instruction as the memory address. The LOC and MAR are then incremented by two.

Vector through DROM1

C Field	Symbolic
0010	D1

The next sequential micro-instruction is executed and then control is transferred to the ROM address obtained by vectoring through DROM1 (using operation code of the user instruction as index). If the most significant bit of DROM1 entry is set, the corresponding user instruction is a priviledged instruction. If PSW Bit 23 is set and the Most Significant Bit (MSB) of DROM1 entery is set, the least significant eight bits of the ROM Address Register are forced to hexadecimal value 'FF' (i.e., a branch is taken to the last word on the current ROM page).

Vector through DROM2

C Field	Symbolic
0011	D2

The next sequential micro-instruction is executed and then control is transferred to the ROM address obtained by vectoring through DROM2. If the user instruction being emulated is RHR, RH, WHR, or WH and the I/O device is a byte oriented device, Bit 14 of the ROM Address Register is forced to 1 (the 11 bit address is contained in Bits 5 through 15 of ROM Address Register).

Instruction Read

C Field	Symbolic
0100	IR

Memory read operation for fetching the next user instruction is started. The following additional operations are performed.

- The next sequential micro-instruction is executed. The next micro-instruction should not be a Branch micro-instruction and it must not specify YSH, YSL, YSLX, YSHX, or YSI for source or destination. The control field of the next micro-instruction must specify no action.
- The data from main memory is loaded into the Instruction Register (IR) when data becomes available).
- The Flag Register is cleared after the completion of the next micro-instruction.
- LOC and MAR are incremented by two.
- If no interrupt is pending, control is transferred to START routine (at '001'). If any interrupt is pending or if control console is in the SINGLE mode, the control is transferred to HELP routine (at '045').
- XMDR is cleared.

Instruction Read and Jam Condition Code Half

C Field	Symbolic
0101	IRJH

The control function performed is same as IR except that the contents of the Flag Register is copied into the Condition Code after the next micro-instruction has been executed.

Instruction Read and Jam Condition Code

C Field	Symbolic
0111	IRJ

Same as IRJH.

Memory Read

C Field	Symbolic
1000	MR

Memory read operation is started before loading the destination register.

Memory Read and Increment MAR

C Field	Symbolic
1001	MR2

Memory read operation is started and then MAR is incremented by two.

Memory Read and Disable Memory Access Controller

C Field	Symbolic
10101	MRD

For any memory read or write operation the address contained in MAR is relocated by Memory Access Controller (MAC) if enabled by setting Bit 21 of PSW. If this option is specified, the address contained in MAR is not changed by the MAC and a memory read operation is initiated (Model 7/32 C only).

Extended Read and Increment MAR by Two

C Field	Symbolic
1011	XR2

This control function is the same as MR2 except that the least significant four bits (Bits 16: 19) of the previous contents of MDR are copied to the most significant four bits (Bits 0:3) of the current MDR. For normal read operation, the most significant four bits of MDR are not changed (Model 7/32 C only).

Memory Read with MAC Disabled, Increment MAR

C Field	Symbolic
1101	MRD2

Same as MR2 except that address contained in MAR is not changed by MAC. (Model 7/32 C only.)

Memory Write

C Field	Symbolic
1110	MW

Memory write operation is started. If the current micro-instruction specifies a memory write operation and it uses MDR as the destination register, the new value of MDR is written into the addressed memory location.

Memory Write and Increment MAR by Two

C Field	Symbolic
1111	MW2

Memory write operation is started and then MAR is incremented by two.

Memory Write with MAC Disabled

C Field	Symbolic
1100	MWD

This control function is same as Memory Write (MW) except that memory address is not changed by MAC. (Model 7/32 C only.)

NOTE

If a micro-instruction specifies a memory read or memory write operation, the address of the memory location to be accessed should be loaded into MAR prior to the execution of this micro-instruction. If MAR is specified as destination, the new value is loaded into MAR after starting the memory operation.

2. Opcode Extension One Modifiers (E1)

The E1 field is valid with the Load or the Load Immediate micro-instructions only. Four mutually exclusive modifiers are included in this class. These modifiers are described in the following paragraphs.

Shift Right

E1 Field	Symbolic
100	Shift Right

The source data (from the B Bus) is shifted by the B Bus shifter, right one place and copied into the specified destination register.

Shift Left

E1 Field	Symbolic
010	SL

The source data (from the B Bus) is shifted left one place and copied onto the specified destination register.

Cross Shift

E1 Field	Symbolic
110	CS

The source data (from the B Bus) is rotated eight bit positions and copied into the destination register. If MDR is the source or destination, the cross shift will occur only if MAR is even. If MDR is the destination and MAR is even, only the high byte of MDR (Bits 4 through 11) is loaded. **If MAR is odd,** only the low byte of MDR (Bits 12 through 19) is loaded. The bits not loaded remain unchanged. This special feature of MDR is used for emulating byte instructions.

Length

E1 Field	Symbolic
XX1	LEN

If the user instruction being emulated is of RX3 format (refer to Model 7/32 Reference Manual, Publication Number 29-399), the constant two is loaded into the destination register. If the user instruction is not of RX3 format, zero is loaded into the destination register. MDR must be used as the source operand when this modifier is specified. This modifier is not for general use. The 7/32 C micro-program uses this modifier to emulate some branch instructions.

3. Opcode Extension Two Modifiers (E2)

The E2 field of a micro-instruction specifies this class of instruction modifiers.

If the source or destination is not I/O, the following three modifiers can be specified. These modifiers are not mutually exclusive, so two or more of them can be specified simulataneously.

Carry In

E2 Field	Symbolic
1XX	CI

If the micro-instruction using this modifier is a Load or Load Immediate micro-instruction, the state of the carry flag is shifted into the most significant (if shift right is specified) or the least significant bit (if shift left is specified) of the result.

If the micro-instruction using this modifier is an Add or Add Immediate instruction, the carry flag is added with the least significant bit of the sum.

If the micro-instruction specifying this modifier is a Subtract or Subtract Immediate Instruction, the carry flag represents the borrow situation from the least significant bit of the source data. This borrow participates in the subtraction operation.

If the micro-instruction specifying this modifier does not perform a load, add, or subtract operation, the modifier is ignored.

Carry Out

E2 Field	Symbolic
X1X	CO

If the micro-instruction specifying this modifier performs a load operation, the Carry flag stores the state of the bit shifted out (if shift operation is specified). If shift modifier is not specified by load micro-instruction, the Carry flag is reset.

If the micro-instruction specifying carry out performs an AND, OR, or Exclusive OR operation, the Carry flag is reset.

If the micro-instruction specifying carry out performs an AND, OR, or Exclusive OR operation, the carry flag is reset.

Flags

E2 Field	Symbolic
XX1	F

This modifier is used to enable modification of the flags (V, G, and L) if the micro-instruction specifying F modifier performs an add or subtract operation. G, L and V flags are adjusted to reflect the result of the operation. G and L flags are adjusted to reflect the algebraic value of the result. The V flag is adjusted to reflect the overflow condition.

If the micro-instruction specifying F modifier performs a load or logical operation, V flag is reset and G and L flags are adjusted to reflect the algebraic value of the result.

NOTE

The flags G, L and V reflect the result obtained from 16 bit ALU. The four bit extension to the ALU is used only for address arithmetic and it des not change any flags. The hardware provides a cumulative flage affect to facilitate multi-precision operations. Once the G or L flag becomes set, the G and L flags will never again be both zero unless the flag register is explicitly cleared.

Result	Flags Before Execution		Flags After Execution	
	G	L	G	L
ZERO	0	0	0	0
	0	1	1	0
	1	0	1	0
POSITIVE	0	0	1	0
	0	1	1	0
	1	0	1	0
NEGATIVE	0	0	0	1
	0	1	0	1
	1	0	0	1

If the source or destination of a Load micro-instruction is I/O the following seven modifiers can be specified by E2 Field.

Data Channel Acknowledge (7/16 HSALU only)

E2 Field	Symbolic
000	DCAK

The source data is present on the data lines, and the address and data channel acknowledge control lines are active. The highest priority interrupting data channel device becomes the On-Line device.

Address

E2 Field	Symbolic
001	ADRS

The source data is present on the date lines, and the address control line is active. The device that detects its address becomes On-Line and responds with Sync.

Data Available

E2 Field	Symbolic
010	DA

The source data is present on the data lines, and the data available control line is active. The On-Line device accepts the data and responds with a Sync.

Output Command

E2 Field	Symbolic
011	OC

The source data is present on the data lines, and the output command control line is active.

Acknowledge Interrupt

E2 Field	Symbolic
100	ACK

The acknowledge interrupt control line is active. The highest priority interrupting device responds by placing its address on the data lines. The input data is copied to the destination register.

Data Request

E2 Field	Symbolic
101	DR

The data request control line is active. The On-Line device responds by placing data on the data lines. The input data is copied to the destination register.

Status Request

E2 Field	Symbolic
110	STAT

The status request control line is active. The On-Line device responds by placing status data on the data lines. The input data is copied to the destination register.

4.3 Micro-instructions

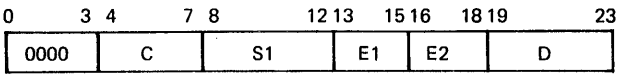
The 7/32 C Processor executes 16 basic micro-instructions. This section describes these 16 micro-instructions. For each micro-instructions the assembler format is shown. The machine instruction format is diagrammed, a description of the instruction is provided, and allowed instruction modifiers are indicated. The execution time of a micro-instruction is given in terms of the number of machine cycles required to complete it. One machine cycle equals 250 nanoseconds.

Arithmetic and logic operations use 20 bit operands. If a specified operand is less than 20 bits long, it is expanded to a 20 bit value (with high order bits forced to zero) before the specified operation is performed. If the specified destination is a 20 bit register, a 20 bit result is loaded into the destination register. If the specified destination is a 16 bit register, the least significant 16 bits of the result are loaded into this register and most significant four bits of the result are ignored.

4.3.1 Load

L D, S1, OPTIONS

Timing: 1 Cycle (No I/O)
2 Cycles (Input I/O)
3 Cycles (Output I/O)



The contents of the register specified by the first source field (S1) are copied into the register specified by the destination field (D).

OPTIONS

If neither the source nor destination field specifies I/O, the following instruction modifiers can be used:

C Field	Any Control Modifier
E1 Field	SR, SL, CS, or LEN
E2 Field	One or more of the following:
	CI, CO, F

If the source or destination field specifies I/O, the following instruction modifiers are used:

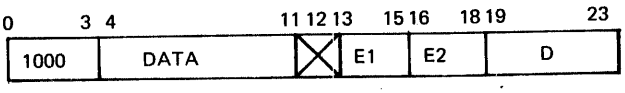
C Field	Any Control Modifier
E1 Field	SR, SL, or CS
E2 Field	DCAK*, ADRS, DA, OC, ACK, DR or STAT

*7/16 HSALU only

4.3.2 Load Immediate

LI D, DATA, OPTIONS

Timing: 1 Cycle (No I/O)
3 Cycles (Output I/O)



The eight bits from the data field are copied into the least significant eight bits of the register specified by the D field. The most significant eight bits (12 bits for 20 bit destination) of the destination are forced to zero.

OPTIONS

If the destination field does not specify I/O, the following modifiers can be used:

E1 Field	SR, SL, or CS
E2 Field	One or more of the modifiers CI, CO, and F.

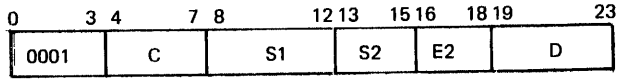
If the destination field specifies I/O, the following modifiers can be used:

E1 Field	SR, SL, or CS
E2 Field	DCAK, ADRS, DA, or OC

4.3.3 AND

N D,S1, S2, OPTIONS

Timing: 1 Cycle



The contents of the register specified by the first source field (S1) are logically 'ANDed' with the contents of the register specified by the second source field (S2). The logical product is loaded into the register specified by the destination field.

OPTIONS

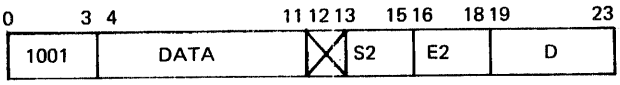
Any of the following instruction modifiers can be specified as options.

C Field	Any Control Modifier
E2 Field	One or more of CI, CO, and F

4.3.4 AND Immediate

NI D, DATA, S2, OPTIONS

Timing: 1 Cycle



The eight bit data field is expanded to a 20 bit value with high order 12 bits forced to zero. This 20 bit value is logically ANDed with the contents of the register specified by the second source field (S2). The logical product is loaded into the register specified by the destination field.

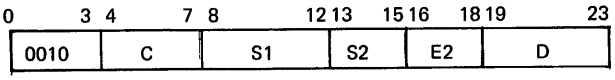
OPTIONS

E2 Field One or more of the following three modifiers:

CI, CO, and F

4.3.5 OR

O D, S1, S2, OPTIONS **Timing: 1 Cycle**



The first operand and second operand are logically added (or ORed). The logical sum replaces the contents of the specified destination register.

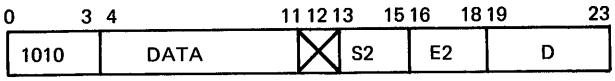
OPTIONS

C Field Any Control Modifier

E2 Field One or more of CI, CO, and F

4.3.6 OR Immediate

OI, D, DATA, S2, OPTIONS **Timing: 1 Cycle**



The eight data field is expanded to a 20 bit immediate value with high order 12 bits forced to zero. This immediate value is logically added (or ORed) to the second operand. The logical sum is loaded into the specified destination register.

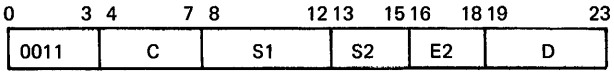
OPTIONS

E2 Field One or more of the following modifiers:

CI, CO, and F

4.3.7 Exclusive OR

X D, S1, S2, OPTIONS **Timing: 1 Cycle**



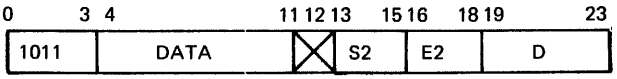
The first operand (specified by S1) is 'Exclusive ORed' with the second operand. The resulting logical difference is placed into the register specified by the destination field (D).

OPTIONS

C Field	Any Control Modifier
E2 Field	One or more of CI, CO, and F

4.3.8 Exclusive OR Immediate

XI D, DATA, S2, OPTIONS **Timing: 1 Cycle**



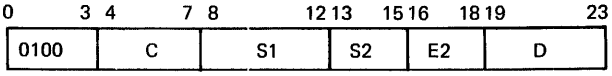
The eight bit data field is expanded to 20 bit immediate value with high order 12 bits forced to zero. This immediate value is 'Exclusive ORed' with the second operand. The resulting logical difference replaces the contents of the destination register.

OPTIONS

E2 Field	One or more of the following modifiers:
	CI, CO, and F

4.3.9 Add

A D, S1, S2, OPTIONS **Timing: 1 Cycle**



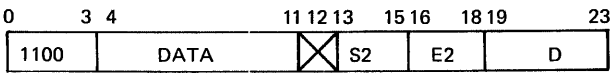
The second operand is algebraically added to the first operand. The sum replaces the contents of the destination register.

OPTIONS

C Field	Any Control Modifier
E2 Field	One or more the modifiers
	CI, CO, and F

4.3.10 Add Immediate

AT D, DATA, S2, OPTIONS **Timing: 1 Cycle**



The eight bit data field is expanded to 20 bit immediate value with high order bits forced to zero. This immediate value is added to the second operand. The sum replaces the contents of the destination register.

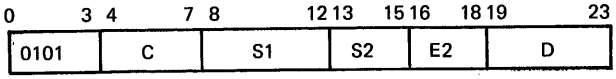
OPTIONS

E2 Field — One or more of the following modifiers can be specified as options:

CI, CO, F

4.3.11 Subtract

S D, S1, S2, OPTIONS — **Timing: 1 Cycle**



The second operand is algebraically subtracted from the first operand. The difference is loaded into the register specified by the destination field.

OPTIONS

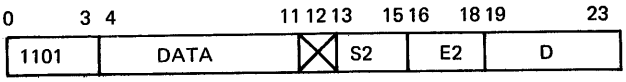
C Field — Any Control Modifier

E2 Field — One or more of the following modifiers:

CI, CO and F

4.3.12 Subtract Immediate

SI D, DATA, S2, OPTIONS — **Timing: 1 Cycle**



The eight bit data field is expanded to 20 bit immediate value with high order bits forced to zero. The second operand is subtracted from the expanded immediate operand, the difference is loaded into the register specified by the destination field.

OPTIONS

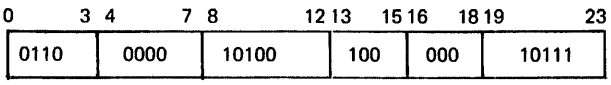
E2 Field — One or more of the modifiers

CI, CO and F

4.3.13 Calculate Address

CA MAR, LOC, MDR

3 Cycle (RX1 or RX2)
5 Cycles (RX3)



The Calculate Address instruction is a very powerful and special purpose micro-instruction. This micro-instruction has been specifically designed to improve the efficiency of the Instruction Fetch and operand Fetch processes of the RX format user instructions with the Model 7/32 C emulation. The following conditions should be satisfied when the Calculate Address instruction is executed.

1. **The first source and the second source registers must be LOC and MDR respectively. The destination register must be MAR. The Control field (C) and Opcode Extension Two (E2) field must specify no action.**

2. Memory Data Register (MDR) should contain the second halfword of an RX instruction, or the memory read operation for fetching the second halfword should be in progress.

3. The Location Counter and the Memory Address Register must contain the current user instruction address plus four.

An RX instruction can specify any one of three RX formats (refer to Model 7/32 Reference Manual, Publication Number 29-399). The particular RX format is specified as follows:

Most Significant Two Bits of the Second Half Word of the User Instruction		RX Format
Bit 16	Bit 17	
0	0	RX1
1	X	RX2
0	1	RX3

The Calculate Address micro-instruction examines the most significant two bits of the second halfword of the user instruction (contained in Bits 4 and 5 of the MDR) and determines which one of the three RX formats has been used. If the user instruction is of the RX1 format, the least significant 14 bits of the second halfword (contained in Bits 6 through 19 of the MDR) are expanded to a 20 bit value by forcing the high order bits to zero. This 20 bit value is added to the least significant 20 bits of the index value specified by the YS field. The 20 bit sum is loaded into the MAR.

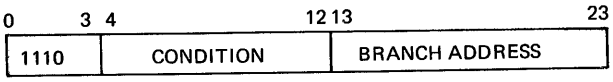
If the current user instruction is of the RX2 format the least significant 15 bits of the second halfword (contained in Bits 5 through 19 of the MDR) are expanded to a 20 bit value by propagating the most significant bit (Bits 5 of MDR) through the high order bits. This 20 bit value, 20 bit value contained in the Location Counter, and the least significant 20 bits of the index value are added to form the 20 bit effective address of the second operand. This 20 bit address is loaded into the MAR.

If the current user instruction is of the RX3 format, the **Calculate Address micro-instruction starts extended** memory read operation (XR2) to fetch the third halfword of the user instruction, and then increments LOC and MAR by two. While waiting for the memory data to become available, the Processor adds the least significant 20 bits of the first index value (contained in the General Register specified by Bits 12 through 15 of the user instruction) to the least significant 20 bits of the second index value (contained in the General Register specified by Bits 24 through 27) of the user instruction. The 20 bit sum forms the effective index value. When the memory data becomes available, **the MDR Bits 0 through 19 contain the 20 bit address** specified by Bits 28:47 of the user instruction. The Processor adds this 20 bit address to the 20 bit effective index value. The resulting 20 bit effective address is loaded in to the Memory Address Register.

4.3.14 Branch On True

BT CONDITION, ADDRESS

1 Cycle (No Branch)
2 Cycles (Branch)



The **Branch on True micro-instruction results in a transfer to the Branch Address if any of the specified** conditions is true. If none of the specified conditions is true, the next sequential micro-instruction is executed. The branch conditions to be tested are specified by Bits 4 through 12 of the micro-instruction. See Table 4 for the branch conditions.

If counter = 0 (CNTR) is specified as the branch condition, the transfer takes place only if the **counter** Register contains a zero value. The Counter is decremented by one after testing the condition.

TABLE 4. BRANCH CONDITIONS

CONDITION FIELD									SYMBOLIC CONDITION	MEANING
4	5	6	7	8	9	10	11	12		
0	0	1							C	Carry Flag Set
0	0		1						V	Over Flow Flag Set
0	0			1					G	Greater Than Flag Set
0	0				1				L	Less Than Flag Set
0	0					1			MSK1	Mask (AND Operation Between YD Field and Condition Code Produce Non-Zero Result)
0	0						1		WAIT	Processor is in Wait State (PSW Bit 16=1)
0	0							1		
0	1	1							ATNX	I/O Attention and PSW Bit 17=1 and No Higher Priority Interrupt is Present
0	1		1						HWA	Fast Floating Point Option Presence (7/32 C)
0	1			1					QUE	PSW Bit 22 is Set
0	1				1				RR	Current User Instruction is an RR or SF Format Instruction
0	1					1			ATN	I/O Attention and PSW Bit 17 Set
0	1						1		MAC	MAC Interrupt and PSW Bit 21 Set
0	1							1		
1	0	1							SNGL	Console Single Mode
1	0		1						CATN	Console Attention
1	0			1					DC	Data Channel Requests
1	0				1				DRD	(7/16 HSALU)/COMM Option Presence (7/32C)
1	0					1			MALF	Machine Malfunction
1	0						1		PPF	Primary Power Fail
1	0							1		
1	1	1							HWIO	Halfword I/O Line is Active
1	1		1						NNORM	Not Normalized (SRH Bits 8 through 11 are 0)
1	1			1					CNTR	Counter Contains a Zero Value
1	1				1				ARST	Auto Restart Present
1	1	0	0	0	0	1	0	0	UT	Utility Flip-Flop Set
1	1						1		SHORT	User Instruction is of RX1 or RX2 Format
1	1							1		

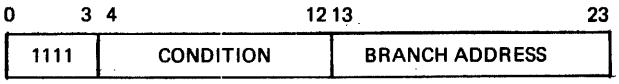
4.3.15 Branch on False

BF CONDITION, ADDRESS

Timing: 1 Cycle (No Branch)
2 Cycles (Branch)

or

B ADDRESS (condition field is forced to zero by the assembler)



The Branch on False micro-instruction results in a transfer to the Branch Address if none of the specified conditions is true. If any of the specified conditions is true, the next sequential micro-instruction is executed. The branch conditions to be tested are specified by Bits 4 through 12 of the micro-instruction. See Table 4 for the branch conditions.

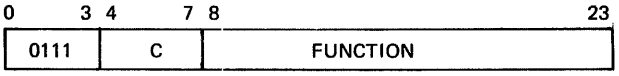
If Counter = 0 (CNTR) is specified as the branch condition, the transfer takes place only if the Counter Register does not contain a zero value. The counter is decremented by one after testing the branch condition.

4.3.16 Command

C FUNCTION + CONTROL OPTIONS

Timing: 1 Cycle (except MPY, DIV, RPT, and UNMPY)
10 Cycles (MPY or UNMPY)
16 Cycles (DIV)

16 Cycles (DIV)



The Command micro-instruction instructs the Processor to perform the functions specified by the function field (Bits 8 through 23 of the micro-instruction). The following paragraphs describe the various command functions (see Table 5).

Multiply (MPY)

The Processor multiplies the 16 bit multiplicand in MDR (Bits 4 through 19) by the 16 bit multiplier in SRL. The 32 bit signed product is obtained in SRH and SRL. The following set up conditions must exist prior to the execution of the command micro-instruction.

1. MDR contains the multiplicand in two's complement form.
2. ARL contains twice the multiplicand in two's complement form.
3. SRL contains the multiplier in two's complement form.
4. Carry flag contains the most significant bit of the multiplicand.

TABLE 5. FUNCTIONS (FOR COMMAND MICRO-INSTRUCTIONS)

FUNCTION FIELD																SYMBOLIC FUNCTION	MEANING
8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23		
1	0				1											MPY	Multiply
1	1				1											UMPY	Unsigned Multiply
		1				1										DIV	Divide
			1	0	0											SL1	Shift (SRH,SRL) Left One Place
			1	0	1											SL2	Shift (SRH,SRL) Left Two Places
			0	1	0											SR1	Shift (SRH,SRL) Right One Place
			0	1	1											SR2	Shift (SRH,SRL) Right Two Places
						1										CI	Carry In
									1							CO	Carry Out
								0									
								0		1	0	0				SUT	Set Utility Flip-Flop
								0		0	1	0				CUT	Clear Utility Flip-Flop
								0		1	1	0				TUT	Toggle Utility Flip-Flop
								0				1				RPT	Repeat
								0					1			SWA	Set Wait Indicator
								0					0			CWA	Clear Wait Indicator
								0						1		POW	Power Down
								0							1	ALRM	Load Alarm Flags
								1									
								1		1							
								1			1					PRIV	Privileged Memory Operation
								1				1				JH	Copy FLR to Condition Code
								1					1				
								1						1		TS	Test and Set
								1							1	CYD	Clear YD Field

The Processor used a fast multiplication algorithm to multiply two 16 bit numbers. The algorithm used by the Processor speeds up the multiplication by pairing the multiplier bits and inspecting one pair at a time. The multiplication process is completed in 10 machine cycles and the signed product in two's complement form is obtained in SRH and SRL.

Unsigned Multiply (UMPY)

This command performs the same operation as MPY except that it multiplies two unsigned 16 bit numbers, and the product obtained in SRH and SRL is an unsigned 32 bit number.

Divide (DIV)

The Processor divides the 32 bit dividend in SRH and SRL by the 16 bit divisor in ARL. To achieve this, the following setup condtions must exist.

1. The Counter contains 16
2. SRH, SRL contain a positive dividend that is less than 65,536 times the divisor magnitude.
3. The ARL contains the divisor in two's complement negative form.
4. Carry flag is reset.

Shift Left One Place (SL1)

The 32 bit shift register (SRH, SRL) is shifted left one place. Carry in and carry out can be specified.

Shift Left Two Places (SL2)

The 32 bit shift register (SRH, SRL) is shifted left two places. The carry in or carry out can be specified, but the carry produced at the end of the first shift is ignored.

Shift Right One Place (SR1)

The 32 bit shift register (SRH, SRL) is shifted right one place. Carry in and carry out can be specified.

Shift Right Two Places (SR2)

The 32 bit shift register (SRH, SRL) is shifted right two places. Carry in and carry out can be specified but the carry produced at the end of the first shift is ignored.

Carry In (CI)

Carry flag is shifted into the most significant bit of the SRH (if shift right) or the least significant bit of the SRL (if shift left).

Carry Out (CO)

The bit shifted out is saved in the Carry flag.

Set Utility Flip-Flop (SUT)

Utility flip-flop is set.

Clear Utility Flip-Flop (CUT)

Utility flip-flop is reset.

Toggle Utility Flip-Flop (TUT)

Utility flip-flop state is complemented

Repeat (RPT)

If the counter is not zero, the next sequential micro-instruction is repeated the number of times specified by the Counter Register. If the Counter is non-zero, reasonable micro-instructions that do not result in a branch can be executed.

Set Wait Alarm (SWA)

The Wait indicator is set

Clear Wait Alarm (CWA)

The Wait indicator is reset

Power Down (POW)

The system is initialized

Copy Alarm Bits (ALRM)

The bits set in the Alarm Register are **'ORed'** with the Flag Register **the next time PSWL is loaded.**

Privileged Memory Operation (PRIV)

If this function is specified, the address contained in MAR is not relocated by MAC, and all memory protection is disabled for this micro-instruction.

Test and Set (TS)

This command function is used to achieve synchronization in **multi-processor systems.** When this function is received in conjunction with a memory read operation, the most significant bit of the addressed word in the common memory is set during the write portion of the same memory cycle. **(Model 7/32 only.)**

Clear YD Field (CYD)

YD field of the Instruction Register is forced to zero.

4.4 Micro-program

The INTERDATA Model 7/32 C is a 32 bit computer. The user instructions on the Model 7/32 C are interpretively executed (emulated) by the micro-program. The micro-program is executed by the micro-processor which has 16 bit wide data paths. Since the host (micro-processor) and target (7/32 C user machine) machine data widths do not match, the micro-program creates a "virtual match" through the proper manipulation of the facilities available on the micro-processor. The micro-program uses multiple precision micro-programming techniques to perform 32 bit operation with 16 bit data paths.

The listing of the Model 7/32 C Firmware or micro-program is documented and self-explanatory for many of the less involved user instructions requiring short execution routines. The latter section on the Emulation Process explains the basic emulation process and the emulation of the simple arithmetic and logic user instruction. The subsequent sections describe the Firmware implementation of some of the more involved user instructions. Console support, interrupt support, and the Auto Driver Channel Firmware routines have also been explained. Most of this description is also applicable to the 7/16 HSALU micro-program.

4.4.1 Emulation Process. At the highest level, the process of emulation can be divided into three major tasks as depicted in Figure 2A: User Instruction **Fetch, Operand Fetch, and Execution.** In Figure 2B, the major tasks are broken into typical subtasks. This general functional diagram applies to the emulation of both the 7/32 C and 7/16 HSALU user machines.

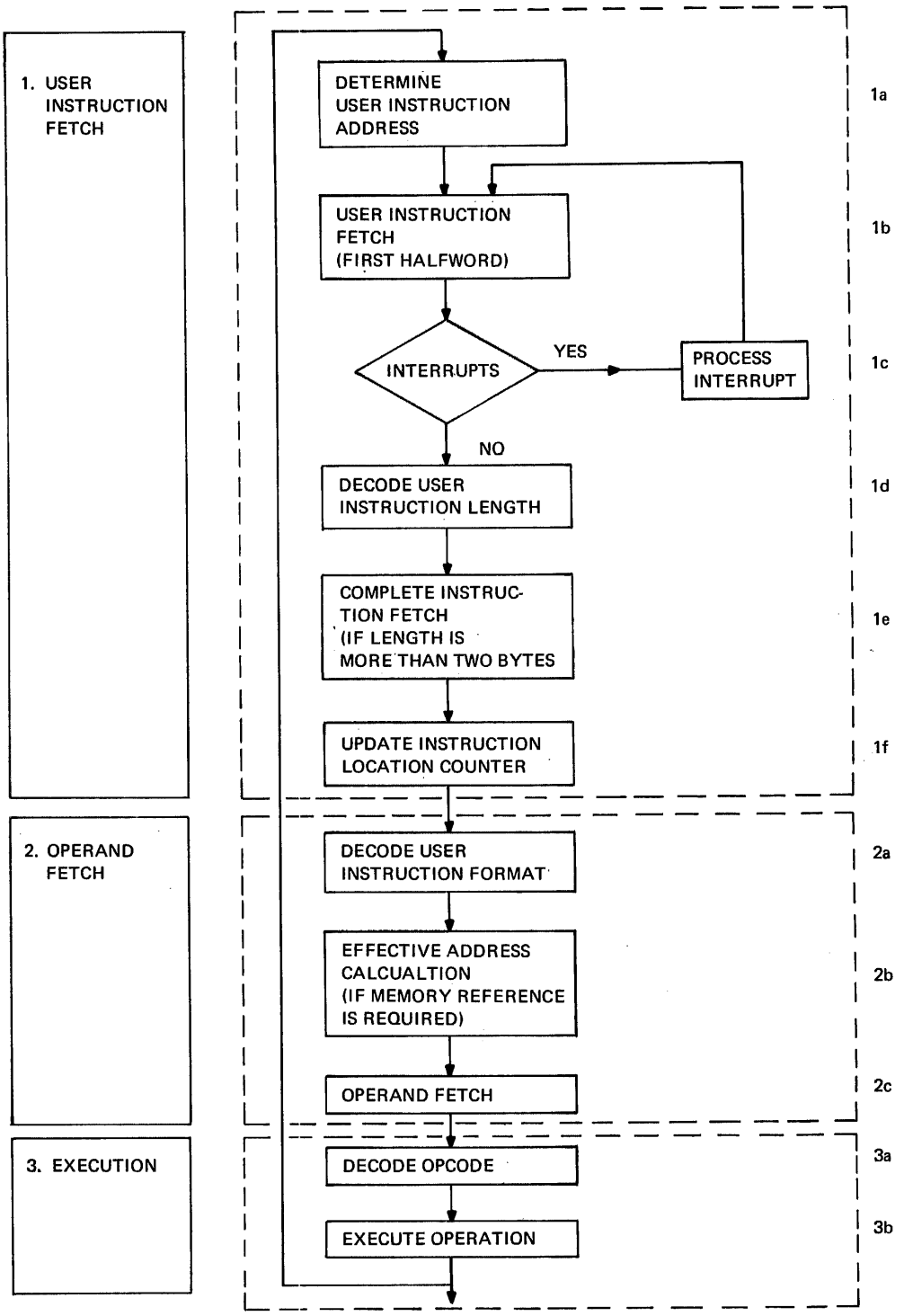


FIGURE 2A: HIGH LEVEL EMULATION TASKS

FIGURE 2B: EMULATION SUBTASKS

Subtasks of the emulation process can be further divided into multiple subtasks. For example, subtask 3B, Execute Operation, consists of many alternate processes, essentially one per operation code. Each of these processes may be represented as one or more subtasks, some of which may be similar to other subtasks in the emulation process.

1. User Instruction Fetch

User instruction fetch begins when a micro-instruction specifying instruction read (in Control Modifier field) is executed. The instruction fetch for the next user instruction is started by the next to last micro-instruction of the execution micro-routine. The execution micro-routine for the current user instruction copies the updated Location Counter (LOC) into the Memory Address Register (MAR) before the execution of the next to the last micro-instruction. The next to the last micro-instruction of this micro-routine then specifies IR, IRJ or IRJH (see Section 4.2.8 for the description of these control modifiers) in its Control Modifier field. The hardware executes the last micro-instruction of the micro-routing and then sets the ROM Address Register to '001' (corresponds to label START on the micro-program listing). If any interrupts are pending, the hardware sets the ROM Address Register to '045' (corresponds to label HELP) instead of '1'. Before transferring control to the micro-instruction at START the hardware increments the Location Counter by two, clears the Flag Register (FLR), resets the Abort flip-flop, and copies the first halfword of the user instruction from the MDR into the Instruction Register (IR)(OP, YD, and YS).

The following two micro-instructions at 'START' load the contents of the General Register specified by the YS field into ARH and ARL (only ARL is loaded for the 7/16 HSALU).

```
START    L    ARH, YSH, D1     (ARH, ARL) = (R2) VECTOR THROUGH
*        L    ARL, YSL, MRI    DROM1; START MEMORY READ AND INCREMENT
                                LOC AND MAR BY TWO
```

The second micro-instruction uses the MRI Control Modifier to fetch the second halfword of the user instruction (see Section 4.2.8 for the description of MRI Control Modifier). If the user instruction is of the SF or RR format, (refer to the 7/32 Reference Manual, Publication Number 29-399 for the description of the user instruction formats) format, this control operation is not performed by the processor.

The instruction decoding can be easily performed using a table look-up on eight bits of the instruction (operation-code), which establishes not only the operation to be performed but also the format and the method of operand fetch. Since most instructions require an operand, a table can be devised to direct the reading of the operand and the subsequent operation to be performed. DROM1 and DROM2 have been designed to implement this look-up procedure. Since any DROM operation is specified one micro-instruction in advance, the table look-up on the op-code is achieved without any time penalty. The micro-instruction at 'START' specifies vectoring through DROM1. The Processor, therefore, interrogates DROM1 after the execution of the micro-instruction at START + 1. If the current user instruction is a fixed point RR or an SF instruction, the ROM address supplied by DROM1 is the execution routine address. If the current instruction is an RI1, RI2, RX1, RX2, RX3 or a Floating Point instruction, the DROM1 address is the Operand Fetch routine address.

2. Operand Fetch

Most user instructions require two operands to perform the specified function. The first operand is contained in a General Register and the second operand is contained either in a General Register or in a memory location. Normally, the execution micro-routine for any arithmetic or logical operation assumes that the second operand is contained in the Arithmetic Register (ARH, ARL). If the current user instruction is of the RR format, two micro-

instructions at 'START', load the Arithmetic Register (ARH, ARL) with the second operand value. If the current user instruction is not an RR format instruction, the appropriate Operand Fetch routine is entered by vectoring through DROM1. The following paragraphs describe the various Operand Fetch routines used by the 7/32 C micro-program.

RI1 Operand Fetch

In an RI1 format instruction, the second operand is obtained by adding the contents of the index register specified by the X2 field to the value contained in the I2 field (refer to the 7/32 Reference Manual, Publication Number 29-399). Before adding the immediate value to the contents of the index register, the 16 bit immediate value is expanded to a 32 bit fullword quantity by propagating the most significant bit through the high order bits. The following two micro-instructions at label RI1 perform this operand fetch operation.

```
RI1     A   ARL, YSLX, MDR, CO + D2    (ARH, ARL) = EXTENDED IMMEDIATE

        A   ARH, YSHX, SIGN, CI        FIELD + INDEX VALUE; VECTOR THROUGH
*                                      DROM 2
```

As explained previously, obtaining the second operand value requires a 32 bit addition. Since the Arithmetic Logic Unit (ALU) cannot perform a 32 bit operation, this addition is accomplished in two steps. The first micro-instruction adds the 16 bit immediate value (now contained in the MDR as a result of the MRI Control operation) to the least significant 16 bits of the 32 bit index value. The arithmetic carry produced is saved in the Carry Flag of the Flag Register. The first micro-instruction also specifies D2 control action (vector through DROM2) so that control is transferred to the appropriate execution routine after the fetch operation is complete. The second micro-instruction adds the most significant 16 bits of the index value. This second micro-instruction also specifies Carry In (CI) in its Opcode Extension Two Modifier (E2) field. Specifying Carry In (CI) instructs the Processor to add the Carry flag of the Flag Register with the least signficant bit of the sum. Thus, a 32 bit sum is obtained in the Arithmetic Register (ARH, ARL).

RI2 Operand Fetch

If the current user instruction is of the RI2 format, the second operand is obtained by adding the contents of the index register specified by X2 to the 32 bit immediate value contained in the I2 field. The following three micro-instructions load ARH and ARL with the second operand value.

```
RI2     L   ARH, MDR, MRI              (ARH) = MS 16 BITS OF IMM. VALUE;
*                                      START THIRD HALFWORD FETCH;
*                                      INCREMENT LOC AND MAR BY TWO

        A   ARL, YSLX, MDR, CO + D2    (ARH, ARL) = IMM VALUE + INDEX VALUE;

        A   ARH, YSHX, ARH, CI         VECTOR THROUGH DROM2
```

The first micro-instruction saves the most significant 16 bits of the immediate value (contained in MDR) in the Arithmetic Register High (ARH), starts the memory read operation for fetching the least significant 16 bits of the immediate value contained in the third halfword of the user instruction, and increments the contents of the Location Counter (LOC) and the Memory Address Register (MAR) by two. The second micro-instruction adds the least significant 16 bits of the immediate value (now contained in MDR) to the least significant 16 bits of the index value and saves the arithmetic carry in the carry Flag. The sum is stored in the Arithmetic Register Low (ARL). The second micro-instruction also specifies D2 in its Control field, so that control is transferred to the appropriate Execution routine

after the completion of the third micro-instruction. The third micro-instruction adds the most significant 16 bits of the immediate value (contained in ARH), the most significant 16 bits of the index value, and the carry from the previous addition. The sum is stored in the Arithmetic Register High (ARH).

RX Halfword Operand Fetch

If the current user instruction is an RX instruction and it requires only a halfword from memory (for the second operand), this routine is entered after vectoring through DROM1. The user instruction specifies the memory address for the second operand. The halfword located at the specified memory address is fetched and expanded to a 32 bit value by propagating the most significant bit through the high order bits. This fetch routine consists of the following four micro-instructions.

```
RXH     CA  MAR,LOC,MDR         CALCULATE EFFECTIVE ADDRESS OF THE
*                                SECOND OPERAND AND PLACE IT INTO MAR
*       L   MAR,LOC,MR          START MEMORY READ AND THEN COPY CON-
*                                TENTS OF LOC INTO MAR
        L   ARL,MDR,D2          (ARH,ARL)== 32 BIT SECOND
        A   ARH,NULL,SIGN       OPERAND VALUE;VECTOR THROUGH DROM2
```

The first micro-instruction is a very powerful micro-instruction. This micro-instruction examines the most significant two bits of the second halfword of the user instruction, and determines which one of the three RX formats has been specified. The effective address of the second operand is then loaded into MAR as follows:

RX1 FORMAT: (MAR)←INDEX VALUE (BITS 12:31) + 14 BIT ABSOLUTE VALUE IN MDR (BITS 6:19)

RX2 FORMAT: (MAR)←INDEX VALUE (BITS 12:31) + CONTENTS OF LOCATION COUNTER + 15 BIT TWO'S COMPLEMENT NUMBER IN MDR (BITS 5:19)

RX3 FORMAT: (MAR)←FIRST INDEX VALUE (BITS 12:31) + SECOND INDEX VALUE (BITS 12:31) + 20 BIT ADDRESS SPECIFIED BY USER INSTRUCTION (BITS 28:47)

If the user instruction specifies RX3 format, the Calculate Address (CA) micro-instruction also fetches the third halfword, and increments MAR and LOC by two.

The second micro-instruction starts a memory read operation for fetching the halfword located at the effective address, and then copies the contents of the updated Location Counter (LOC) into the Memory Address Register (MAR). The third micro-instruction loads the ARL with the contents of the halfword located at the specified address. This micro-instruction also specifies a D2 control operation so that the appropriate execution routine is entered after the completion of the fourth micro-instruction. The fourth micro-instruction loads the ARH with the most significant 16 bits of the expanded second operand value.

RX Fullword Operand Fetch

If the current user instruction is an RX instruction and it requires a fullword from memory, this routine is entered after vectoring through DROM1. This routine consists of the following five micro-instructions.

```
RXF     CA  MAR, LOC, MDR       (MAR) = EFFECTIVE ADDRESS OF SECOND
*                               OPERAND
*
        L   NULL, NULL, MR2     START MEMORY READ AND INCR MAR BY TWO
        L   ARH, MDR, MR        (ARH) = MS 16 BITS OF SECOND OPERAND;
*                               START MEMORY READ OPERATION
*
        L   MAR, LOC, D2        (MAR) = (LOC); VECTOR THROUGH DROM2
        L   ARL, MDR            (ARL) = LS 16 BITS OF SECOND OPERAND
```

The first micro-instruction loads the effective second operand address into MAR. The second micro-instruction starts the memory read operation (for fetching the most significant 16 bits of the second operand) and increments MAR by two. The third micro-instruction loads the most significant 16 bits of the second operand into the ARH and starts the memory read operation for fetching the least significant 16 bits. The fourth micro-instruction copies the updated Location Counter (LOC) into the Memory Address Register and specifies a D2 control operation. The fifth micro-instruction loads the ARL with the least significant 16 bits of the second operand. After the completion of the last micro-instruction control is transferred to the appropriate Execution routine.

3. Execution

Most arithmetic and logic user instructions require two micro-instruction execution routines. The execution routine for a normal arithmetic or logic user instruction assumes that the first operand is contained in a General Register specified by the YD field of the Instruction Register (IR). It also assumes that the second operand value has been loaded into the

Arithmetic Register (ARH, ARL), and the updated Location Counter (LOC) value has been copied into MAR. If the current user instruction is an RR or SF instruction, the Execution routine is entered from DROM1. If the current user instruction is an RI1, RI2, or RX instruction, the Execution routine is normally entered from DROM2. The following two micro-instructions form the Execution routine for the Fixed Point Add Operation. This routine is used by AR, A, AH, AI, and AHI user instructions. (This routine is also used by Halfword mode AHR, AH, and AHI instructions.)

```
A       A   YDL, YDL, ARL, CO+F+IRJ   (R1) = (R1) + (ARH, ARL);

        A   YDH, YDH, ARH, CO+CI+F     FETCH NEXT INSTR. AND SET CONDITION
*                                      CODE
```

The first micro-instruction adds the least significant 16 bits of the second operand to the least significant 16 bits of the first operand, and deposits the 16 bit sum into the least significant 16 bits of the General Register specified by the YD field. This micro-instruction also saves the arithmetic Carry In (CI) the Carry flag, modifies the G, L and V flags to reflect the result of the addition and initiates the instruction fetch for the next user instruction. The modified flag register is copied to the Condition Code.

The second micro-instruction adds the most significant 16 bits of the second operand to the most significant 16 bits of the first operand. The Carry flag is added with the least significant bit of the sum and the result is loaded into the upper half of the General Register specified

by the YD field. The Arithmetic carry produced by the add operation is saved in the Carry flag, the G and L are adjusted to reflect the algebraic value of the result, and the V flag is adjusted to reflect the overflow condition. Since the hardware provides a cumulative flag affect to facilitate multiprecision operations (refer to Section 4.3.3), the Flag Register, at completion of the second micro-instruction, reflects the result of the 32 bit add operation. The contents of the Flag Register, at the conclusion of the second micro-instruction is copied into the user Condition Code (if the Processor is in Halfword mode, the second micro-instruction does not modify the Condition Code).

After the execution of the second micro-instruction LOC and MAR are incremented by two, Flag Register is cleared and control is transferred to 'START' (at address X'001'). Now the same emulation process is repeated for the next user instruction.

The execution routines for other Fixed Point Arithmetic and Logical Operations are similar and they can be understood from the micro-program listing (refer to 7/32 C micro-program listing 05-063A13 and 7/16 with HSALU micro-program listing 05-051A13).

4.4.2 System Initialization. On power up, or following initialize, when the System Clear signal (SCLR) goes high, the Processor starts executing micro-instructions. The system clear signal forces the ROM Address Register to X'100' (see Figure 3 for flow chart of the System Initialization Routine).

The micro-program addresses the Loader Storage Unit (LSU) (Device Number 5). If false sync does not occur (LSU is present), the micro-program branches to routine 'LSU' otherwise normal power up operation is performed by the micro-program.

The PSW Save Pointer is fetched from location X'84' and saved in MR0. The Register Save Pointer is fetched from location '86', and both the register sets (Set 0 and Set 'F') are loaded from the memory area (of 128 bytes) pointed to by this pointer. If the Double Precision Floating Point option is equipped, the Double and Single Precision hardware registers are restored from their main memory save areas.

The Program Status and the Location Counter are restored from the memory area (of eight bytes) pointed to by the PSW Save Pointer. The micro-program examines the old console status (saved in location X'29' by the CONSER routine before powerfail or initialize). If the Console is not in the Run mode or the Processor is not equipped with Auto-Restart, a branch is taken to routine LOCDIS, (shown in Figure 5). If the Console is in the Run mode and the Processor is equipped with Auto-Restart, the Machine Malfunction Enable bit (PSW Bit 18) is tested. If this bit is set, a branch is taken to MMFINT routine, otherwise the Wait bit (PSW Bit 16) is tested. If the Wait bit is set, routine WAIT is entered. If the Wait bit is reset, the Wait indicator is cleared and the user instruction pointed to by LOC is executed.

Routine LSU is entered from the System Initialize routine (PWRUP) if false sync does not occur when the Loader Storage Unit (LSU) (Device Number 5) is addressed. The micro-program clears the most significant 16 bits of the Program Status, reads in two bytes from the LSU and loads them into the least significant 16 bits of the Program Status. The LSU routine reads in a 16 bit new LOC value, a 16 bit starting memory address, and a 16 bit ending memory address. The difference between the ending address and the starting address is formed in MR1. If the starting address is greater than the ending address, routine IDLE is entered. If the starting address is less than or equal to the ending address, data bytes are read from the LSU and stored in consecutive byte locations in main memory. When a data byte has been loaded into the memory location corresponding to the ending address, PSW Bit 16 is examined. If PSW Bit 16 is set, the interruptable Wait loop is entered, otherwise the user instruction addressed by LOC is executed.

4.4.3 Interrupt System. During user instruction fetch, the hardware tests for interrupts. If any of the tested interrupts (PPF, MALF, MAC, ATN, or CATN) are active routine HELP is entered. Routine HELP determines the nature of the interrupt, and branches to the appropriate interrupt processing routine. See Figure 4 for the interrupt support routines.

4.4.3.1 Primary Power Fail. Routine PWRDWN is entered if the Primary Power Fail signal is active. Current Program Status and Location Counter are saved in the PSW save area (pointed to by the PSW Save Pointer) and the General Registers of both register sets (Set 0 and Set 'F') are saved in the Register Save area (pointed to by the Register Save Pointer). If equipped, the Single and Double Precision Floating Point registers are saved in their power fail save locations. The Command Power Down micro-instruction (C POW) is performed which stops the Processor and closes the Initialize relay.

4.4.3.2 Machine Malfunction Interrupt. Machine Malfunction (MALF) can be caused by Memory Parity Error or Early Power Fail if PSW Bit 18 is set, or by Primary Power Fail (PPF). If MALF is active and PPF is not active, routine MMFINT is entered. This interrupt routine saves the Current Program Status and Location Counter in memory locations '20' to '27'. The new Program Status and Location Counter values are loaded from the locations '38' to '3F'. This Routine copies the contents of the Alarm Register (ALRM) to the Flag Register (FLR). If the Machine Malfunction occurred during the Auto-Driver Channel operation, the C flag is set by the micro-program. Routine TWAIT is then entered. If PSW Bit 16 is reset, the next user instruction is executed. If PSW Bit 16 is set, the interruptable Wait loop is entered.

4.4.3.3 Memory Access Controller Interrupt (MACINT). This interrupt routine is entered from HELP routine, if the Memory Access Controller interrupt is active and PSW Bit 21 is set. The Memory Address Register (MAR) is loaded with the constant '90', the Utility flip-flop is cleared, and the Common Interrupt routine (COMINT) is entered.

4.4.3.4 Arithmetic Fault Routine. This routine is entered when a fixed point or floating point fault occurs. If this routine is entered as a result of the floating point fault, the register MR0 contains eight, otherwise MR0 contains zero. This routine examines PSW Bit 19. If Bit 19 is set, the MAR is loaded with address '48', the Utility flip-flop is set, and the Common Interrupt routine (COMINT) is entered. If Bit 19 of the PSW is reset, the user instruction addressed by the Location Counter is executed.

4.4.3.5 Illegal Instruction Interrupt (ILLEG). If the current user instruction specifies an illegal operation code or if a privileged user instruction is executed in the protect mode (PSW Bit 23 set), this routine is entered. This routine decrements the LOC value by two if the instruction format is RR or or four if the instruction format is not RR or SF, loads the MAR with the address '30', clears the Utility flip-flop and transfers control to the Common Interrupt routine (COMINT).

4.4.3.6 Queue Interrupt (QUEINT). This routine is entered after the execution of a LPSW, LPSWR or EPSR user instruction if PSW Bit 22 is set. The routine examines the system queue. If the system queue is empty, routine TWAIT is entered. If the system queue contains any entries, the queue interrupt is taken. The Memory Address Register (MAR) is loaded with '88'; the queue address is saved in Register 13 (of Set 0), the Utility flip-flop is cleared, and a branch is taken to the Common Interrupt routine (COMINT).

4.4.3.7 Common Interrupt Routine (COMINT). The Program Status and the Location Counter values are saved in Registers 14 and 15 of Set 0. The new values of the Program Status and Location Counter are loaded from the eight byte memory area pointed to by the contents of the MAR. If the Utility flip-flop is set, the least significant four bits of MR0 are copied into the Condition Code, and routine TWAIT is entered.

4.4.3.8 Routine TWAIT. Most interrupt routines enter TWAIT after performing the PSW swap. If PSW Bit 16 is reset, the next user instruction is fetched. If PSW Bit 16 is set, the WAIT indicator is set and CATN signal is examined. If the CATN signal is active, the Console Service routine (CONSER) is entered otherwise an interruptable Wait loop (WAIT) is executed. If ATN, PPF, MALF, or CATN becomes active, the Wait loop is exited. If SNGL is active, one user instruction is executed otherwise routine HELP is entered to determine the exact nature of the interrupt.

4.4.3.9 I/O Interrupt. If none of the PPF, MALF, or MAC interrupt signals are active, the microprogram tests for I/O Attention (ATN). If ATN is active and PSW Bit 17 is set, routine AUTI0 is entered for performing Automatic I/O. The detailed flow chart of the Automatic I/O routine (AUTI0) is shown in Figure 6.

4.4.4 Console Support. The Hexadecimal Display Panel is serviced by routine CONSER. Routine CONSER is entered from HELP routine if CATN or SNGL is active and none of the higher priority interrupts (PPF, MALF, MAC or I/O interrupts) are pending. The detailed flow chart of the Console Support routine (CONSER) is shown in Figure 5.

4.4.5 Floating Point Instructions. If the processor is not equipped with the hardware Floating Point option, the Floating Point instructions are emulated by microcode. This section describes the microprogram implementation of the Floating Point instructions. The 'load' routine normalizes an unnormalized number but all other micro-routines (except 'float') assume normalized floading point operands and produce normalized results (except FIX). The R1 (and R2 for an RR Floating Point instruction) field of the user instruction must specify an even floating point register. If an odd floating point register is specified, the result obtained is incorrect. All floating point registers require two halfwords in reserve memory area. The addresses of the first and second halfwords of the n^{th} floating point register are calculated as follows:

Address of first halfword = 2*n

Address of second halfword = 2*n+2

In floating point arithmetic micro-routines, sign and magnitude processing is used, where the signs are stripped off and processed separately. The basic arithmetic processes positive operands and produces positive results (the fraction part of a floating point number is always in the true form).

If underflow occurs, a zero result (all bits zero) is generated; if overflow occurs the largest possible magnitude (all bits one) is generated.

The detailed flow charts of LME, STME, STE, LE, LER, AE, AER, SE, and SER instructions are shown in Figure 7.

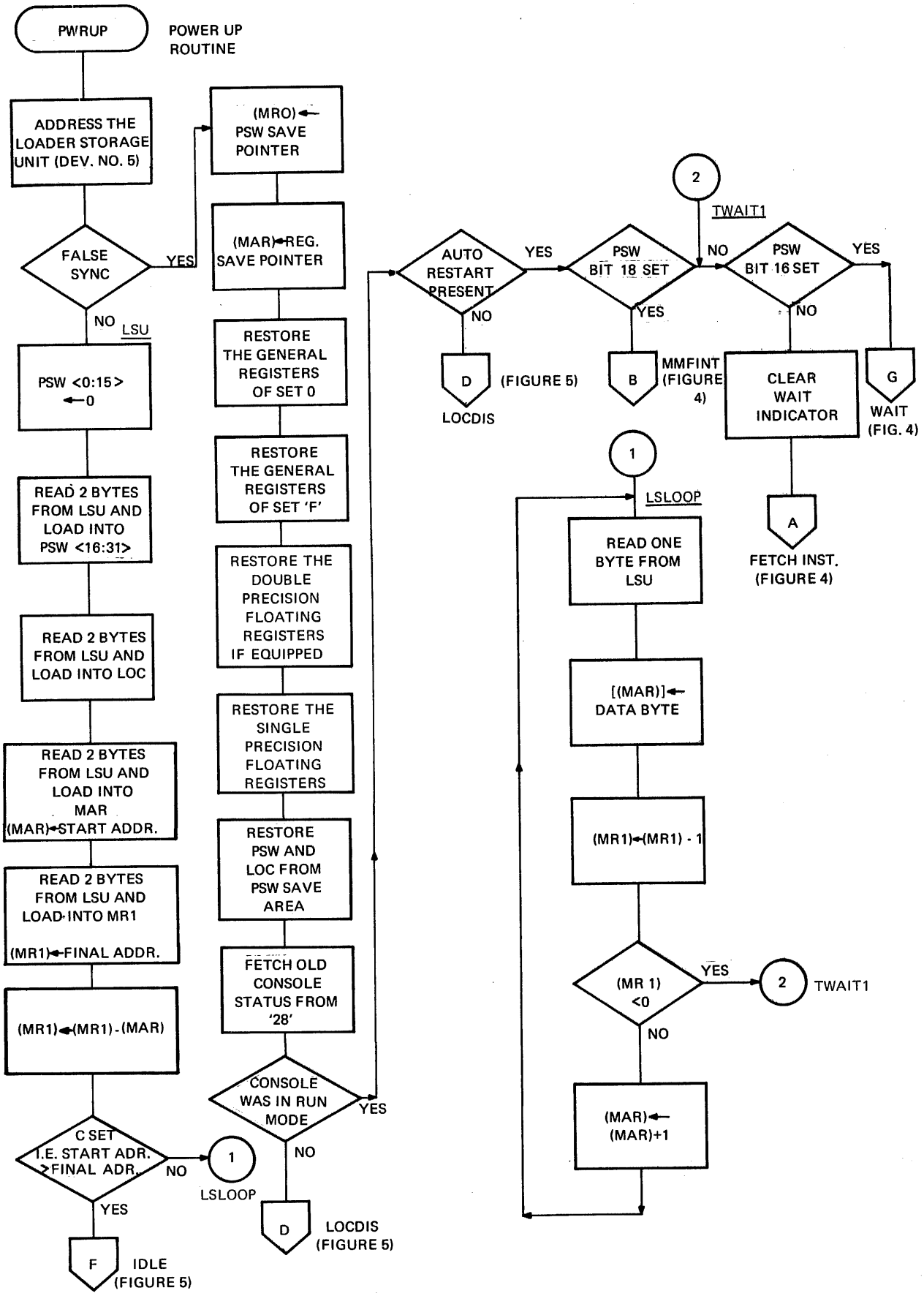


Figure 3. System Initialization

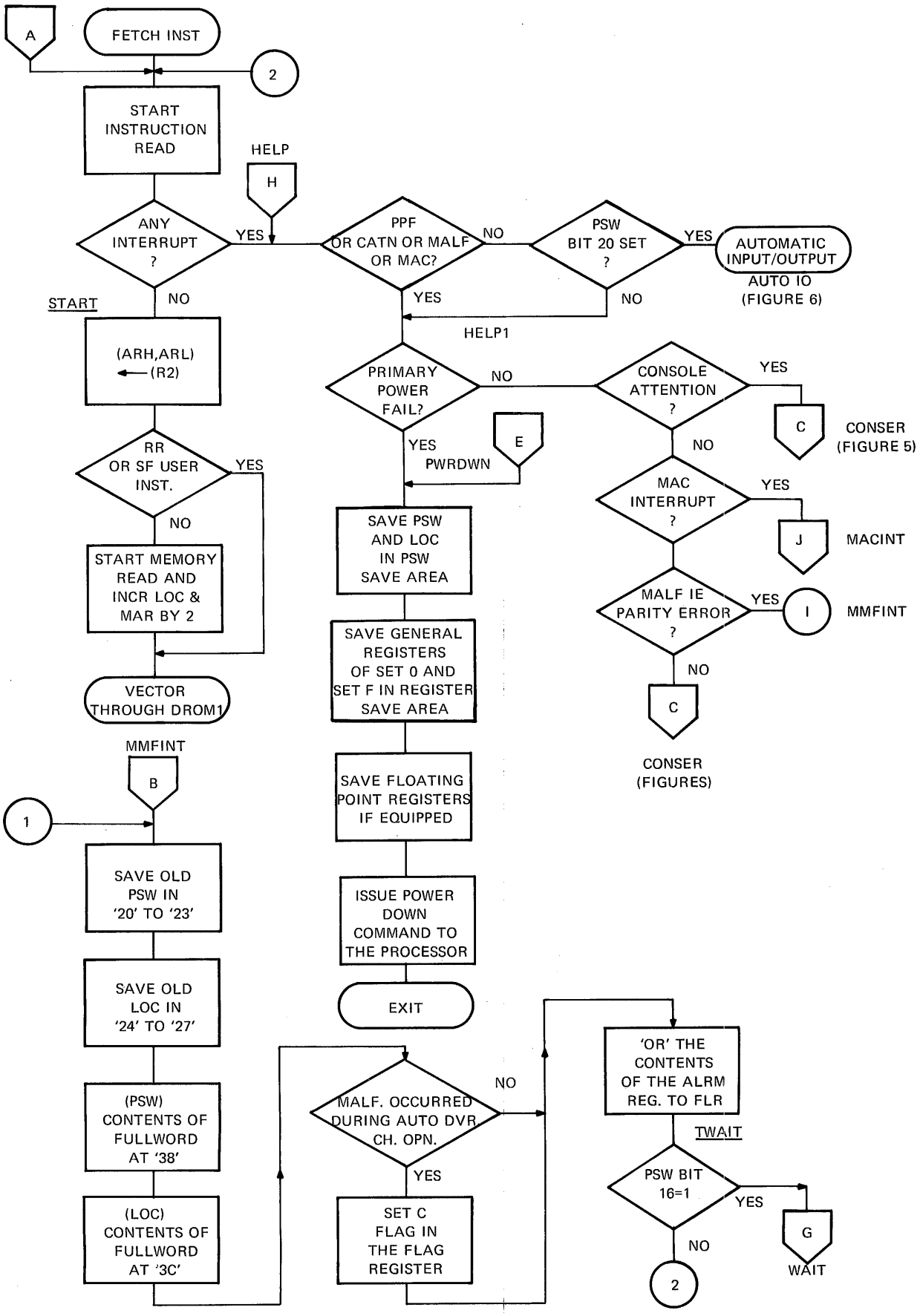


Figure 4. Interrupt Support

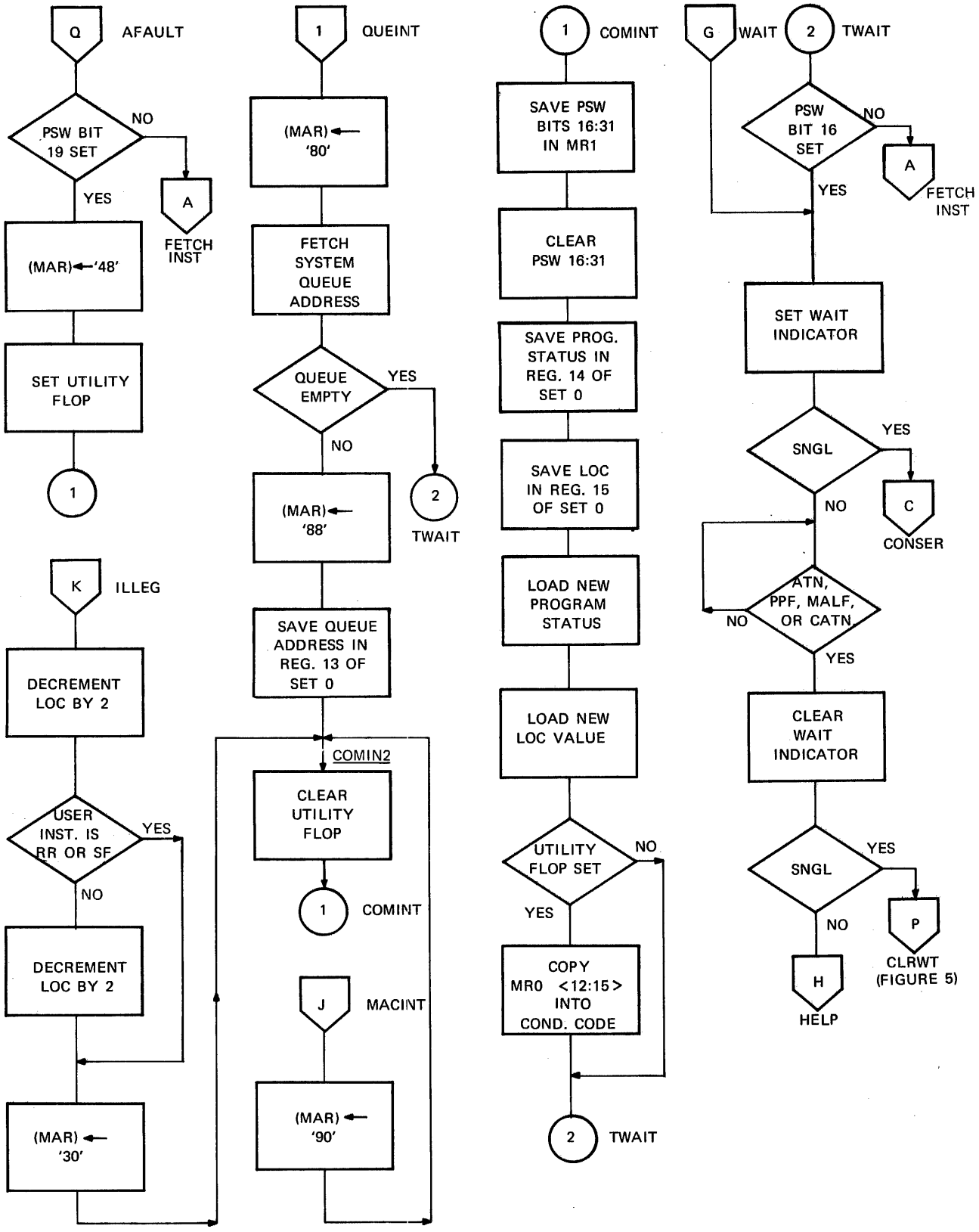


Figure 4. Interrupt Support (Continued)

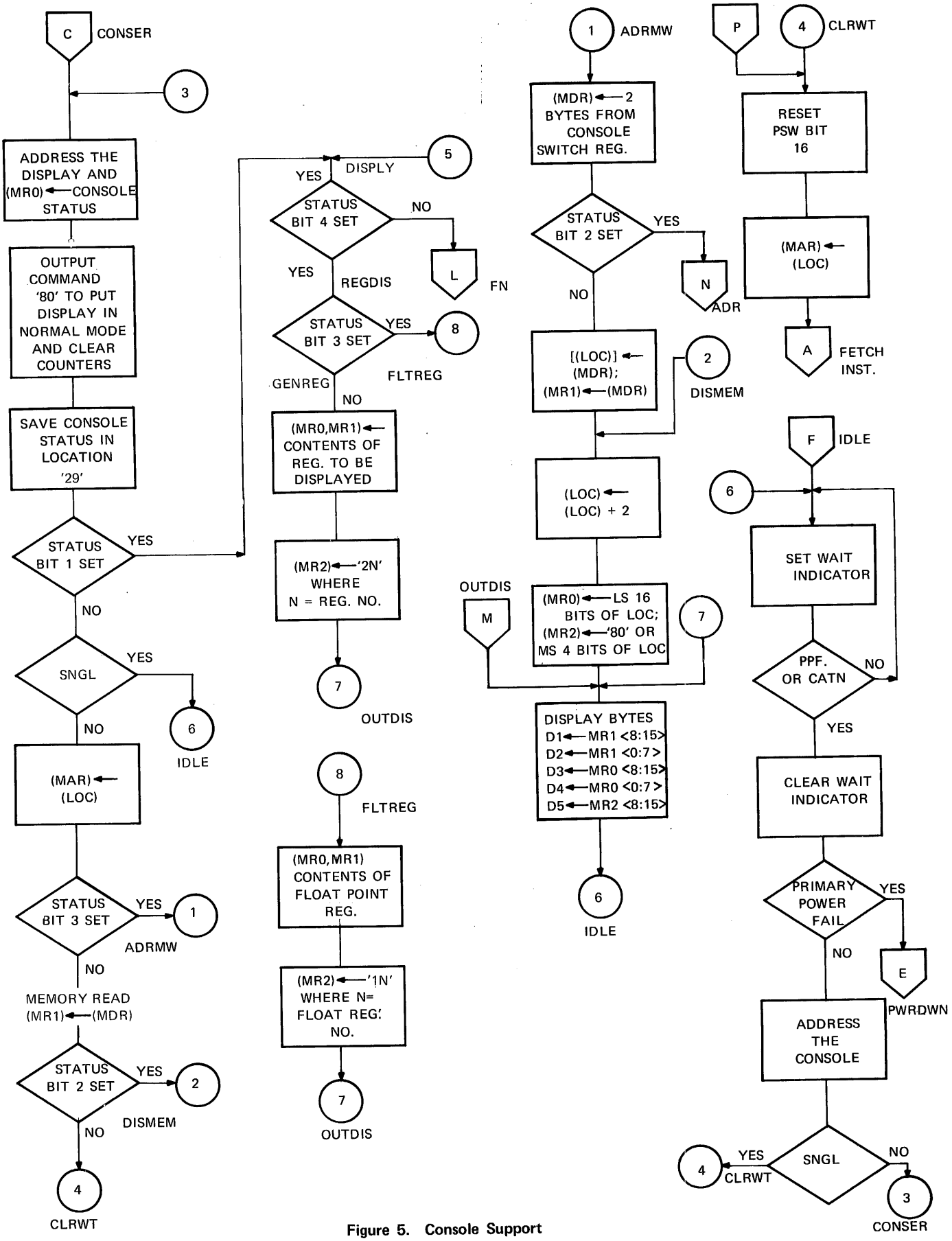


Figure 5. Console Support

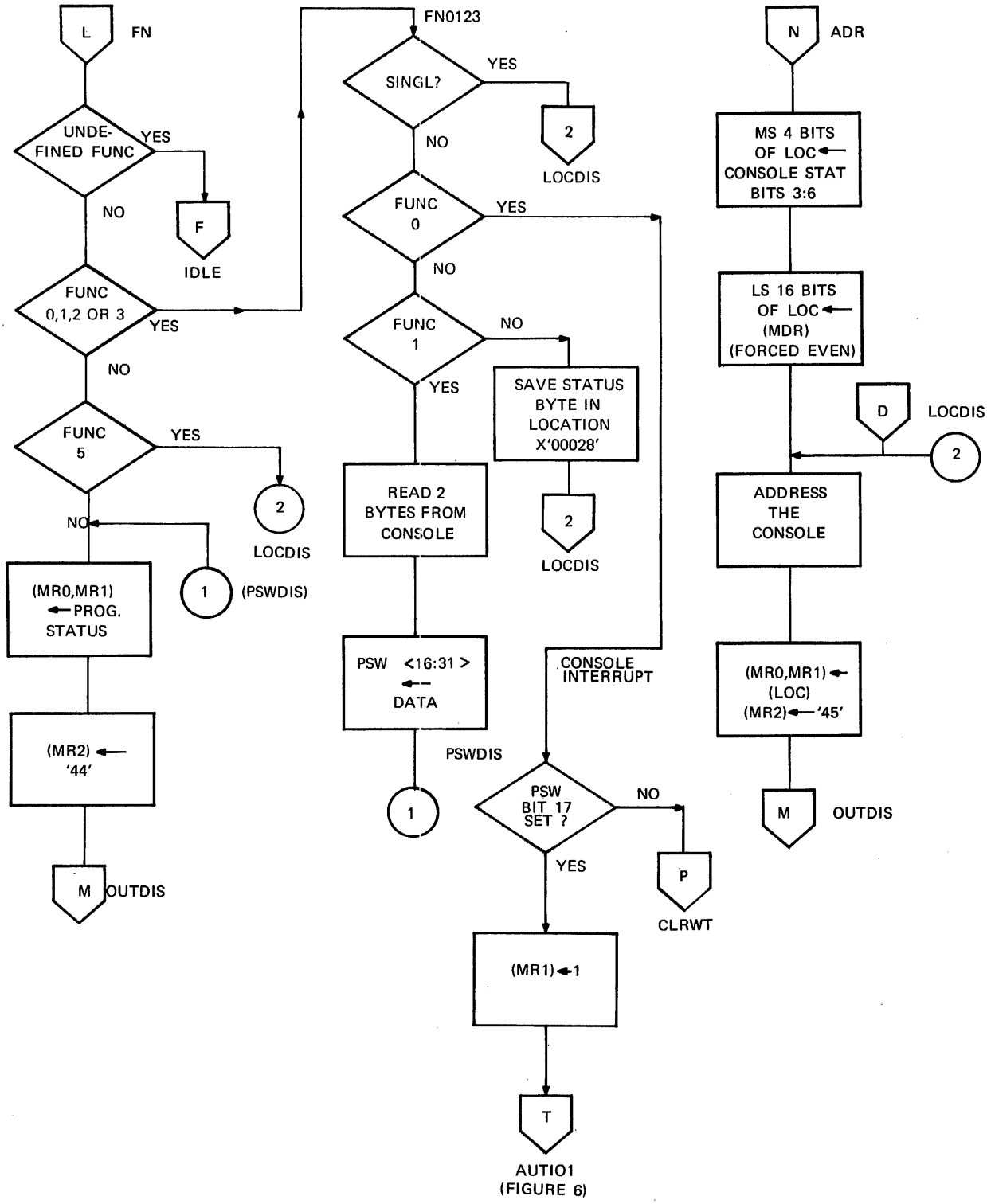


Figure 5. Console Support (Continued)

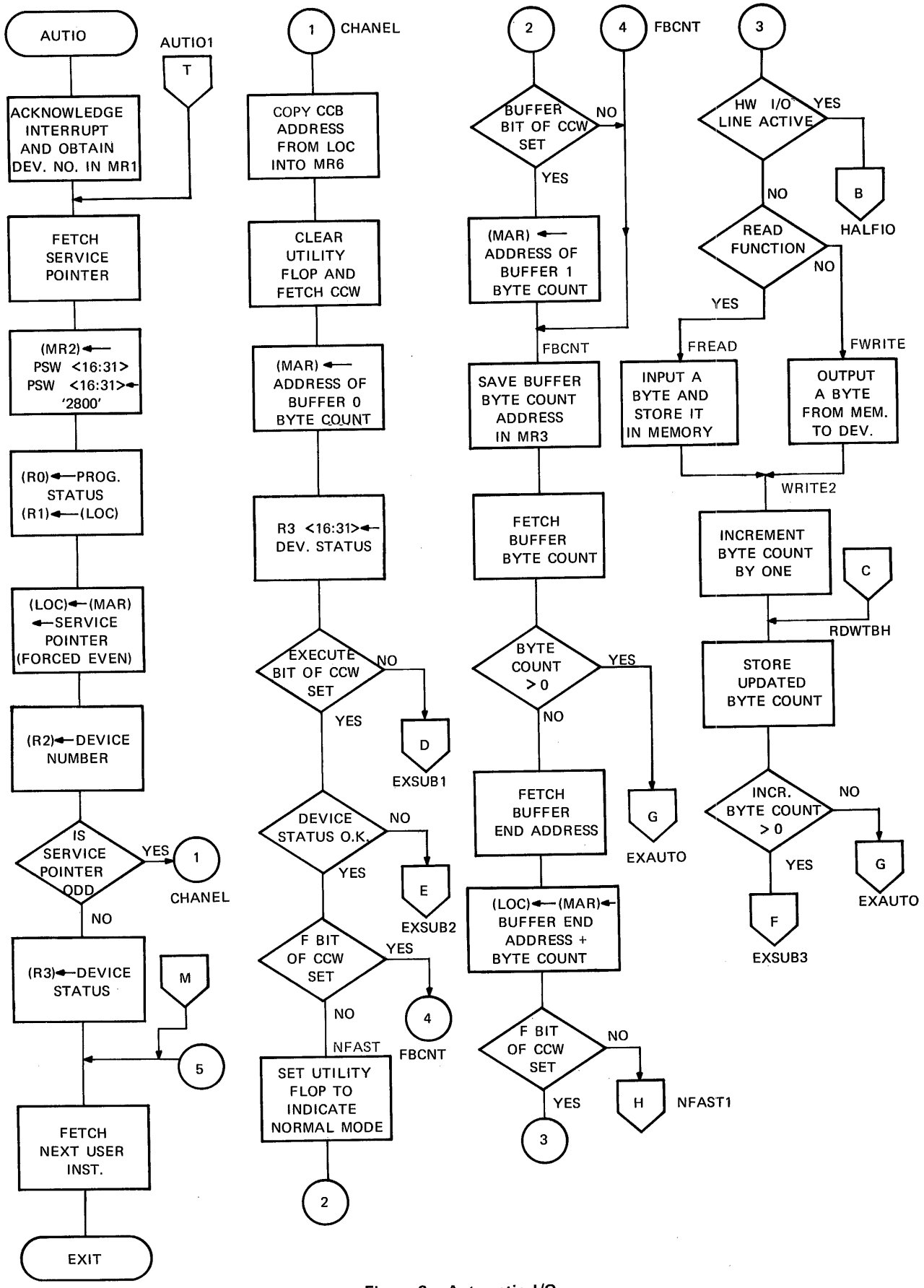


Figure 6. Automatic I/O

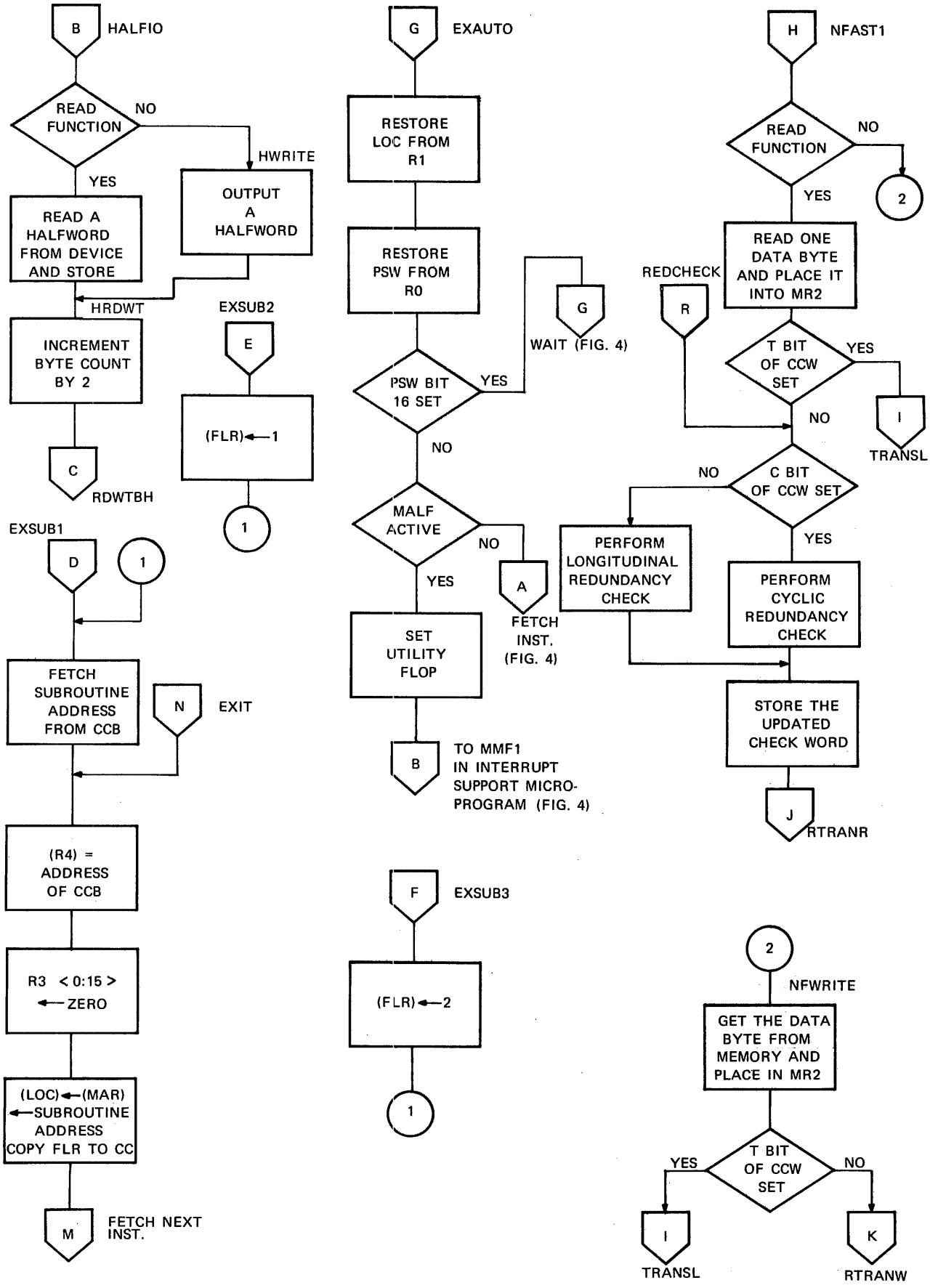


Figure 6. Automatic I/O (Continued)

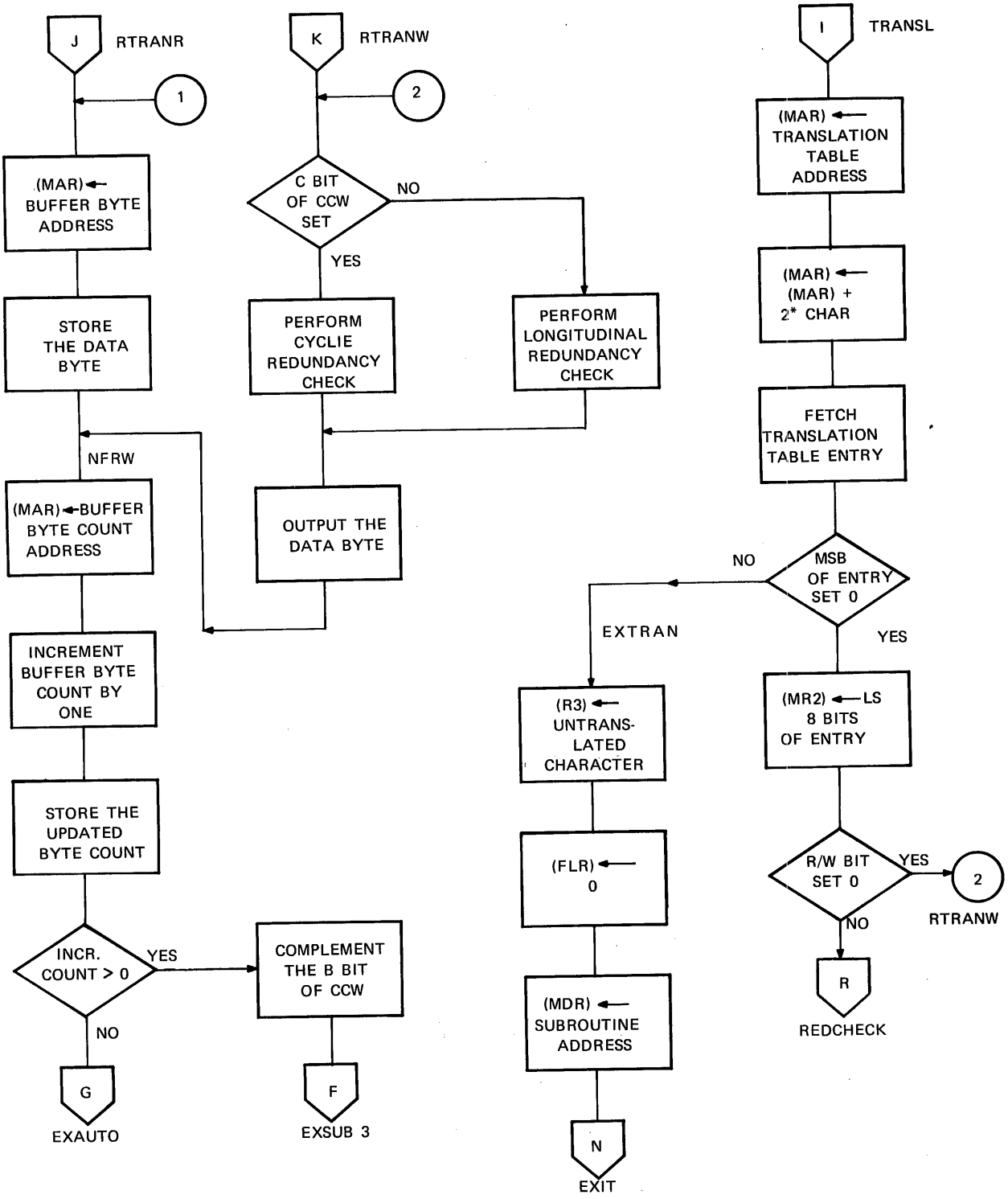


Figure 6. Automatic I/O (Continued)

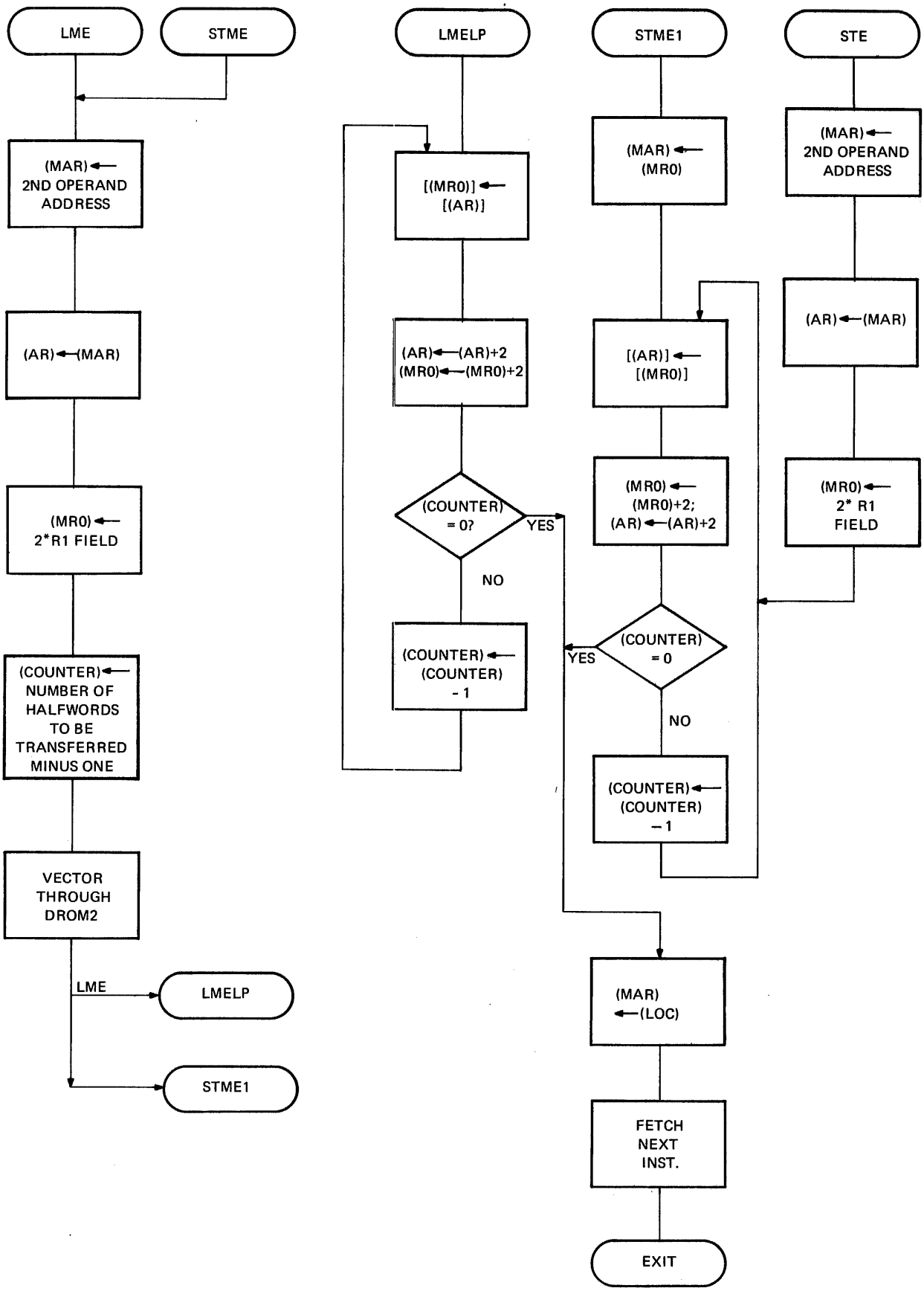


Figure 7. Floating Point Instructions

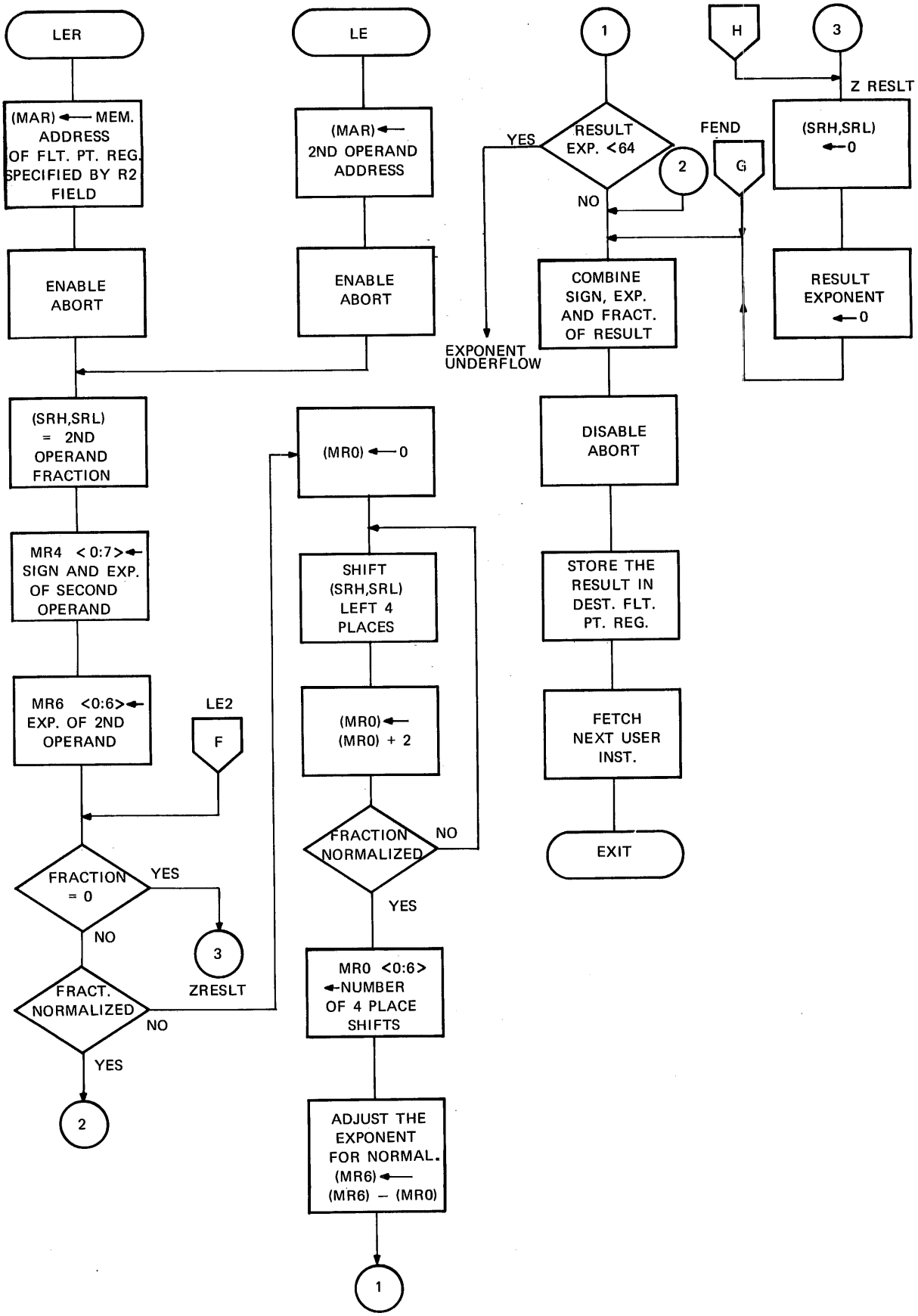


Figure 7. Floating Point Instructions (Continued)

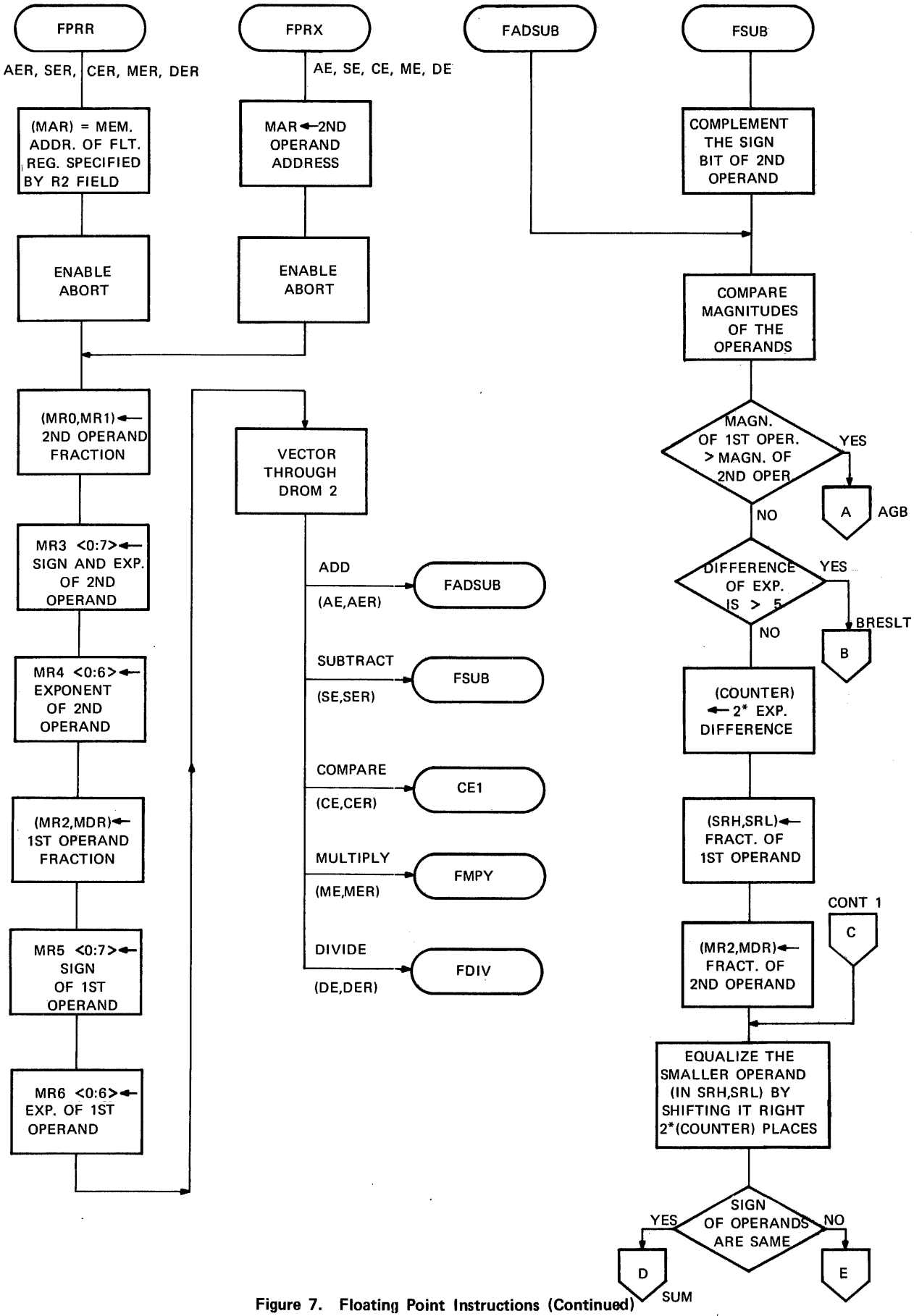


Figure 7. Floating Point Instructions (Continued)

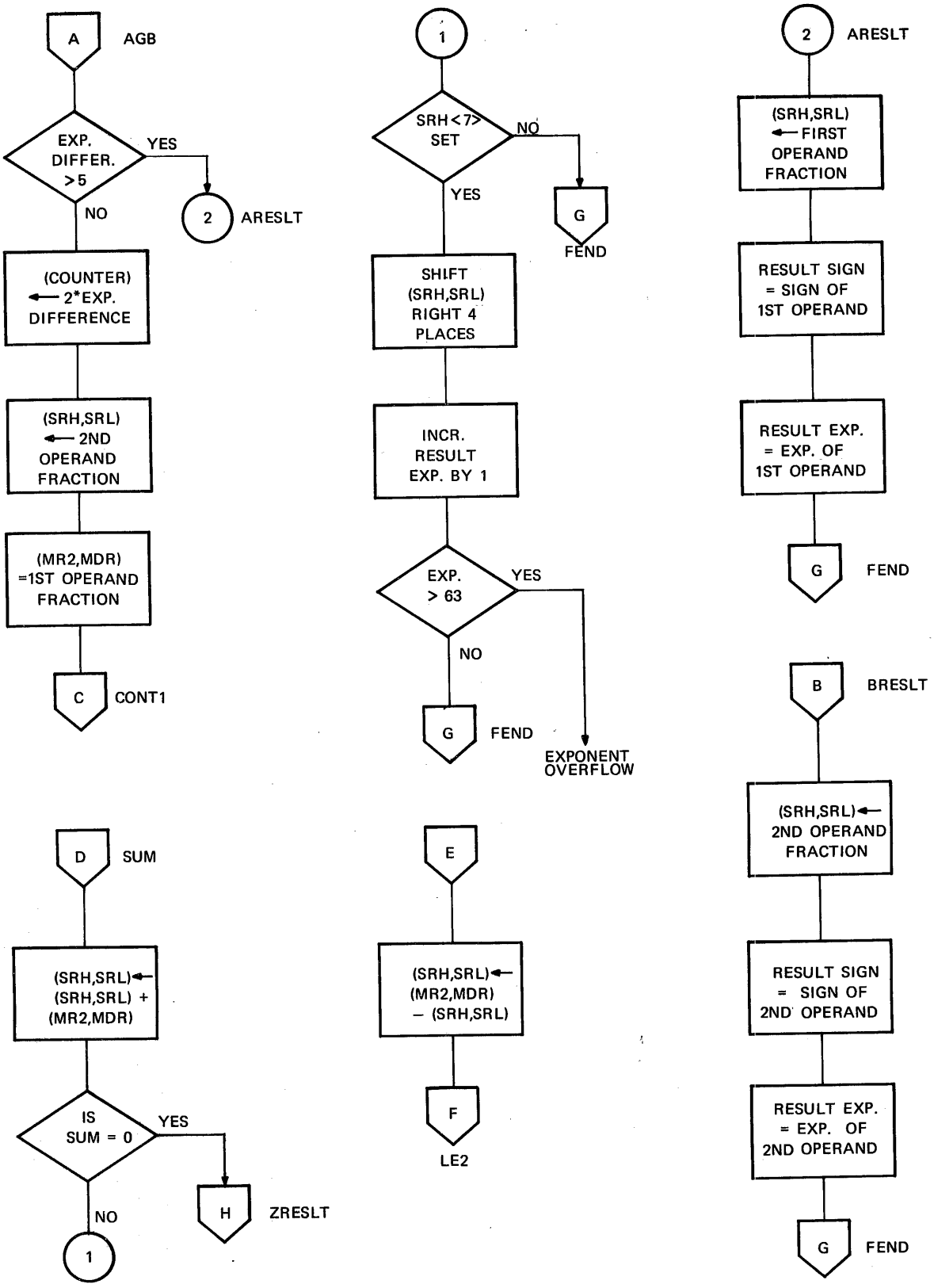


Figure 7. Floating Point Instructions (Continued)

5. FUNCTIONAL DIAGRAM ANALYSIS

5.1 Introduction

This section relates to Functional Schematic 01-079D08, Sheets 4 through 36. Note that in INTERDATA functional schematics, the last character in the mnemonic symbol designates the logic level when the signal is active. For example; D050 is Data Line Number 5 (D05). The last character (0) indicates that when D050 is active, the line is at a logical zero level. Refer to the General Description section of this manual for further information concerning the INTERDATA documentation system.

5.2 Clock Control

The Clock Generator is shown on Sheet 32. The clock system employs a free running 16 MHz oscillator. The oscillator output is inverted to generate OSC0. The oscillator is adjustable (via the variable Capacitor C1), over the range of 55 to 120 nanoseconds.

OSC0 is used as the clock inputs to a pair of flip-flops arranged as a two bit counter. The outputs from this counter are ANDed to form the **Clock signal** (CLK1, CLK1A, CLK1B, and CLK1C). These clocks, hereafter, are referred to as CLK1. CLK1 is the basic clock of the Models 7/16 HSALU and 7/32 C. Another clock, FA1FB00, is decoded from the counter and is used primarily for controlling the enables to the DROMs and the loading of the ROM Address Register. The counter is initialized and held in this state by STOP0, on a power down or a power up, to inhibit the clocks. Refer to Figure 8 for clock timing.

The clock control logic of these Processors is shown on Sheet 33. Clock inputs to most flip-flop or registers are derived from CLK1 and are delayed from CLK1 by one and only one TTL gate delay. The clock system in the Processor is controller by clock stops. These stops prevent various functions from being performed within the machine at a given time.

Memory Stop (MSTOP0) and Input/Output Stop (ISTOP0) are the two clock stops in the Processor which inhibits all clocks in the machine. The clocks are stopped when the Processor is waiting for data from the memory or when waiting for memory to become available to begin a new memory operation. When MSTOP0 becomes active it halts all activity except the current memory operation. Likewise, during an I/O operation, when ISTOP0 is active, all clocks are inhibited until the current **I/O operation is complete.** In the case where both a memory operation and an I/O operation is specified by the same **micro-instruction, the** hierarchy of stops is **as follows; first any** previous memory operations must be completed, the I/O operation specified by the instruction is then executed, finally, upon completion of the I/O operation, the memory operation specified is started.

ROM Stop (RSTOP0) is used to prevent both incrementing the ROM Address Register and loading the ROM Data Register. This stop is activaetd by MSTOP0, ISTOP0, SKIP0, and SPSTOP0. MSTOP0 and ISTOP0 were discussed previous. SKIP0 is active during the first clock of any True Branch operation **(Figure 9)**, and SRSTOP0 is active on any Counter operation when the value in the counter is greater than one (refer to Section 5).

The Destination Stop (DSTOP0), when active, prevents loading any destination register. DSTOP0 is active when MSTOP0, ISTOP0, BRCH0, or SDSTOP0 is active. MSTOP0 and ISTOP0 were discussed previously. BRCH0 is active during any Branch operation whether or not the branch is taken and SDSTOP0 is active on any command mode operation when the Repeat flip-flop is reset (34M6). Refer to **Section 5.12 for Command Mode operations.**

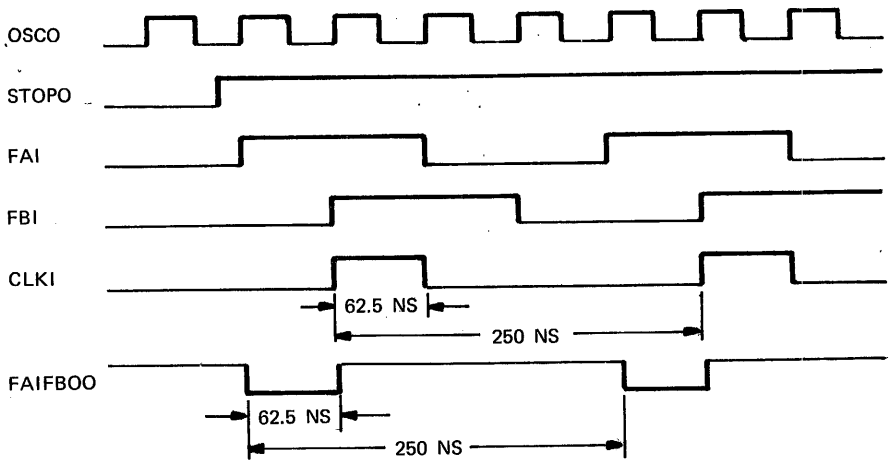


Figure 8. Nominal Clock Timing

5.3 Initialize Control

System initialization is performed by de-energizing the System Clear (SCLR) relay (32A4). This relay is de-energized as a result of one of the following conditions.

1. Placing the Processor ON-OFF-LOCK Switch in the OFF position.
2. Operating the Processor Initialize key.
3. Activating PFDT0 by the watchdog timer feature of the optional Loader Storage Unit (LSU) or other external source.
4. Activating PFDT0 from the optional Primary Power Fail (PPF) detection if the AC input level falls below a minimum operating level.
5. Loss of either +5VDC or +15VDC from the Processor power supply.

The SCLR function provides an orderly shut down of the Processor as well as a reset signal to both the memory and the Multiplexor Bus. On a power up, the SCLR relay remains deactivated until all DC voltages are in regulation. This assures predictable initial states of latched functions.

An Early Power Fail (EPF) indication is provided to the user program if Bit 2 of the PSW is set, (Bit 18 on the 7/32 C). This indication is provided by the micro-program by means of a machine malfunction interrupt swap.

Upon receipt of a power down indicator, PFDT0 (32C7) active, by the hardware, the one millisecond timer (32G7) is triggered. The leading edge of this pulse sets the Early Power Fail flip-flop (EPF) (32H5) which in turn enables, if PSW181 is set, a branch on machine malfunction to be taken by the micro-program. In the machine malfunction interrupt swap routine, the micro-program issues a Command Jam Alarm register (JALRM1) (34E8) active, which direct sets the Alarm flip-flop (28E8). The one output of this flip-flop is ANDed with Load PSW Low (LPSWL1) which causes the less than flag of the new PSW to be active following the machine malfunction interrupt swap. On the trailing edge of the one millisecond timer, the Power Fail (PF) flip-flop (32H7) becomes set, initiating a power down sequence.

The optional Primary Power Fail Detector (Sheet 12) monitors the AC input by sampling the secondaries of a 12VAC transformer, C1 and C3, from the Processor power supply. If the AC is lost or if the AC falls below a present level, PFDT0 and POWDN0 becomes active. PFDT0 initiates the power down sequence and POWDN0 provides a fast discharge path for Capacitors C5 and Cy which de-energizes the SCLR relay and holds the relay off in the event the AC is fluctuating about its preset power down level.

5.4 Read-Only-Memory

The Read-Only-Memory (ROM) is a high-speed, solid-state, non-destructive memory used to hold the micro-program. The ROM is organized into pages of 256 24-bit words. Each page of ROM contains six integrated circuit (IC) packages arranged such that each integrated circuit holds four-bits of each word on the associated page.

The Model 7/16 HSALU micro-program is complete in five ROM pages or 30 ROM integrated circuits. Seven additional ROM integrated circuits comprise the Decoder ROM (DROM). Seven pages of ROM are used in the Model 7/32 C using 42 ROM ICs, six Integrated Circuits for the DROM, and one IC for detection of illegal instructions (IDROM).

Each ROM integrated circuit has two enable leads. Both enables have to be low before a read-out is obtained. If the enables are false, the four data output leads are high. Address decoding is done internal to the IC.

5.4.1 Decoder Read-Only-Memory. The Decoder Read-Only-Memory (DROM) logic of the Model 7/16 HSALU and Model 7/32 C differ, refer to the strapping table for DROMs, Sheet 9. The DROM for these two machines are discussed in the following paragraphs.

The DROM for the Model 7/16 HSALU consist of several ROM integrated circuits shown on Sheet 5. Each IC contains 256 four bit words. The DROM is address by the outputs of the operation code (op-code) field of the Instruction Register (IR). Each of the 256 possible bit combinations in this op-code field address a unique word in the ROM. The DROM in the 7/16 HSALU is divided into two sections DROM1 and DROM2.

DROM1, enabled by FDEC10 (5A1), consists of four ROM ICs. The 11 least significant bits of the ROM chips labelled DROM1 (F) (5B5) are presented as inputs to the ROM Address Register (RAR) and represent an address in the micro-program of this machine. The most significant bit of this set indicates that a privileged instruction is decoded.

The two least significant bits of the ROM ICs labeled DROM1 (H) (5D5) are used to modify the control field of the next sequential instruction to be executed. Table 6 represents the bit meaning of these outputs. No other bits are used in DROM1 (H).

Table. 6.

Pin 11	Pin 12	Output Meaning
0	0	No Action
0	1	Memory Read and Increment
1	0	Instruction Read
1	1	Instruction Read and Jam CC

DROM2, enabled by FDEC20 (5E5) is used exclusively to modify the contents of the RAR and is accessed when the micro-program specifies D2 in the control field of the micro-instruction.

The Model 7/32 C has two separate DROMs, DROM1 and DROM2. These DROMs are addressed as discussed previously but the enabling of DROM1 is under control of the Illegal Instruction DROM (IDROM). DROM1 is enabled when D1 is specified by the control field of the current micro-instruction and if the IDROM has decoded a legal OP code in the Instruction Register (IR bits 0:7). The eleven least significant bits of all three DROM1 integrated circuits are presented as inputs to the RAR which becomes the address of a point in the micro-program where the processing of the decoded instruction type begins. The most significant bit of DROM1 indicates that the decoded instruction is a priviledged instruction. In addition, Bits 9, 13, 14, and 15 of the RAR inputs can be forced low for vectoring to unique locations in the micro-program.

On an Instruction Read, FINR1A active (9H5), with no interrupts pending, INIT1 (9J4) inactive, address X'001' is forced. An Instruction Read with an interrupt pending causes location X'045' to be accessed. If a user instruction is being aborted during the execution of the instruction, GABORT1 (9J4) is forced active and during the time of a D2 on Read Halfword or Write Halfword instructions if the device is in the Byte (eight-bit) transfer mode SRA140 is forced low.

5.4.2 ROM Address Register. The ROM Address Register (RAR) (Sheet 5) is an 11-bit register which is loaded from the false SRAXX0 bus. This bus contains the data from the DROM during a Decode micro-operation and the RD register during a Branch micro-operation. The eight least significant bits of this register are arranged as a counter so that sequential ROM addresses, in a given page, may be selected.

5.4.3 ROM Data Register. The contents of the ROM from the selected address are loaded into the ROM Data Register (RD) (Sheet 7) on the trailing edge of Clock RD (CKRD0). The RD is a 20-bit register which can be thought of as the micro-instruction register. Refer to the Micro-Program Description section of the specification for the micro-instruction word format.

The RD is initialized by SCLR on a power up to an X'F00100'. This is decoded as an unconditional branch to address X'100' which starts the micro-program execution at the specified location.

5.5 Processor Registers

The majority of instructions in the micro-program are concerned with moving data from one Processor register to another. This transfer takes place by way of the 16-bit B and S Busses and modification of the data, under control of the micro-program, is done by either the Arithmetic Logic Unit (ALU) or the Shifter. Most of the Processor registers are general purpose but a few of them perform special functions. Each register is described in the following paragraphs.

5.5.1 Memory Address Register and Memory Address Slave. The memory address function of these Processors is accomplished in two steps. First, the selected address is loaded by the micro-program into the Memory Address Register (MAR) and then, the hardware copies the contents of the MAR into the Memory Address Slave (MAS) at the beginning of a memory cycle and presents this address to the memory. The micro-program is then free to modify the contents of the MAR.

Both registers are 20-bit registers and are shown on Sheets 10 and 16 (only 16-bits are provided in the 7/16 HSALU). The MAR is loaded from the S Bus whenever either the MAR or the LOC is specified as a destination and its outputs are dumped onto the B Bus if MAR is decoded as a source register or are loaded into the MAS at the beginning of a memory cycle on the leading edge of LMAS0.

5.5.2 Memory Data Register. The Memory Data Register (MDR) is shown on Sheets 18 and 19. This register is divided into two parts MDR High and MDR Low and is located on the CPU-C board LO. On a memory read operation, the MDR is first direct cleared by either CLMDH0 or CLMDL0 and then each active bit from the Memory Data Lines (MD000:160) direct sets its corresponding bit in the MDR. The MDR may also be loaded from the S Bus when it is specified as a destination register by the micro-program. When loading from the S Bus, if Cross Shift is specified, only MDR High is loaded when Bit 15 of the MAR is set and only MDR Low is loaded when Bit 15 is reset.

The outputs of the MDR are presented to the memory during the write portion of a memory cycle, to the B Bus if MDR is a source register and, to the B inputs to the ALU when MDR is specified as the second source.

On the Model 7/32 C four additional bits of the MDR are provided, XMDR (9K7). This extention to the MDR is loaded from Bits 12:15 of the MDR during Phase two of a Calculated Address (CA) (Section 5) or when an Extended Read (ER) is specified by the micro-program.

5.5.3 Instruction Register. The Instruction Register (IR) is a 16-bit register which stores the user instruction presently being executed. The IR is divided into three parts or fields; OP code (Bits 0:7) YD field (Bits 8:11), and YS field (Bits 12:15). The IR is loaded from the Memory Data Bus, by the hardware, on an Instruction Read. **Refer to Figure 9 for timing information.**

The op code field (Sheet 9) contains the encoded instruction to be performed. Its outputs are decoded by the hardware and presented as address to the Decoder Read-Only-Memory. All 256 combinations have unique entry points in the micro-program.

The YD field is defined as the user destination field. YD selects one of the General Registers, in the Processor, in which the result of the user instruction is to be stored. This portion of the IR (Sheet 21) is arranged as an up/down counter. If YDP1 is specified as either the source or destination of a micro-instruction, the YD field of the IR is incremented by one at the end of the instruction. Likewise, if YDM1 is specified, YD is decremented by one.

YS is the user source field of the instruction being emulated. The second operand of the instruction is contained in the General Register specified by YS for RR format instructions. This field also contains the number of the General Register being used as the index register on an RX or an RS instruction or the actual hexadecimal number in a short form instruction. Refer to User's Manual, Publication Number 29-261 or Model 7/32 Reference Manual, Publication Number 29-399, for instruction format information.

The YS field of the IR can also be loaded from the S Bus by the micro-program if YSI is the selected destination register. The three fields of the IR can be selected separately as source registers by the micro-program.

5.5.4 Arithmetic Register. Two 16-bits Arithmetic Registers **(ARH and ARL) (Sheets 21 and** 22) are available to the micro-program to be used as second operand on the Add, Subtract, OR, AND, or Exclusive OR micro-instructions. These registers may be loaded from the S Bus when they are specified as the destination register of a micro-instruction. If AR is specified as the destination both ARH and ARL are loaded. Bits 0:11 of ARH are forced inactive and Bits 12:15 of ARH and Bits 0:15 of ARL loaded from the XS Bus and S Bus respectively. The output of the registers are presented to the 'B' inputs to the ALU when they are specified as the second source by the micro-instruction.

5.5.5 Flag Register and Condition Code. **The Flag Register (FLR) (Sheet 30) is a four bit re**gister which contains the Carry flag (C), the Overflow flag (V), the Greater than flag (G), and the Less than flag (L). The outputs from the FLR are copied into another four bits register, the Condition Code, at the end of each user instruction being emulated. These flags represent results of user instructions which cannot be indicated otherwise.

The FLR is loaded from the S Bus whenever either the FLR or the Program Status Word (PSW) register **is specified as a destination. The contents of FLR is copied into the Condition Code on an Instruction Read (see Figure 9) or on a command if JAM CC is specified. The outputs from the Flag Register** are also used by the Branch Circuit (Sheet 31) for conditional branches. The contents of the CC are copied onto the B **Bus (Bits 12:15)** when the PSW is specified as the source register.

The following conditions also modify the FLR:

1. Carry Flag - The C flag changes on any micro-instruction except Load I/O if carry out is specified. It sets if B Bus Bit 0 is set on a Shift Left, if B Bus Bit 15 is set on a Shift Right, if Carry Save (CSV1) from the ALU is set on an Add, or if CSV1 is inactive on a Subtract. For all other cases the C flag is reset.

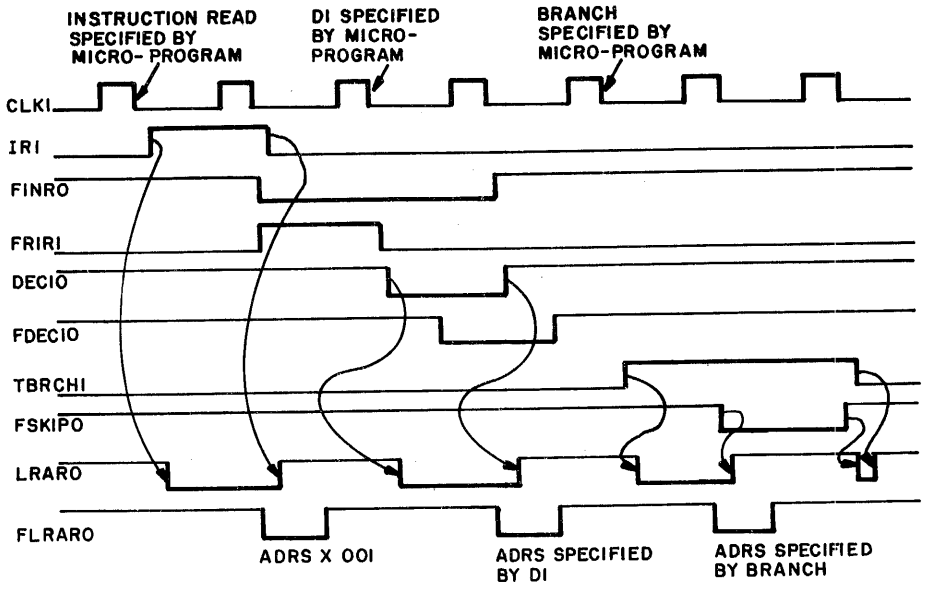


Figure 9. Micro-Program Decode and Branch Operations

2. Overflow Flag - The V flag is direct set if false sync is detected on an I/O operation and is changed on any micro-instruction except Branch, Command, or Load I/O if Flags (F) are specified. The V flag is set on an Add if the sign of the number of the B Bus is positive and the sign of the B Bus is the same as the sign of the A Bus (Arithmetic Register) and the resulting sign (S Bus) is negative or the number on the B Bus is negative and the sign of the B Bus is again the same as the sign of the A Bus and the result is positive. This flag is also set on a Subtract operation if the sign of the B Bus is positive and the signs of the B Bus and A Bus differ and the result sign is negative and the B and A bus signs differ and the result is positive. For all other combinations of A, B, and S Bus signs on Adds and Subtracts, the V flag becomes reset, The following Boolean expression also defines the setting of the V flag:

$$V = ADD \cdot B000 \cdot \overline{(B000 \oplus GA000)} \cdot S000$$

$$+ADD \cdot B0000 \cdot \overline{(B000 \oplus GA000)} \cdot \overline{S000}$$

$$+SUB \cdot \overline{B000} \cdot (B000 \oplus GA000) \cdot S000$$

$$+SUB \cdot B000 \cdot (B000 \oplus GA000) \cdot \overline{S000}$$

3. Greater than and Less than - These flags change on any micro-instruction except Branch Command or Load I/O as long as F is specified. The G flag is set if the result of the operation (S Bus) is positive or if the result is zero and either the G or L flag was set from a previous operation. The L flag is set if the resulting sign is negative. Either flag is reset if these conditions are not met.

5.5.6 Register Stacks. The register stacks in these machines are located on Sheets 12 and 13. Each IC used in these stacks are four bit by 16 word register files. Each stack has four select lines which are decoded internally to select one of 16 words. Associated with each IC are also two control leads Memory Enable (ME) and Write Enable (WE).

When the ME control line is at a low state, the outputs represent the contents of the selected word in the register file. During the time that the WE control line is active the selected register file is loaded from the S Bus. Each machine cycle is divided into a Read portion, READ1 active (11J3), and a Write portion, READ1 inactive. During the time that READ1 is inactive, data to the ALU is latched-up by the B Bus Shifter/Latch circuit (Section 5.6) to prevent changing the B Bus during the time that the outputs of the register stacks may be changing. Refer to Figure 10 for timing information.

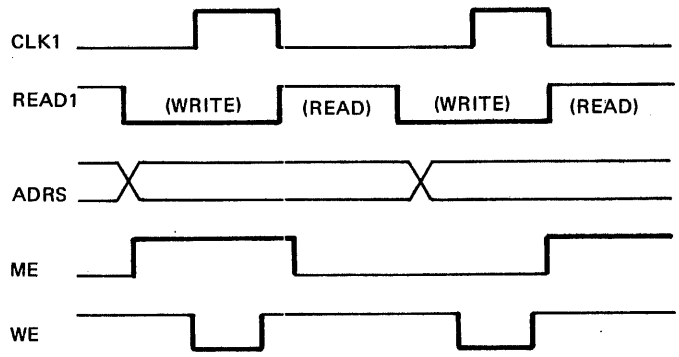


Figure 10. Register Stack Timing

The Model 7/16 HSALU uses eight register stack ICs in the register stack, four for the micro-registers MR0:6 and PSWL and four for the sixteen 16-bit General Registers. Twenty-two register files are used in the Model 7/32 C four for the micro-register and the remaining 18 for the two sets of 32 bit General Registers.

The Memory Enable logic for the register stacks is found on Sheet 11. The AND gate on the left half of each AND/OR gate is used for source decoding and the AND gate on the right hand side is used for destination decoding. ROM data bits are used to address micro-registers while the YS and YD fields of the Instruction Register (IR) is used for addressing the General Registers. In the 7/32 C, selection of General Register Set 0 or 'F' is under control of PSW Bit 27 (11F2).

5.6 Shifter and Latch

The Shifter/Latch circuit (Sheet 20) takes the data on the B Bus, manipulates that data and stores it (when READ1 is inactive) prior to presenting it to the A inputs of the ALU. The shifter can load, shift left, shift right, or cross shift the B Bus data. The function performed is determined by the state of the A and B inputs to the eight shifter ICs. A truth table defining these inputs is provided on Sheet 1A. The 19-073 ICs which comprise the shifter are tri-state devices. When the S inputs to the shifter are at a logical ZERO level, the chips are enabled and the specified function is performed. If these inputs are high, the outputs of the shifter are disabled and assume a high impedance state.

The cross coupled flip-flops at the output of each state of the shifter latch the data on the Gated B Bus (GB000:150) during the time that READ1 is inactive. This prevents the data, which may be changing on the B Bus at this time, from being felt at the inputs to the ALU.

5.7 Arithmetic Logic Unit (ALU)

The Arithmetic Logic Unit (ALU) consists of four 19-039 four-bit ALU packs and one 19-046 Carry Look-Ahead pack. The ALU is shown on Sheets 21 and 22. In the Model 7/32 C the ALU is extended to 20 bits for address calculations by additional ALU IC (10N3).

FUNCTION	M	S_0	S_1	S_2	S_3
LOAD	1	1	1	1	1
AND	1	0	1	1	1
OR	1	1	1	0	1
XOR	1	1	0	0	1
ADD	0	1	0	0	1
SUB	0	0	1	1	0
CMD	0	1	0	0	1

Each 19-038 ALU pack develops four-bits of the low active S Bus. The internal Carry Propagated (CP) from the most significant stage of the ALU pack and the Carry Generated (CG) for the most significant stage (CPXX1 and CGXX1) are applied to the 19-040 Carry Look-Ahead pack to develop the Carry into the next more significant ALU pack (CNXX1). Only the carry output of the most significant ALU chip is used (CSV1) (22B8). Each function of the ALU that is used is described inthe following pargaraphs. All gate references are to the arbitrary labels on Figure 11. The mnemonics indicated are the actual symbols used as reference on the ICs (22N7).

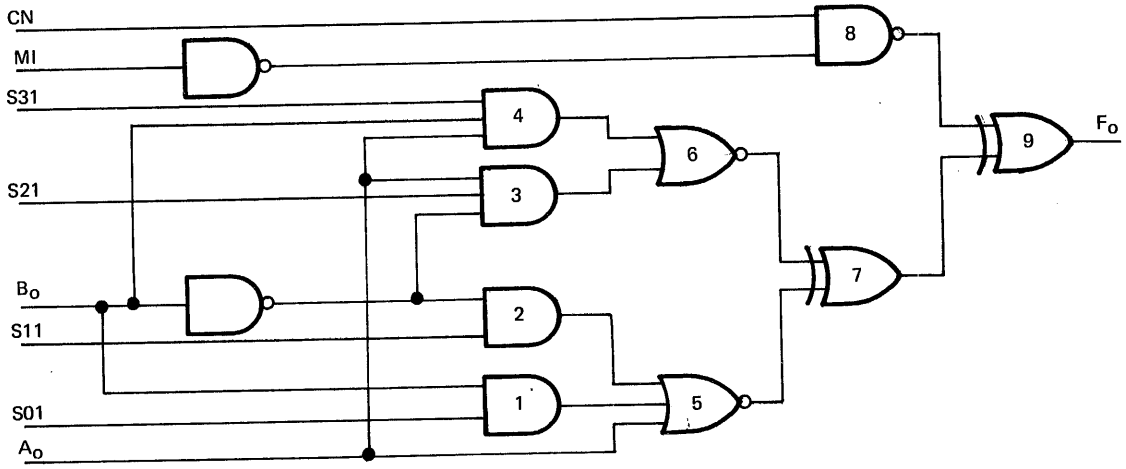


Figure 11. Least Significant ALU Stage

5.7.1 Load. The ALU is conditioned to the Load mode on any Load micro-instruction. In this mode, Gates 1, 2, 3, and 4 are enabled by S01, S11, S21, and S31 respectively, and Gate 8 is disabled by M1. Since both Gates 1 and 2 are enabled, at least one of their outputs are high producing a low at the output from Gate 5. The state of Gate 6 is the inverse of $\overline{Ao}$. If $\overline{Ao}$ is low, the output of Gate 7 is high and the output of Gate 8 is low ($\overline{Fo}$). For $\overline{Ao}$ high, the inverse is true at each stage causing $\overline{Fo}$ to also be high. Therefore, in this mode, the state of $\overline{Fo}$ is the same as the state of $\overline{Ao}$ independent of the $\overline{Bo}$ input. The state of the Gated B Bus is passed, unmodified, to the S Bus.

5.7.2 AND. The AND function produced by the AND micro-instruction conditions the ALU to logically AND each bit of the Gated B Bus with the gated outputs of the AR. In this mode the output equation for Gate 5 is (Bo·Ao) and the output equation for Gate 6 is (Ao). The simplified expression for the output from Gate 7 is then (Ao · Bo). Since Gate 8 is disabled by the M1 input to the ALU, its output is high causing the output from Gate 9 to be defined by the same equation as the output from Gate 7, the AND function.

5.7.3 OR. The OR micro-instruction causes each bit from the B Bus to be logically ORed with the corresponding bit from the gated output of the AR. Gate 5 produces a low because of the complimentary Bo inputs. The outputs equation for Gates 6 and 7 is (Ao + Bo) which corresponds to the $\overline{Fo}$ output from Gate 9.

5.7.4 Exclusive OR. The Exclusive OR micro-instruction produces a logical low at the S Bus if the corresponding bits on the Gated B Bus and the gated outputs of the AR are at different logic levels. The expressions for the outputs from Gates 5 and 6 are (Ao • Bo) and (AoBo) respectively. The function of the output from Gate 7 is; therefore, $A_o\overline{B_o} + \overline{A_o}B_o$, the Exclusive OR function. Since, once again, the output from Gate 8 is high, $\overline{F_o}$ is the same as the output from Gate 7.

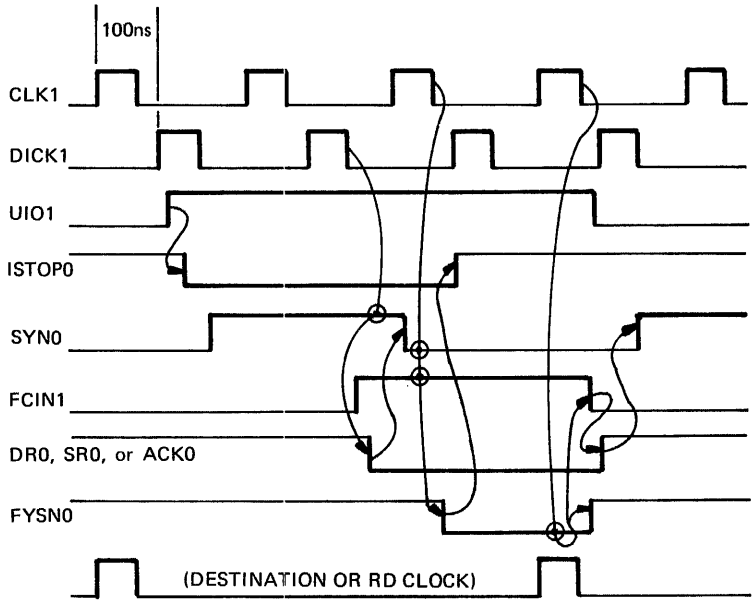
5.7.5 Add. The ALU is conditioned to the Add mode on either a command or an Add micro-instruction. Note that with the exception of the M1 control line, Add is the same as Exclusive OR. The M1 control line enables the carry network internal to the ALU device so that the output from Gate 8 is CN. Fo now becomes CN ($A_o\overline{B_o} + \overline{A_o}B_o$) + $\overline{CN}$ (AoBo + AoBo). Figure 11 shows only the least significant stage of the 19-039 four bit ALU. The next three stages are identical except for the internally propagated carry.

5.7.6 Subtract. The Subtract function produced by the four-bit ALU device is A-B-1. For this reason, the carry in to the least significant stage is inverted by the Exclusive OR gate (23B3) on a Subtract micro-instruction. The output equation for Gate 5 is (Ao • Bo) and the equation for Gate 6 is (Ao + $\overline{B_o}$). Gate 7 produces a high output when the equation (Ao • Bo + AoBo) is satisfied. The output function, $\overline{F_o}$ = CN ($\overline{A_oB_o}$) + $\overline{CN}$ (AoBo + $A_o\overline{B_o}$), yields A-B.

5.8 I/O Control

An I/O operation is initiated if I/O is the Source or Destination of a Load micro-instruction. The I/O control logic is shown on Sheet 25. If I/O is a source, then an input operation is initiated if I/O is a destination, an output operation is indicated. I/O timing is discussed separately for input and output.

5.8.1 Input. Refer to Figure 12 for input timing information. When I/O is specified as a source, unload I/O (UI10) (25N5) is decoded and ISTOP0 goes active. On the trailing edge of the next Delayed Clock (DICK 1) the Control In flip-flop (CIN) (25L7) sets. On receipt of SYN0 (26L1) or the detection of False Sync, the 14 millisecond timer (25N7) timed out, the Sync flip-flop (25J7) sets which deactivates ISTOP0. On the trailing edge of the next CLK1 the destination register is loaded and both the Control In and Sync flip-flops become reset completing the operation.



*SYN0 is active due to a previous I/O instruction.

Figure 12. I/O Input

5.8.2 Output. Refer to **Figure 13** for output timing information. An I/O out operation is very similar to the input operation. When Load I/O LDI01 (25N5) is detected, ISTOP0 goes active and on the leading edge of the next CLK1 the Data flip-flop, FDAT1 active (25F8), sets, the output of the Data flip-flop is used to gate data to the Data Bus, D000:160, (Sheet 15). On the trailing edge of the next DICK1 the Control Out flip-flop (25E7) is set which activates the specified output control line. The output operation now progresses in the same manner as the I/O input discussed previously.

To insure a minimum width of 350 nanoseconds on ADRS0 the FSR0 strap option (25H7) may be removed. Exercising this option allows the Catch flip-flop (25H7) to set on an address operation. The 0 output of this flip-flop delays the setting of the Sync flip-flop by 250 nanoseconds. All other sequencing is as discussed previously.

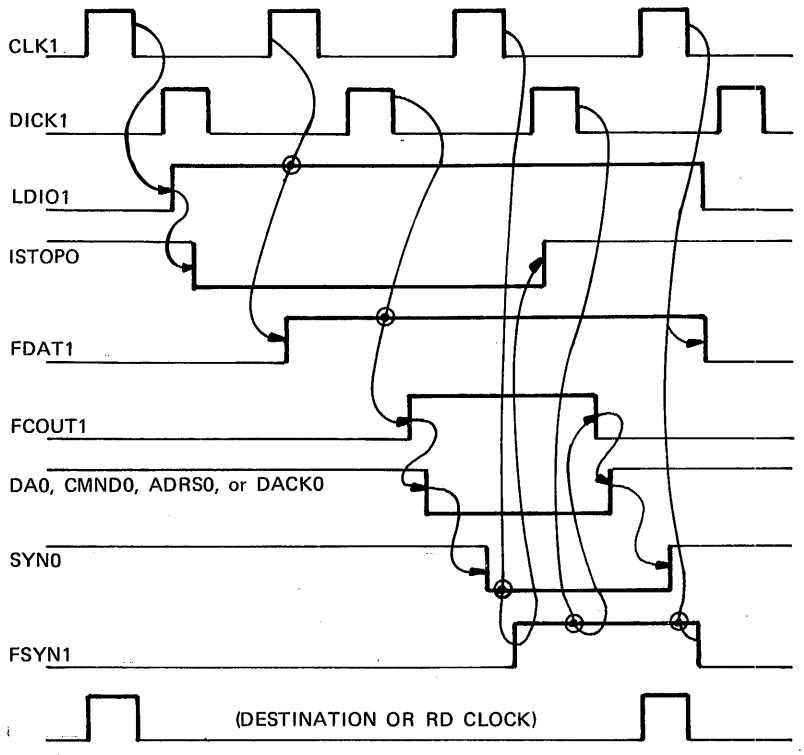


Figure 13. I/O Output

5.8.3 Hardware Assist Output. The 7/32 C Processor has a feature whereby the I/O D Bus may be used to transmit data to optional hardware assist features. A special address and control line validates the data being presented on the D Bus, to the hardware assist devices. (Refer to Figure 14 during the following description.) When the micro-program specifies a unique destination ('D') in any micro-instruction, the Hardware Assist Output logic becomes activated. The state of the Carry In bit (CI) of the Opcode Extension Two field is gated out on a unique line that is used to select one of two possible hardware assists features (BADR0 sheet 25A9). On the trailing edge of CLK1A the FBCNT flop sets (sheet 25D3), causing GDAT0 (sheet 25D5) to go low, gating the S Bus onto the D Bus. Also, BCNT0 (25D5) goes low when the FBCNT flop sets. BCNT0 validates the data on the D Bus as data intended for the hardware assist features. ISTOP0 becomes active when BENA1 (25C2) is decoded. ISTOP0 halts the processor to keep data from changing on the D Bus. When the FBCNT flop sets ISTOP0 becomes inactive allowing the processor to proceed.

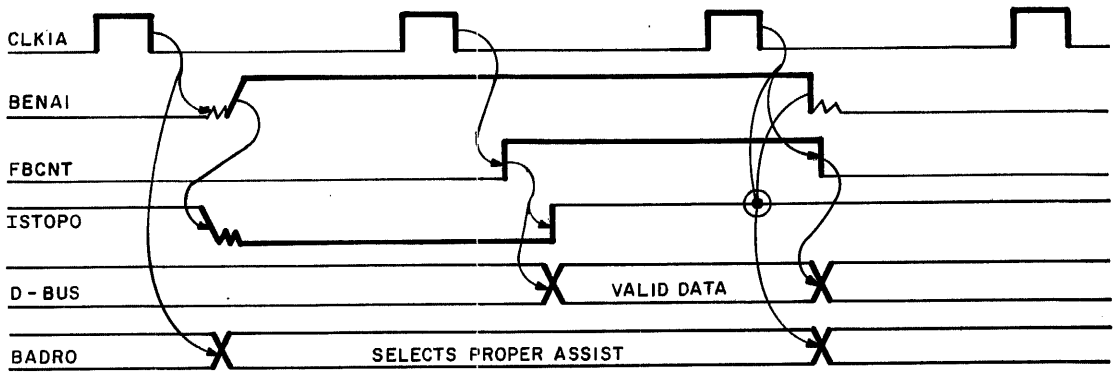


Figure 14. Hardware Assist Output

5.9 Memory Control and Timing

The memory control logic in the Processor is found on Sheet 27. Refer to Figure 15 A and B for memory control and timing information.

There are two different memory systems associated with this Processor, local memory and extended memory. Only local memory can be used with the Model 7/16 HSALU or the Model 7/32 C without either the Memory Access Controller or the Direct Memory Access Bus Controller options. In addition, for local memory, two difefrent memory timings are provided under option control, depending on whether 1 microsecond or 750 nanoseconds memories are equipped.

Local memory timing is initiated by a Direct Memory Access request, REQ0 active, or a Processor request, MEM1 active, either of which activates Set Local Memory Busy (SLMBY1) (27M4). On the leading edge of CLK1, with SLMBY1 active, the Early Read (ER) flip-flop (27E5) is direct set. The setting of the ER0 flip-flop triggers the local memory timing (refer to the Local Memory Timing Diagrams Figure 15 A and B).

On the trailing edge of the same clock which sets the ER flip-flop, the Local Busy (LBSY) flip-flop (27L5) is set, the Local Processor Busy (LPBSY) flip-flop (27K5), if the request for memory was from the Processor is set, and the Read (RD) flip-flop (27G5) for a Processor read operation is set. These flip-flops are used for controlling memory timing and clock stops within the Processor. The Read flip-flop is set for one clock and is used to indicate Data Unavailable (DU) (generate MSTOP0 if the MDR is specified as the source) when it is set. The two busy flip-flops are set for two clocks for 750 nanoseconds memory timing and three clocks for 1.0 microsecond memory timing. The Write (WT) flip-flop (26G7) is set on the leading edge of ER0 for write operations and reset on the same edge for read operations. This flip-flop is used to indicate to the memory system that a write operation is in progress and to inhibit the generation of Enable Memory Strobed data (ENMS1) (27 G9) when set.

A Direct Memory Access device (MAC, SELCH, etc.) requests a memory cycle by activating Request (REQ0) (27K1). On the leading edge of the first CLK1 after REQ0 becomes active. The Request flip-flop (27J3) is set thus activating the Enable (EN) flip-flop (27J5) and generating the EN0 control line to the DMA Bus. When the Enable (EN) flip-flop is set and memory is not busy, the Processor Select flip-flop (27H5) and the Enable flip-flop are reset, initiating a DMA memory cycle.

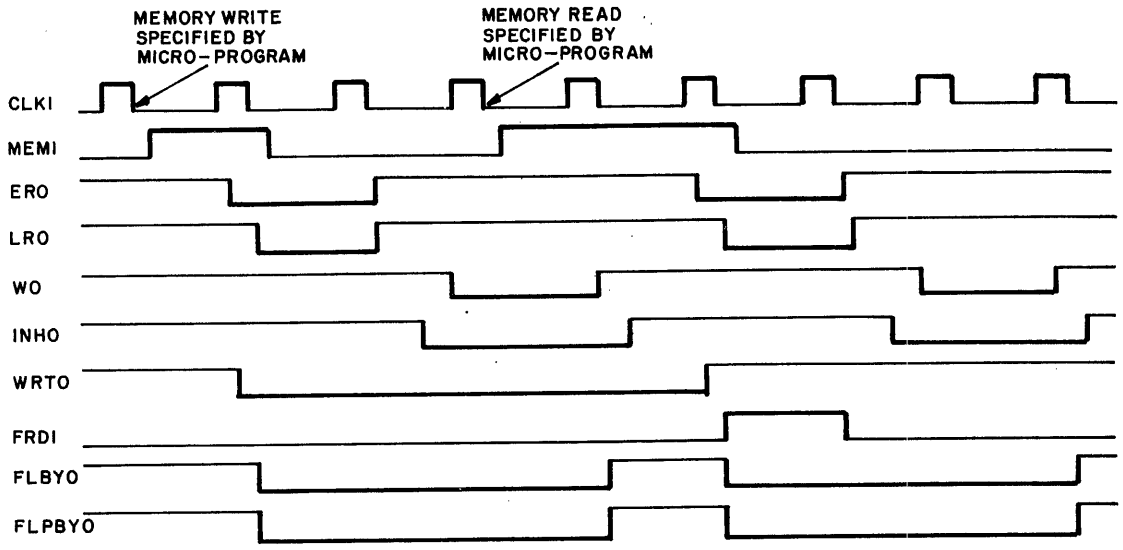


Figure 15.A Processor to Local Memory (1.0 Microsecond Memory)

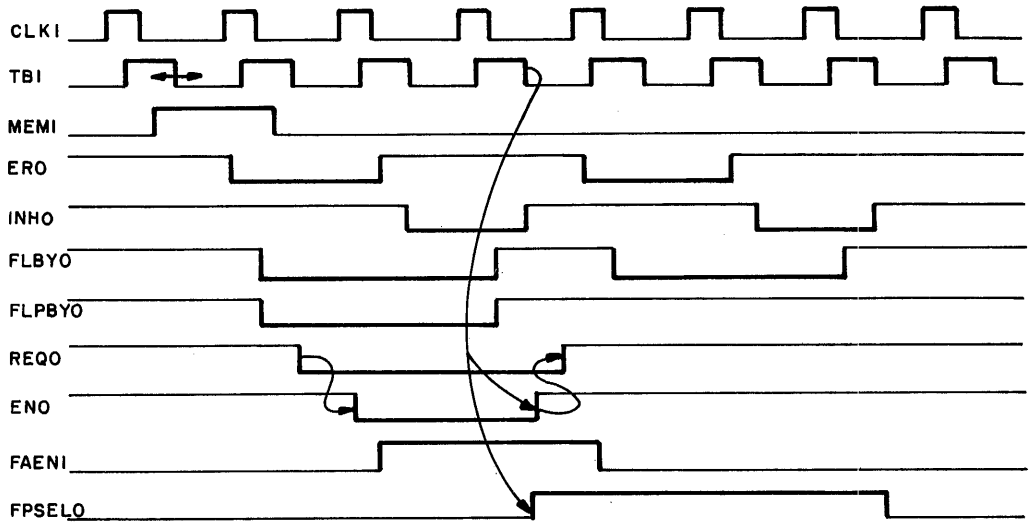


Figure 15.B Processor and DMA to Local Memory (750 Nanoseconds Memory)

When the Processor attempts a memory operation beyond Bank 0 (the first 256KB of memory) on a Model 7/32 C equipped with either a MAC or DMABC, XMEM0 is active. XMEM0 prevents the generation of local memory timing and sets the Extended Processor Busy (XPBY) (27N5) flip-flop. The MAC or DMABC then activates Extended Data Unavailable (EXDUA0) and Extended Busy (EXBYS0) until the memory cycle is complete. When the XPBY flip-flop is set a DMA device is still able to initiate a memory cycle to local memory. Refer to Figure 16.

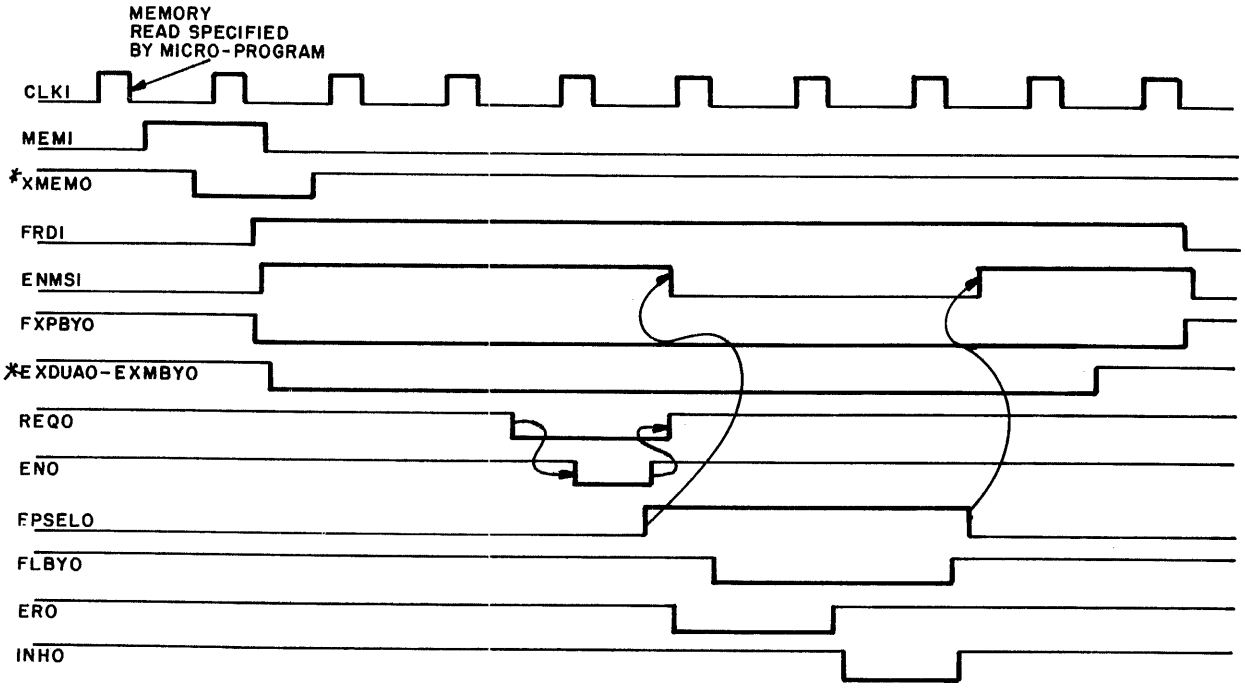


Figure 16. Extended Memory Timing and DMA to Local Memory

5.10 X Bus Logic (Model 7/32 C only.)

On the Model 7/32 C, the S and B Busses are extended to 20 bits for the purpose of address calculations. This logic is found on Sheets 9 and 10.

An additional four bit ALU (10N9) is appended to the standard 16 bit ALU to provide this 20 bit arithmetic and logic capability during a single machine cycle. Carry Save (CSV1) (10L9) is used as the carry input to this ALU. The Flag Register (Section 5.5.5)is not modified as a result of any operation on the X Bus. The operation of this logic including its associated registers has been covered in more detail in their individual sections described previously.

5.11 Calculate Address (Model 7/32 C Only)

The Calculate Address (CA) micro-instruction is used to generate an effective address of the second operand of a user instruction and load that address into the Memory Address Register. This micro-instruction requires a minimum of three machine cycles for its execution but could require more depending on the instruction format and the access and cycle time of the memory being used.

A phase counter (Sheet 8) is used to keep track of where, within the execution of the CA micro-instruction, the machine is at a given time. Refer to Figures 17A and 17B. Depending on the instruction format of the user instruction being executed different functions are performed. Refer to the 32 Bit Reference Manual, Publication Number 29-365, for descriptions of the various Memory Indexed (RX) instructions. The two most significant bits of the current contents of MDR determines the format being used.

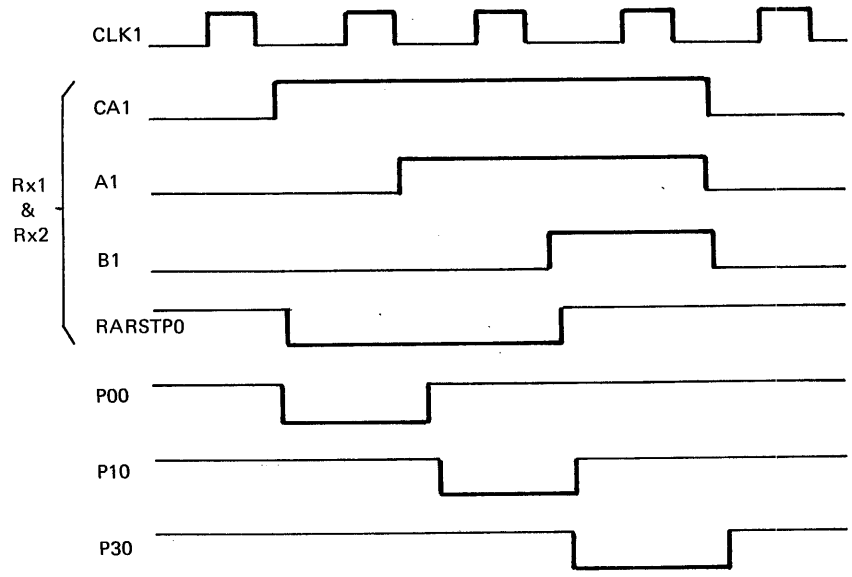
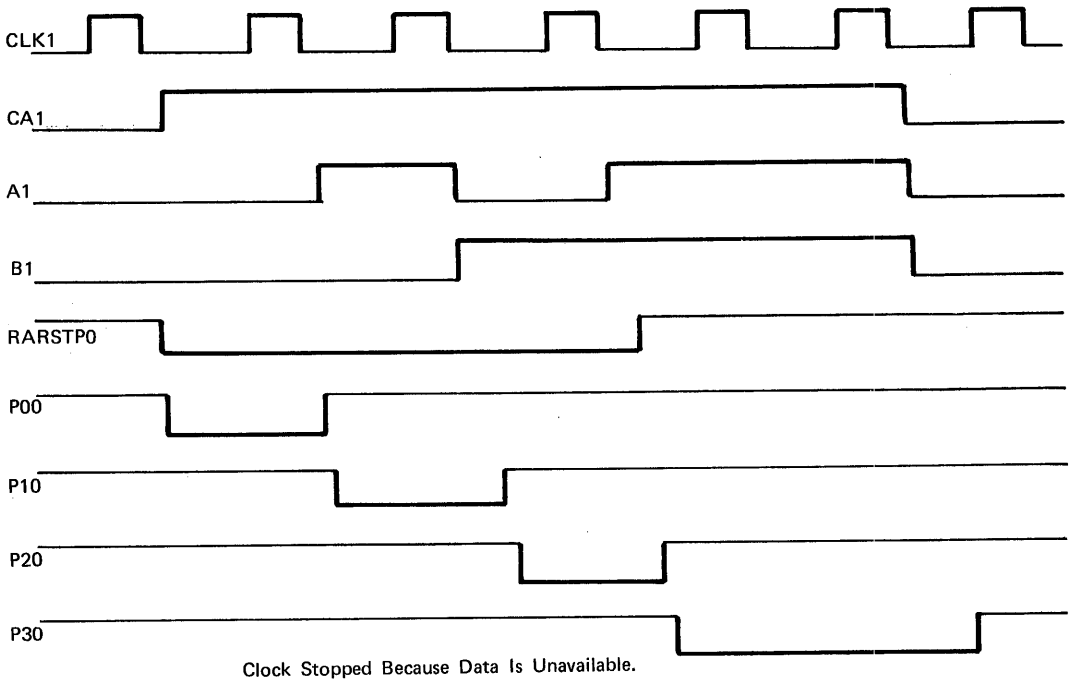


Figure 17A. Calculate Address RX1 or RX2



Clock Stopped Because Data Is Unavailable.

Figure 17B. Calculate Address RX3.

Phase zero, independent of the instruction format, is only used to decrement the ROM Address Register by one so that it points to the address of the CA micro-instruction. This is necessary because, set RD bits generated by the Calculate Address (CA) logic are ORed with the data from the ROM to modify the micro-instruction during the various phases of the CA.

During Phase zero of the CA instruction RARSTP0 is forced active. This prevents incrementing the RAR. Phase zero is also used to inhibit the RD clock (7D9) decremented the RAR by one (SK1) by generating a clock on the count up input to the RAR (negative logic is used). The Calculate Address instruction conditions the ALU to the Add mode. The following describes the execution of this instruction for each of the possible formats. Refer to Table 7 during the description.

TABLE 7. RX FORMATS FOR CALCULATE ADDRESS

FORMAT	PHASE	CONTENTS OF RDR	OPERATION
RX1	0	X'60A417'	Decrement RAR
RX1	1	X'60A417'	MDR→MAR
RX1	3	X'60BE17'	MAR + *AR→MAR
RX2	0	X'60A417'	Decrement RAR
RX2	1	X'60A417'	MDR + LOC→MAR
RX2	3	X'60BE17'	MAR + *AR→MAR
RX3	0	X'60A417'	Decrement RAR
RX3	1	X'60A417'	MDR04:07→YSI
RX3	2	X'61F617'	*AR + **YSLX→AR, MDR12:15→XMDR
RX3	3	X'60B617'	*AR + MDR→MAR

*Conditional on FAMOD
** Conditional on AMOD

5.11.1 RX1. The contents of the RDR during Phase one is an X'60A417'. This is normally decoded by the hardware as (A MAR, LOC, MDR). Gated RX1 or RX3 (GRX130) (8N8), however, disables the B Bus source causing the contents of MDR to be loaded into the MAR. Phase one also causes set RD bits (SRD110, SRD120, and SRD140) to go active which changes the contents of the RDR to an X'60A417' when Phase three is entered. In Phase one, for RX1, and RX2, RARSTP0 is deactivated which allows the RAR to increment to the next sequential instruction. Phase three executes the indicated operation (A MAR, MAR, AR). Since this instruction performs the indexing, the second source, AR, is conditional on the Address Modification (FAMOD0) (29N4) flip-flop. If the YS field of the user instruction contains all zeros the AMOD flip-flop is reset following an Instruction Read and Disable Source Two (DS20) (9K8) is active.

5.11.2 RX2. The CA micro-instruction for a RX2 format works the same as the RX1 format except the operation specified by RDR in Phase one (A MAR, LOC, MDR) is performed, GRX130 inactive. The sign bit, MDR011, is extended through the XB-Logic (10N3) since the value in MDR is in the two's complement form.

5.11.3 RX3. Phase one, for RX3 formats, does not change the contents of MAR, RX3P10 active (14K1). Phase one jams Bits 7, 9, 11, and 14 of the SR0 lines causing an X'61F67' to be loaded into the RDR in Phase two. This is decoded as (A AR, YSLX, AR, MRI). RX3P10 also loads MDR04:07 into the YS field of the IR (29G2). In Phase two the first and second level index values are added and loaded into the AR. The second source is conditional on FAMOD0 as described in Section 5.11.1. Phase two, in addition to performing the indicated function, also loads MDR Bits 12 through 15 into the Extended Memory Data Register (XMDR) (9K9) and jams SRD Bits 11 and 14 which causes an X'60B67' to be loaded into RDR in Phase three. Phase three then executes the indicated function (A MAR, MDR, AR).

5.12 Counter Dependent Operations

A Command micro-instruction with RD Bit 6 set implies a counter dependent mode of operation that is maintained until the Counter Register (CTR) is zero. Command Repeat causes the next micro-instruction to be repeated the number of times specified in the CTR. Command Multiply and Command Divide cause the Command itself to be repeated with SRH forced to be the Source and Destination Register. These modes are implemented by the circuit shown on Sheet 34.

5.12.1 Repeat. When a Command Repeat micro-instruction is executed, CMND1 goes high (34N2). The Repeat flip-flop (REPT) (34N5) toggles set on the trailing edge of CLK1. On the same edge, the Counter Mode flip-flop (CMODE) will toggle set if the CTR is not zero (CEMT0) (34K6). If the CTR is zero, the next micro-instruction should be not executed. Since, at the same time RPT flip-flop toggles set, the next micro-instruction toggles into RD, the Processor has to execute the instruction. However, SDSTOP0 goes active (34N9) stopping the Destination Clock. No register is modified, nor is the FLR changed. RPT toggles (34N9) reset on the next CLK1.

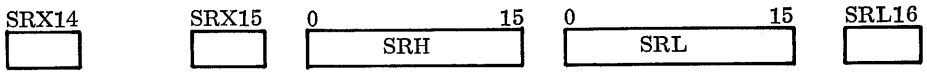
If the CTR is not zero, CMODE and RPT both toggle set. The target micro-instruction is in RD. Because CMODE is set, DECTR0 (34M9) goes low until the CTR is zero. The CTR will decrement on each Destination Clock (DC). As long as CMODE is set and the CTR does not equal zero or one (CTONE0) (34L9), SRSTP0 is low (34L9), disabling CLKRD0 and RDSTP0 (19L9). The RAR will not increment nor will another micro-instruction be strobed into RD until the Counter (CTR) decrements from one to zero. As soon as the CTR decrements from one to zero, CMODE and RPT both toggle reset, SRSTP0 is high and the next sequential micro-instruction is executed.

5.12.2 Multiply. Prior to executing the Command Multiply micro-instruction, the following preliminary conditions are assumed:

1. The MDR contains the multiplicand in two's compliment form.
2. ARL contains twice the multiplicand in two's compliment form.
3. SRL contains the multiplier in two compliment form.
4. The Carry flag (FLR121) contains the most significant bit of the multiplicand.

These registers are loaded by the micro-program.

SRH and SRL with a two bit extention on the left and a one bit extention on the right is used to contain partial products. When multiplication is complete SRH and SRL contains the 32 bit result.



SRL16 is used to remember the last bit shifted out and SRX14, SRX15, SRH, and SRL are used to contain the partial products (34 bits are required to represent signed partial products in two's compliment form). The least significant 18 bits of the first partial product are zero, SRL contains the 16 bit multiplier. SRL14, SRL15, and SRL16 are used to decide which operation is to be performed. After calculating a parital product, an arithmetic shift of two places is performed of the entire partial product. This procedure is repeated until all multiplier bits are shifted out.

The algorithm used in the multiplication instruction requires 10 machine cycles for its execution. The first clock of the instruction, Clear Shift Register High (CSRH1) (36C7) active, is used to clear SRH, SRL16, SRX14, and SRX15 and load the Counter with an X'09'. The next eight clocks perform the multiplication by executing either an Add or Subtract operation on the partial product contained in SRX and SRH and either the multiplicand contained in MDR, twice the multiplicand contained in ARL, or zero depending on the result of the shift operation SRL14:16. Refer to Table 8.

TABLE 8. OPERATION CODE

SRL14	SRL15	SRL16	OPERATION
0	0	0	ADD Zero to SRH
0	0	1	ADD Multiplicand to SRH
0	1	0	ADD Multiplicand to SRH
0	1	1	ADD 2x Multiplicand to SRH
1	0	0	SUB 2x Multiplicand from SRH
1	0	1	SUB Multiplicand from SRH
1	1	0	SUB Multiplcand from SRH
1	1	1	SUB Zero from SRH

On the last clock of the multiplication, the operation to be performed differs depending on whether a signed multiplication C MPY (RD091 inactive) or an unsigned multiplication C UMPY (RD091 active) is being executed.

If Signed Multiply:

L SRH, SRH, SR is performed.

If Unsigned Multiply:

L SRH, SRH, SR is performed if SRL161 is inactive.

or

A SRH, SRH, MDR, SR is performed if SRL161 is active.

Shift Register High (SRH) is conditioned to the load state during the first clock of the pulse pair of SHCLK0 and to the Shift Right mode during the second clock. The second shift is performed by the fact that the B Bus Multiplexor (Sheet 20) is conditioned to the Shift Right mode. SRL is conditioned to the Shift Right state for both clocks. Refer to timing diagram Figure 18.

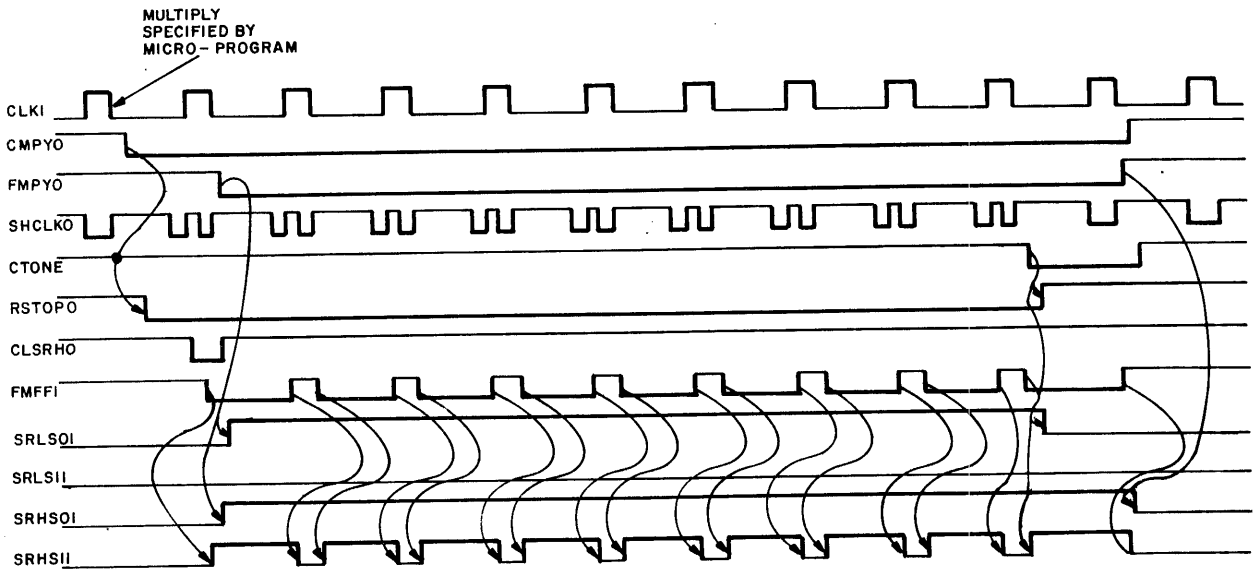


Figure 18. Multiply Timing

During Command operations the ALU is conditioned to the ADD mode. If a Subtract operation is required, Force Subtract (FRSUB0) (36M4) is activated, which conditions the ALU to the Subrtact mode. A four-bit Adder (36G5) is used to allow a 20-bit parallel operation to be performed during the execution of the Multiply algorithm. The 'A' input to this adder is SRX and the B input is a function of the Carry flag.

Table 9 shows the hexadecimal contents of each of the registers during each clock of the multiplication of 5 multiplied by 4. Prior to execution, MDR contains a X'5', ARL contains a X'A', and the Carry flag is reset.

Table 10 shows another example of a multiplication (X'1111'*X'1111'). Prior to execution, MDR contains a X'1111, ARL contains a X'2222' and the Carry flag is reset.

TABLE 9. MULTIPLICATION EXAMPLE (5 x 4)

	SRX14		SRH			SRL				SRL16
1	0	0	0	0	0	0	0	0	4	0
2	0	0	0	0	0	0	0	0	1	0
3	0	0	0	0	2	4	0	0	0	0
4	0	0	0	0	0	5	0	0	0	0
5	0	0	0	0	0	1	4	0	0	0
6	0	0	0	0	0	0	5	0	0	0
7	0	0	0	0	0	0	1	4	0	0
8	0	0	0	0	0	0	0	5	0	0
9	0	0	0	0	0	0	0	1	4	0
10	0	0	0	0	0	0	0	1	4	0

TABLE 10. MULTIPLICATION EXAMPLE (X' 1111' x '1111')

	SRX		SRH			SRL				SRL16
1	0	0	0	0	0	1	1	1	1	0
2	0	0	8	8	8	4	4	4	4	0
3	0	0	2	2	2	1	1	1	1	0
4	0	0	9	1	1	8	4	4	4	0
5	0	0	2	4	4	2	1	1	1	0
6	0	0	9	1	9	C	8	4	4	0
7	0	0	2	4	6	3	2	1	1	0
8	0	0	9	1	A	0	C	8	4	0
9	0	0	2	4	6	4	3	2	1	0
10	0	0	1	2	3	4	3	2	1	0

5.12.3 Divide. Prior to executing the Command Divide micro-instruction, the following preliminary conditions are assumed: The 32-bit positive dividend is in SRH and SRL, the divisor is in two's complement negative form in the ARL, the carry flag is reset, and the CTR contains 16. The Command Divide executes in 16 machine cycles. On each DCL0: the CTR is decremented, SRL is shifted left one position, FLR12 is updated from the ALU carry, and SRH is either shifted left one position or loaded from the S Bus. Refer to Figure 19.

The signal CDIV0 is low during the Command Divide. CDIV0 causes DECTR0 to go low until the Counter (CTR) decrements to zero. SRL is conditioned to the Shift Left mode, and SRH assumes the Load mode or the Shift Left mode depending upon the state of the ALU Carry (CSV1).

The most significant 16-bits of the dividend in the SRH are present on the B Bus. The data is shifted left one position by the B Bus Shifter and presented to the ALU. Note that SRL001 is carried into CISL0 (36R5). The ARL is unloaded to the ALU and an 'Add' is performed.

By adding the two's complement from the divisor in the ARL to the most significant half of the dividend in the SRH, the result on the S Bus is actually the difference between the two. If this 'trial subtraction' is successful, the ALU produces a Carry (CSV1 high), and the partial remainder on the S Bus is gated into the SRH. If the 'subtraction' is unsuccessful, CSV1 is low, and the SRH is shifted left one position; the S Bus data is ignored. The CSV1 signal is shifted into SRL15 to form the quotient bits. CSV1 is also saved in FLR12. After the Command Divide, the remainder is in the SRH and the quotient is in the SRL.

5.13 Display System

The Display System provides, if the Hexadecimal Display Panel is present, a means for reading the contents of all the system registers and any core memory location, together with the capability of manually entering data and programs. Figure 20 shows the Hexadecimal Display Panel layout. Within the Hexadecimal Display Panel are five eight-bit byte Display Registers, D1 through D5, that hold data output from the Processor, and a 20-bit Switch Register which stores data input from the Hexadecimal Keyboard.

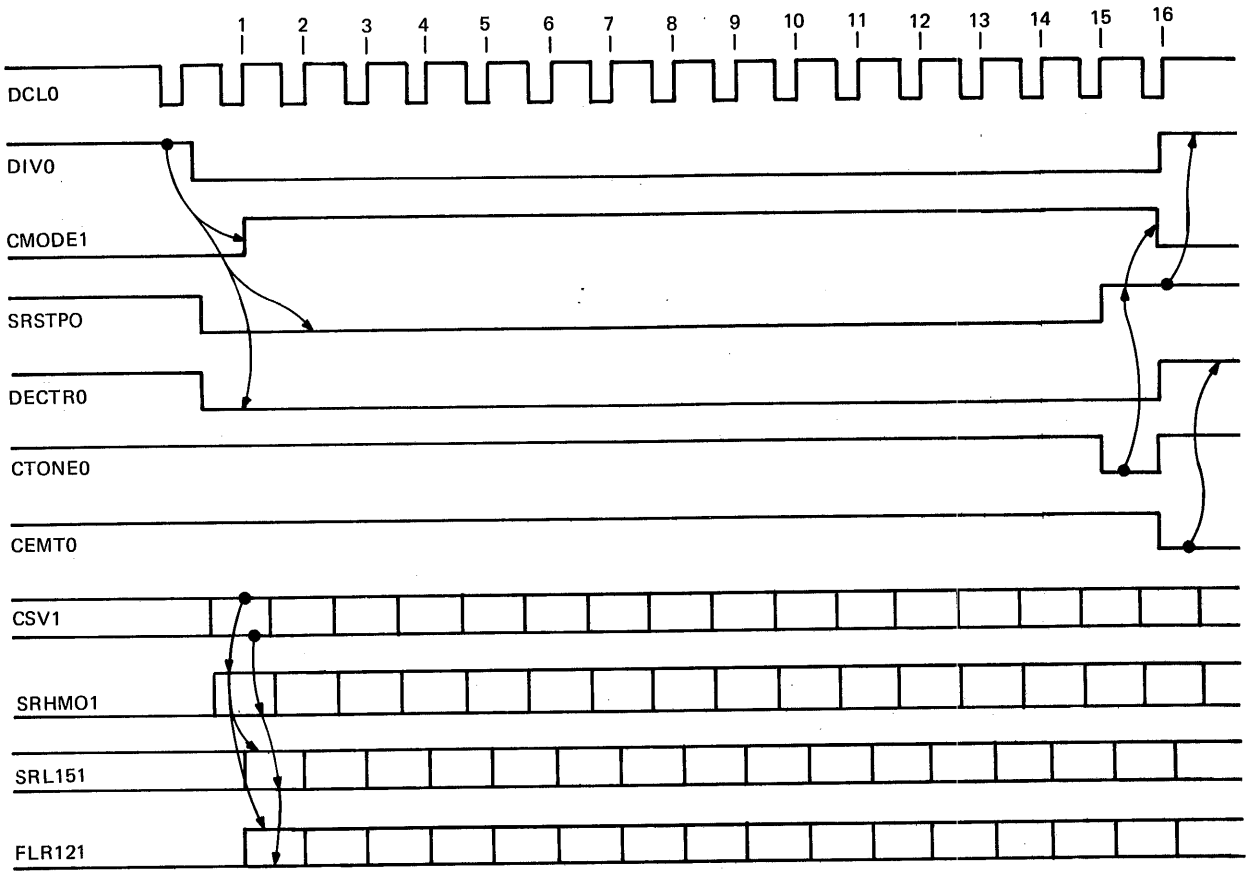


Figure 19. Command Divide Timing Diagram

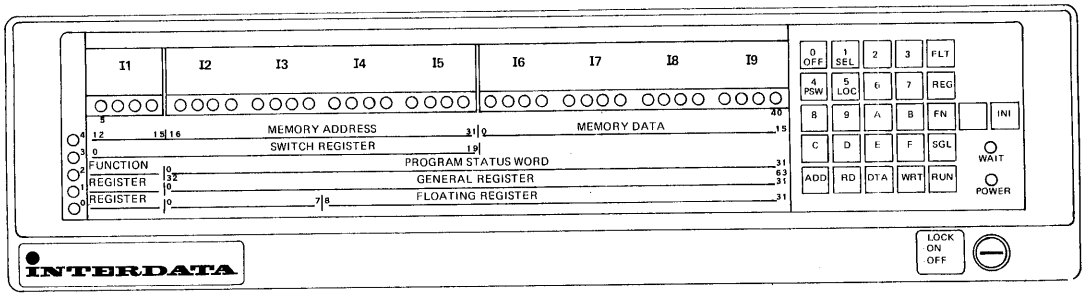


Figure 20. Hexadecimal Display Panel

Associated with each Display Register D1 through D4 are eight indicator lamps that provide a binary read-out and two optional hexadecimal read-out indicators. Associated with Display Register 5 are four indicator lamps for binary display and one optional hexadecimal read-out indicator.

The most significant four bits of Display Register D5 (Bits 0:3) control four of the five indicator lamps along the left edge of the Hexadecimal Display Panel. The fifth indicator lamp is controlled by logic internal to the Hexadecimal Display Panel. To the right of each of these five lamps is a diagram that defines what is being displayed. In general, only one of the diagram lamps is on at a time. If none of the diagram lamps are on, a user program has written data to the display registers.

The most significant 20-bits of the display show the contents of Display Registers D3 and D4 and the least significant four bits of Display Register D5 (Bits 4:7) or the contents of the 20-bit Switch Register. When the Switch Register is being displayed, the lamp next to the Switch Register diagram is illuminated. Any other diagram lamp that may have been on, remains on. When the Switch Register is no longer displayed, its diagrma lamp goes out and the most significant 20-bits of the display again shows the contents of Display Registers D3 and D4 and the least significant four bits of Display Register D4 (Bits 4:7).

The Key Operated Security Lock is a three-position, OFF-ON-LOCK, key-operated locking switch, which controls the primary power to the system. This switch can also disable the Hexadecimal Display Panel, thereby preventing any accidentical manual input to the system. The power indicator lamp (PWR) associated with the key lock is located in the lower right corner of the Hexadecimal Display Panel. The PWR lamp is on when the key lock is in the ON or LOCK position. The relationship between the key lock switch positions, primary power, the Control keys, and the Hexadecimal keys is:

OFF	The primary power is OFF.
ON	The primary power is ON and the Control keys and Hexadecimal keys are enabled.
LOCK	The primary power is ON and the Control keys and Hexadecimal keys are disabled.

The Hexadecimal Display Panel operating procedures may be found in the appropriate User's Manual.

The Display Controller, built into the Processor, is shown on Sheet 26. Unlike most I/O controllers, data transfer does not take place over the D Bus. Data from the Hexadecimal Display Panel is gated directly to the B Bus, B08:14, and the content of the S Bus, S08:15, is gated by DAG1 and sent to the Hexadecimal Display Panel. Data is transmitted between the Hexadecimal Display Panel and the Display Controller one byte at a time.

5.13.1 Data Transfer. When the display is in the Normal mode, all data outputs are directed into Display Register D1. Conditioning the controller to the Incremental mode, via an Output command, causes the two bit counter (26H7) to be incremented at the trailing edge of DAG1. The output of this counter is decoded to activate LA0, in response to the first DAG1 and then LB0 for all subsequent DAG1's until the counter is initialized. In this mode, the first DA loads Display Register D1, the next DA loads Display Register D2. The next two DAs load Display Registers D3 and D4. This counter is initialized by SCLR0, by an Output command placing the controller in the Incremental mode, or whenever the display is addressed and the Normal mode is selected.

Input data from the Switch Register on the Hexadecimal Display Panel is handled in a similar manner as output data. In the Normal mode or on the first Data Request (DR), if in the Incremental mode, Switch Register Bits 12:19 are read. The second DR, in the Incremental mode, reads Switch Register Bits 4:11. The two bit counter (26H5) directs the DR to the appropriate group of Switch Registers. This counter is initialized by the same function as the four bit counter discussed above and is incremented at the trailing edge of DRG1.

NOTE

Bits 0:3 are gated out as part of the status byte when address is read.

5.13.2 Control Logic. When the display requires micro-program support, it generates two outputs, ESNO0 and ESNC0, which are latched in the RS flip-flop at 26C2. The output of this flip-flop sets the Console Attention flip-flop (CATN) at 26F1. This flip-flop is reset by GADR0 when the Processor addresses the display.

When the SGL function switch is depressed, SSGL1 becomes active (26A2) and ESNC0 and ESNO0 are generated which caused the Single flip-flop (26G3) to become set. This flip-flop remains set until another execute is generated and the SGL function is not selected.

5.13.3 Status Input. The status byte encoding is shown in Table 11. The status byte is gated onto the SD00:07 lines by the SRG0 lead. SRG0 gates the SD00:07 lines onto Bits 08:15 of the B Bus.

TABLE 11. DISPLAY STATUS AND COMMAND ENCODING

STATUS

	0	1	2	3	4	5	6	7
Run	X	0	0	0	X	X	X	X
Memory Write	X	0	0	1	X	X	X	X
Memory Read	X	0	1	0	X	X	X	X
Address	X	0	1	1	X	X	X	X
Fixed Register	X	1	0	0	X	X	X	X
Floating Register	X	1	0	1	X	X	X	X
Function	X	1	0	0	X	X	X	X

General Register									Floating Register
0	0	1	0	X	1	0	0	0	0
1	1	1	0	X	1	0	0	0	
2	0	1	0	X	1	0	0	1	2
3	1	1	0	X	1	0	0	1	
4	0	1	0	X	1	0	1	0	4
5	1	1	0	X	1	0	1	0	
6	0	1	0	X	1	0	1	1	6
7	1	1	0	X	1	0	1	1	
8	0	1	0	X	1	1	0	0	8
9	1	1	0	X	1	1	0	0	
A	0	1	0	X	1	1	0	1	A
B	1	1	0	X	1	1	0	1	
C	0	1	0	X	1	1	1	0	C
D	1	1	0	X	1	1	1	0	
E	0	1	0	X	1	1	1	1	Floating Register E
F	1	1	0	X	1	1	1	1	General Register

Function									
0	0	1	0	0	0	0	0	0	Console Interrupt Register Set Select
1	1	1	0	0	0	0	0	0	
2	0	1	0	0	0	0	0	1	
3	1	1	0	0	0	0	0	1	
4	0	1	0	0	0	0	1	0	PSW
5	1	1	0	0	0	0	1	0	LOC
6	0	1	0	0	0	0	1	1	
7	1	1	0	0	0	0	1	1	
8	0	1	0	0	0	1	0	0	
9	1	1	0	0	0	1	0	0	
A	0	1	0	0	0	1	0	1	
B	1	1	0	0	0	1	0	1	
C	0	1	0	0	0	1	1	0	
D	1	1	0	0	0	1	1	0	
E	0	1	0	0	0	1	1	1	
F	1	1	0	0	0	1	1	1	Function

COMMAND

Normal	1	0	0	0	0	0	0	0
Incremental	0	1	0	0	0	0	0	0

5.14 Turnkey Console (Figure 21)

Refer to Functional Schematic 02-352C03. The Basic Switch Control Panel provides a means by which a program, previously loaded into memory, can be executed without the aid of the optional Control Console.

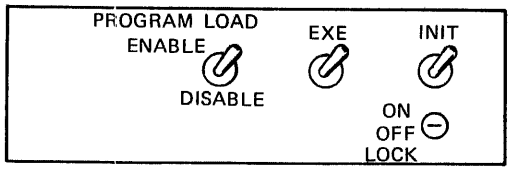


Figure 21. Turnkey Console

This panel provides a means of controlling the system power, initializing the system, and generating a Console Attention (FCATN1) to start program execution, if the Primary Power Fail/Auto Restart option is not installed.

This option conditions the Processor to the Run mode by grounding SSGL1, SD011, SD021, and SD031 at the Control Console connector. The status of the display is X'8F'. If a data byte is read from the display it is X'8F'. The Display Controller, when addressed by the micro-program in the power up sequence, indicates the Run mode. With the Auto-Restart option present, program execution commences at the address specified in the Location Counter (LOC), when the system is turned on and without the Auto-Restart option the micro-program performs a normal power sequence and then goes to the un-interruptable idle Loop until the Execution (EXE) switch is operated. When the EXE switch is operated, program execution then begins as described previously.

6. MAINTENANCE

This section describes maintenance procedures which may be used to check and, if necessary, adjust the Processor.

6.1 Clock Timing

Clock timing is checked with an oscilloscope. By monitoring CLK1 B at the Processor back panel, Slot 7, Pin 202-1 of the CPU-A board. The period of CCK1B should be 250 nanoseconds. Refer to Figure 22.

6.2 Clock Timing for 35-624, CPU-A

There is only one adjustment associated with the Processor clocks. The variable Capacitor C70 on the CPU-A board 35-624 is very stable and should not require field adjustment. The adjustment should only be changed after the test indicates that it is out of tolerance and there are no faulty components in the system.

Clock timing is checked with an oscilloscope by monitoring CLK1 B at the Processor back panel, Slot 7, Pin 202-1 of the CPU-A board. The period of CLK1B should be 250 nanoseconds. Refer to Figure 22. Adjust Capacitor C1 to obtain the 250 nanosecond period.

6.3 Fast Memory Timing Adjustment

The fast memory timing adjustment is set up at the factory and should not require field need adjustments. There are two adjustments for fast memory timing: (1) adjust the time between the falling edge of the ER0 and the falling edge of INH0. (2) adjust the width of INH0. Potentiometer R47 adjusts the start time of INH0. Potentiometer R45 adjusts the width of INH0. Refer to Figure 20. Grounding REQ0 at the Processor back panel Slot 7, Pin 139-0 of the CPU-A board causes constant memory cycles to occur. Before grounding REQ0, remove MAC or extended DMA buffer if installed. ER0 may be found at Slot 7, Pin 204-0 of CPU-A. INH0 may be found at Slot 7, Pin 104-0 of CPU-A.

CAUTION

WHEN SETTING UP FAST MEMORY TIMING, UNPLUG ALL MEMORY STACKS UNTIL THE MEMORY TIMING IS ADJUSTED. FAILURE TO DO SO MAY CAUSE DAMAGE TO THE MEMORIES.

WITH ALL MEMORY STACKS UNPLUGGED, THE PROCESSOR MAY NOT POWER-UP. THIS IS BECAUSE THE -16.5VDC CROWBAR IN THE POWER SUPPLY HAS TRIPPED, REMOVING THE -16.5VDC. LOWER THE -16.5VDC TO CORRECT THIS. BE SURE TO READJUST THE -16.5VDC AFTER PLUGGING THE MEMORY MODULES BACK IN.

6.4 DMA Clock Adjustment for the 35-624 CPU A

The DMA clock (TB1) adjustment is set at the factory and should not require any further adjustment. The DMA clock (TB1) determines, when EN0 is active, when to turn EN0 OFF. To properly adjust TB1 for the 7/16 HSALU, the adjustment should be made while observing the time difference between EN0 and ER0. The adjustment must be made such that the time between the rising edge of EN0 and the falling edge of ER0 is 90 nanoseconds. Adjusting TB1 on the 7/32 C Processor is done by observing FPSEL0 and ER0 on the back panel and adjusting TB1 such that the rising edge of FPSEL0 occurs 115 nanoseconds before the falling edge of ER0. The variable resistor R46 adjusts the TB1 timing.

6.5 Overall Processor Test

Use the 06-106 Processor Test Program to perform a comprehensive test of the 7/16 HSALU Processor.

Use the 06-154 Series 32 Processor Test Part 1, 06-155 Series 32 Processor Test Part 2, 06-178 Series 32 Processor Test Part 3 and the 06-156 F01, F02, and F03 Series 32 Memory Test.

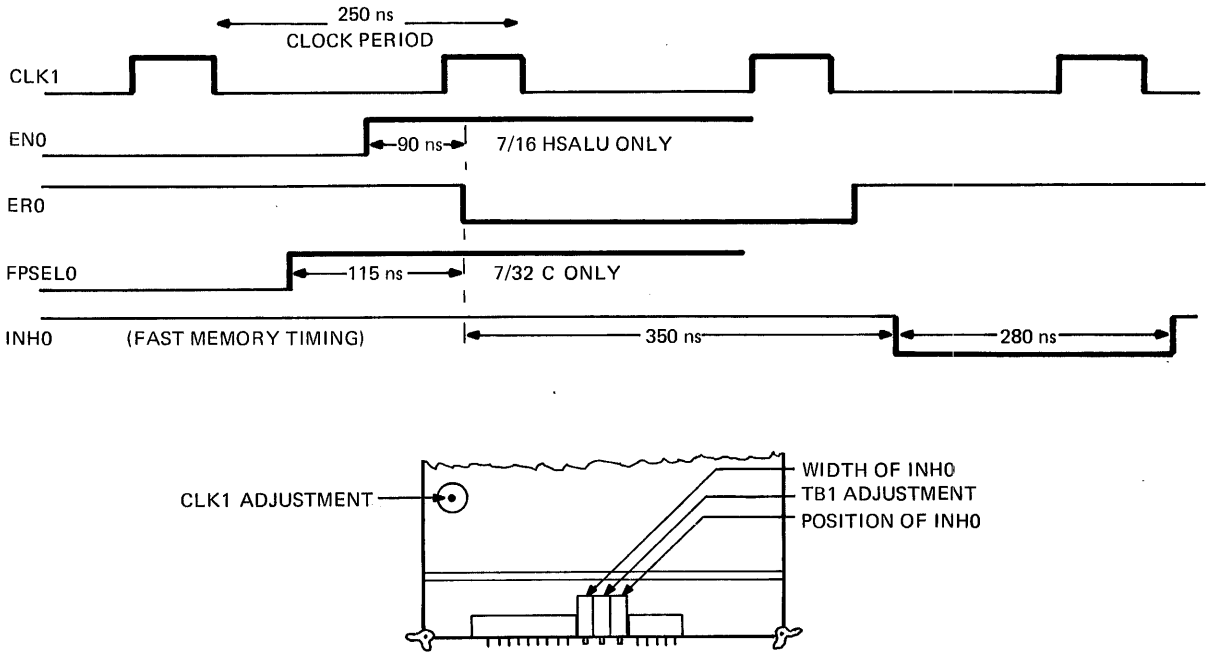


Figure 22. Clock Timing

7. Mnemonics List

The following list provides a brief description of each mnemonic found in the 7/16 HSALU and 7/32 C Processor. The source of each signal on Schematic Drawing 01-097D08 is also provided.

MNEMONICS	MEANING	SCHEMATIC LOCATION
ACK0	Acknowledge Control Line. This signal starts the Rack0/Tack0 Daisy Chain.	25D9
ADD0	Add micro-instruction Decoded	14D9
ADRS0	Address Control line	25A9
AMOD0	Address modification	29R3
ARST1	Automatic Restart	31K6
ATN0	Attention Test line from the I/O Bus	31G1
ATNX1	I/O attention but no higher peiority interrupts	33B9
BCNT0	Hardware Assist output control	25D5
BCLK0	Basic Clock. A non-stoppable clock used for memory timing and test aid control.	11J1
BENA1	ROM decoded Hardware Assist destination	25C3
B000:150	The B Bus which transmits data from the specified source to the shifter.	12A9-12K9
BRCH1	Branch. This indicated a Branch micro-instruction	14F9
BRCMND0	Branch or Command micro-instruction decoded	30F4
CA0	Calculate address Micro-instruction decode	14E9
CATN1	Console Attention. Special Interrupt from the Display Panel	31G9
CC12:151	Condition Code Bits 12 through 15; Carry, Overflow, Greater than, and Less than	30G9-30N9
CDIV0	Command Divide micro-instruction decoded	34R9
CEMT1	Counter empty	34E9
CIN21	Carry into ALU Bits 8 through 11	22B9
CIN31	Carry into ALU Bits 12 through 15	22A4
CISHI	Carry into Shift Register High	36K9
CISLI	Carry into Shift Register Low	36M9
CISL0	Carry in Shift Left to 'B' Bus Latch	36N5
CISR0	Carry in Shift Right to 'B' Bus Latch	36N5

MNEMONICS	MEANING	SCHEMATIC LOCATION
CKMDH0	Clock Memory Data High	18B4
CKMDL0	Clock Memory Data Low	19B4
CKRD0	The Clock used to Load the ROM Data Register and increment the ROM address	7F8
CLK1	The major Processor Clock from which all other clocks are derived	32L3
CLMDR0	Clear Memory Data Register	19B-27F9
CLO70	Control Line 7. This function provides an Early Power Fail indication to devices on the I/O Bus.	25A9
CLRF0	Clear Alarm Register flip-flops	28G7
CLSRH0	Clear Shift Register High ANDed with Processor Clocks	36M3
CMDTS0	Command Test and Set to Memory Access Controller	34H9
CMD0	Command Control line	25C9
CMND0	Command micro-instruction Decoded	14E9
CMPY0	Command Multiply Micro-instruction Decoded	34R9
CPLOC1	Carry propagate for the Location Counter	17A1
CPMAR1	Carry propagate for the Memory Address Register	16D1
CRYIN0	Carry into the least significant bit of the ALU	33M9
CS0	Cross Shift. Conditions the B Bus shifter to perform a Cross Shift.	30R3
CSL0	Command Shift Left micro-instruction	34R9
CSRH0	Clear Shift Register High	36C7
CSR0	Command Shift Right micro-instruction	34S9
CSVDIV0	Divide Carry Save	36F7
CSVI	Carry Save. Carry out from the ALU	22C8
CTONE0	Counter equal to One (1).	34L9
DA0	Data Availabel Control line	25C9
DACK0	Data Channel Acknowledge interrupt	25B9
DC0	Data Channel interrupt	31J1
DCR0	Data Channel Read operation (7/16 HSALU). Presence of Communications Hardware Assist (7/32 C only).	31J1
DEC10	Decode ROM #1. Decoded from micro-instruction.	35G1

MNEMONICS	MEANING	SCHEMATIC LOCATION
DEC20	Decode ROM #2. Decoded from micro-instruction	35F9
DECTR0	Decrement the Counter	34M9
DIR0	Second Time the same Instruction.	33A9
DMAC0	Disable MAC or DMABC Controller.	35C9
D000-D150	I/O Bus data lines.	Sheet 15
DON0	Timing signal derived from functions of the Processor Clock Counter.	32N3
DS20	Disable Source Two	8L9
DSA0	Disable Source A.	35M9
DSB1	Disable Source B.	14R9
DR0	Data Request Control line.	25B9
DSTOP0	Destination Stop. Prevents the loading of any destination register when active.	33G9
ENDA1	Enable Destination 'A'.	14G1
ENDB1	Enable Destination 'B'.	14J9
ENDD1	Enable Destination 'D'.	14K9
ENH1	Enable High. Enables the loading of the Memory Data Register Low.	16S8
ENMS1	Enable Memory Sense. During data time of memory read cycle.	27G9
ENSA0	Enable Source 'A'.	35S9
ENSB0	Enable Source 'B'.	14S9
EN0	Enable signal to the direct Memory Access Port.	27K9
EPF0	Early Power Failure detected.	32K4
ER0	Early Read, used for Read Memory Timing.	27F9
ESNO0	Execute switch normally open contact.	26A2
ESNC0	Execute switch normally closed contact.	26A1
EXBYS0	External or Extended Memory Busy.	27L1
EXDUA0	External or Extended Memory Data Unavailable.	27G1
FABORT1	Abort flip-flop, set during Abortable instruction.	34F9
FAEN0	Auxillary EN0 flip-flop	27J9
FA1	Output from the Processor Timing flip-flop, State A.	32H1

MNEMONICS	MEANING	SCHEMATIC LOCATION
FAIFBO0	Timing signal derived from Processor Clock flip-flop	32J3
FAMOD0	Address Modified flip-flop.	29R4
FB1	Output from the Processor Timing flip-flop, State B.	32G1
FBCNT0	Output from the Hardware Assist flip-flop	25D3
FCATN1	Output from the Console Attention flip-flop indicating a request for Console Service.	26H1
FDAT0	I/O Data Output flip-flop.	25G9
FDECI0	Decode Type #1 flip-flop.	35B9
FDEC20	Decode Type #2 flip-flop.	35C9
FEPF0	Output from the Early Power Fail relay.	32J5
FHLD0	Hold flip-flop for slow memory timing.	27C6
FINR0	Output from the Instruction Read flip-flop.	35K9
FLRAR0	Load ROM Address register flip-flop.	8G4
FLBY0	Local Memory Busy flip-flop.	27L9
FLGL0	Flag Register Greater than or Less than set.	30N9
FLPBY0	Local Processor Memory Busy flip-flop.	27K9
FL121-151	Flag Register Bits 12 through 15.	30H7-30N7
FMBY0	Memory Busy flip-flop.	36B7
FMFF1	Multiply Operation flip-flop.	36K8
FPF1	Power Fail Detection flip-flop.	32J6
FPOW1	The one output from the Power Down flip-flop. Set by the micro-program to Initialize the system.	34D9
FRSUB0	Force Subtract on multiply.	36M3
FSKIP0	Output from the Skip flip-flop.	33F5
FSNGL1	Single flip-flop from Display Controller.	26H3
FSYN1	Output from the Sync flip-flop.	25J9
FTIT0	Clock stop from test aid.	33J1
FUT1	Utility flip-flop.	34B9
FWAIT0	Active when the Processor is in the Wait state.	34C9
FXPBY0	Exetended Processor Memory Busy flip-flop.	27N7

MNEMONICS	MEANING	SCHEMATIC LOCATION
GABB1	'A' or 'B', but not both sources negative	29B4
GATN1	Gated Attention.	31G9
GB00-150	Gated B Bus. The output from the Shifter/Latch circuit to the ALU.	20A9-20S9
GDAT0	Gates S Bus onto D Bus	25D5
GFLR121	Gated Flag Register Bit 12.	36F3
GLOAD1	Load Micro-operation and RD151 Decoded.	18B9
GMDR000	Gated Memory Data Register Bit 0.	24N9
GPSEL1	Gated Processor selected.	10H4
GRX130	Gated RX1 or RX3 format user instruction decoded.	8N9
HALT0	Signal from MAC preventing the setting of the processor Selected flip-flop.	27J1
HW0	Halfword I/O Test line from the active device.	33K1
ICLK1	Buffered Processor Clock used primarily in I/O timing.	25K1
ILOC1	Increment Location Counter.	35E9
IMAR1	Increment Memory Address Register	35D9
IMCMD0	Immediate or Command micro-instruction decoded.	14F9
INIT1	Output from the system Initialize switch.	33C9
INH0	Inhibit, used for write memory timing.	27C9
IR001-071	Instruction Register Bits 0 through 7. Operation Code portion of a user instruction.	A9-8F9
IR031-111	The outputs from the YD field of the Instruction Register.	29N5-29N7
IR1	Instruction Read decoded from a micro-instruction.	35H2
IRG1	Second Clock of Instruction Read. Use to load Memory Data Register to the YD portion of the Instruction Register.	35J9
IR121-151	The outputs from the YS portion of the Instruction Register.	29L1-29L4
ISTOP0	I/O Processor Clock Stop. Active during I/O Transfer, keeps ROM Data from Changing.	25R9
JALARM	Prepares the Alarm Register to jam to the B-Bus with its contents when a Load PSW is specified.	34E9
JARLB1	Force ARL to be the second source during Multiply.	24B9

MNEMONICS	MEANING	SCHEMATIC LOCATION
LA0	Load display Byte A, to Display 2 Bits 8:15.	26J7
LAR1	Load Arithmetic Register Control line.	14M9
LARH120:150	Data Inputs to the AR High	10E3
LARH0	Load Arithmetic Register High.	24C9
LARL0	Load Arithmetic Register Low.	24D9
LARX0	Load the extended portion of the Arithmetic Register.	24D9
LB0	Load display byte B, to Display 2 Bits 0:7.	26J7
LCNTR1	Load the Counter.	35M9
LD100	Load I/O micro-instruction decoder.	30S4
LIO1	I/O operation in progress.	15G9
LFLR0	Load the Flag Register.	35K9
LCC0	Load the Condition Code Register.	34G9
LINH0	Fast Memory Timing INH0.	27N9
LLOC0	Load the Location Counter.	14L9
LMAR0	Load the Memory Address Register from the S Bus.	14L9
LMAS0	Load the Memory Address Slave Register.	27E9
LMDR1	Load the Memory Data Register from the S Bus.	14L9
LOAD0	Any Load micro-instruction decoded.	14B9
LPSWL1	Load Program Status Word Low Order Bits 16 through 31.	31F9
LRAR0	Load ROM Address Register. Enables the loading of the RAR.	33E9
LR0	Late Read, used for read memory timing.	27E9
LSRH1	Load Shift Register High	35L9
LSRL1	Load Shift Register Low	35L9
LYSI0	Lead YS portion of the Instruction Register from the S Bus.	14L9
MA000:140	Output from the Memory Address Register Bits 0:15.	Sheet 16
MAR001:151	Output from the Memory Address Register Bits 0:15.	Sheet 16
MCI0	Multiply Carry into the Shift Register.	36G8
MD0	Multiply or divide operation decoded.	36L3
MD000:150	Memory Data Bus to the memory system.	Sheets 18-19
MDR000:070	Outputs from the Memory Data Register.	Sheets 18-19

MNEMONICS	MEANING	SCHEMATIC LOCATION
MDS20	Multiply operation, disable the second source.	24R9
MEGRL00	Memory enable General Register Low, Set 0.	11D8
MEGRLF0	Memory enable General Register Low, Set F.	11N8
MEGRH00	Memory enable General Register High, Set 0.	11H8
MEGRHF0	Memory enable General Register High, Set F.	11R8
MEM1	Memory Operation decoded from micro-instruction.	35E9
MEMS0	Memory enable for the micro-register stacks.	11B8
MEXR00	Memory enable for the Extended Registers Set 0.	11M8
MEXRF0	Memory enable for the Extended Register Set F.	11R8
M1	The M input to the ALU decoded.	14J9
MMAL1	Machine Malfunction-Parity Error or Power Failure	28L6
MW1	Memory Write Decode from Micro-instruction.	35A9
NORM0	Floating point number not normalized.	23F9
OSC1	Output from the System Clock Oscillator.	32C1
OVAS1	Overflow enable function on an add or subtract.	29G6
OVA1	Overflow enable function on an add.	29G7
OVS1	Overflow enable function on a subtract.	29G5
PO0	Phase 0 of Calculate Address micro-instruction.	8G9
P11	Phase 1 of a Calculate Address micro-instruction.	8N9
P20	Phase 2 of a Calculate Address micro-instruction.	8M9
PBY1	Local Processor memory Busy or Extended Processor Memory Busy	29B6
PERR0	Parity error on Memory Data Bus.	28B6
PFDT0	Power Failure detected.	32D9
POFF0	Output from the On/Off Power switch controlling system power.	32B7
POWDN0	Power is down. Resets the SCLR relay.	32J7
PRIV0	Privileged instruction decoded from DROM.	34G9
PRTECT0	Memory Protected and Processor is doing memory write.	35A9
PSEL1	Processor selected for Memory Bus.	18B3

MNEMONICS	MEANING	SCHEMATIC LOCATION
PSW161-231	Program Status Word Bit 16 through 23.	31A8-31E8
PSW271	Program Status Word Bit 27.	31D4
RAR050:150	The outputs from the RAR.	Sheet 5
RARSTP0	ROM Address Register clock stop.	8F9
RD000:230	ROM Data Register Bit through 23.	Sheet 7
READ1	Register stack read time.	11N1
REQ0	Request from the Direct Memory Access Port.	27K1
RR1	Register to Register format user instruction decoder.	9N3
RSTOP0	ROM Stop. Stops CKRD0 when active.	33F9
SA1	General Register stacks addressing signal.	12A4
SB1	General Register stacks addressing signal.	12E1
SC1	General Register stacks addressing signal.	12E1
SCHRY1	Shifted Carry. Enables the setting of the carry flag on either a shift right or shift left.	29D4
SCLR0	System Clear. Signal used to initialize the system on a power up or power down.	32A5
SD1	General Register stacks addressing signal.	12H1
SD001:071	Status and Data Bus to the Display Console.	26R1-26R7
SDSTOP0	Set Destination Stop Clock during Repeat Mode Micro-instruction.	34M9
SELA1	Source address line for A Bus.	24J9
SELB1	Source address line for A Bus.	24G9
SEQ01	S Bus equals zero.	22N8
SGN10	Second source equal to one.	24L9
SGN20	Second source equal to two.	24K9
SGNMDR0	Sign bit of Memory Data Register.	24K9
SHCLK0	32 bit Shift Register Clock	36A9
SHL1	Shift Left. Conditions the B Bus Shifter to shift data left one place.	16N9
SHR1	Shift Right. Conditions the B Bus Shifter to shift data right one place.	16N9

MNEMONICS	MEANING	SCHEMATIC LOCATION
SHORT1	32 Bit RX instruction being executed	8R9
SHI0	Input high data switches	26J6
SLO0	Input low data switches	26J6
SMALF1	A Machine Malfunction is pending.	31H9
SMPY0	Set multiply flip-flop	36A1
SNGL1	Single. Test Point to the micro-program indicating status of the Control Console.	31G9
S01:S31	S01 The S0 input to the ALU decoded. S11 The S1 input to the ALU decoded. S20 The S2 input to the ALU decoded. S31 The S3 input to the ALU decoded.	14G9:14
S001:S151	S Bus. Outputs from the ALU.	Sheets 21-22
SRA050:150	The Set ROM Address lines to the RAR.	5F4:5F9
SRD000:230	The outputs from the ROM used to load the ROM Data Register.	6S2-6S9
SRH091:111	Shift Register High bits 9 through 11.	23D9
SRHS01	Shift Register High Control lines.	36E7
SRHS11	Shift Register High Control line.	36E7
SRLCI1	Shift Register Low Carry In.	36L9
SRLS01	Shift Register Low Control line.	36C7
SRLS11	Shift Register Low Control line.	36D7
SR0	Status Request Control line.	25D6
SRSTOP0	Set ROM Clock Stop.	34L9
SSGL1	Singl Switch from Display Panel	26A2
SUB1	Subtract micro-instruction decoded.	14H9
SV0	Set Overflow flag. Direct sets the Overflow flag when False Sync is detected.	25L1
SYN0	Sync response from external device controller.	26J4
TBRCH1	True Branch	31S8
ULOCH1	Unload Location Counter high	14N9
ULOC1	Unload Location Counter.	35R9
UMAR1	Unload the Memory Address Register to the B Bus.	35M9

MNEMONICS	MEANING	SCHEMATIC LOCATION
UMDR0	Unload the Memory Data Register to the B Bus.	24F9
UMDR1	Unload the Memor Data Regist to the B Bus.	35M9
USRH1	Unload the Shift Register High.	23M1
USRLOC1	Unload Shift Register Low.	22M2
USRLOC1	Unload Shift Register or Location Counter.	14N9
WAIT	Controls the state of the Wait indicator on the Control Console.	26J3
WRT0	Memory Bus signal indicating that a Processor memory write is taking place.	27H9
WO	Memory Timing signal defining write time.	27B9
XB00:30	Extended B Bus 0 through 3.	9N9
XMA120:150	Extended Memory Address Register Bits 12 through 15	10K5
XMDR00:30	Extended Memory Data Register Bits 0 through 3.	9N9
XMEM0	Extended Memory operation taking place. Comes from MAC or DMABC.	9N9
XS01:31	Extended S Bus Bits 0 through 3.	10N9
YDM1	YD minus one. Decrement YD.	29G8
YDP1	YD plue one. Increment YD.	29G7
YSH1	General Register source address line.	12L1
YLS1	General Register stack source address line.	12H1
YA121:YS151	User Source Bus for loading YS field of Instruction Register and for loading the micro-register stack.	29K1-29K5

Appendix 1.
Multiply-Divide Examples

This appendix to 01-079A21 shows examples of both Multiply and Divide operations indicating the state of the various busses and registers during each clock of the operation. These are examples of the operands used in the test programs.

TABLE A1-1. SIGNED MULTIPLY (MPY) EXAMPLE WITH THE FOLLOWING OPERANDS:

Multiplier = X'FFFF'
Multiplicand = X'1111'

Prior to execution of the Multiply micro-instruction the following registers have been loaded by the micro-program as follows:

MDR = X'1111'
ARL = X'2222'
CARRY Flag = 0

		SRX 14	SRX 15		SRH				SRL				SRL 16
	1	0	0	-	0	0	0	0	F	F	F	F	0
	2			B	0	0	0	0					
				GB	0	0	0	0					
		1	1	S	E	E	E	F	F	F	F	F	1
				SRH	F	7	7	7	F	F	F	F	1
	3			B	F	7	7	7					
				GB	F	B	B	B					
		1	1	S	F	B	B	B	F	F	F	F	1
		1	1	SRH	F	D	D	D	F	F	F	F	1
	4			B	F	D	D	D					
				GB	F	E	E	E					
		1	1	S	F	E	E	E	7	F	F	F	1
		1	1	SRH	F	F	7	7	B	F	F	F	1
	5			B	F	F	7	7					
				GB	F	F	B	B					
		1	1	S	F	F	B	B	D	F	F	F	1
		1	1	SRH	F	F	D	D	E	F	F	F	1
	6			B	F	F	D	D					
				GB	F	F	E	E					
		1	1	S	F	F	E	E	7	7	F	F	1
		1	1	SRH	F	F	F	7	B	B	F	F	1
	7			B	F	F	F	7					
				GB	F	F	F	B					
		1	1	S	F	F	F	B	D	D	F	F	1
		1	1	SRH	F	F	F	D	E	E	F	F	1
	8			B	F	F	F	D					
				GB	F	F	F	E					
		1	1	S	F	F	F	E	7	7	7	F	1
		1	1	SRH	F	F	F	F	B	B	B	F	1
	9			B	F	F	F	F					
				GB	F	F	F	F					
		1	1	S	F	F	F	F	D	D	D	F	1
		1	1	SRH	F	F	F	F	E	E	E	F	1
L SRH, SRH, SR	10			B	F	F	F	F	E	E	E	F	
				GB	F	F	F	F					
				S	F	F	F	F					
RESULT				SRH	F	F	F	F					

TABLE A1-2. SIGNED MULTIPLY (MPY) EXAMPLE WITH THE FOLLOWING OPERANDS:

Multiplier = X'1111'
Multiplicand = X'FFFF'

Prior to execution of the Multiply micro-instruction the following registers have been loaded by the micro-program as follows:

MDR = X'FFFF'
ARL = X'FFFE'
CARRY Flag = 1

		SRX 14	SRX 15		SRH				SRL				SRL 16
	1	0	0	-	0	0	0	0	1	1	1	1	0
				B	0	0	0	0					
				GB	0	0	0	0					
				S	F	F	F	F	8	8	8	8	1
	2	1	1	SRH	F	F	F	F	C	4	4	4	0
				B	F	F	F	F					
				GB	F	F	F	F					
		1	1	S	F	F	F	F	E	2	2	2	0
	3	1	1	SRH	F	F	F	F	F	1	1	1	0
				B	F	F	F	F					
				GB	F	F	F	F					
	4	1	1	S	F	F	F	E	7	8	8	8	1
		1	1	SRH	F	F	F	F	B	C	4	4	0
				B	F	F	F	F					
	5			GB	F	F	F	F					
		1	1	S	F	F	F	F	D	E	2	2	0
		1	1	SRH	F	F	F	F	E	F	1	1	0
				B	F	F	F	F					
				GB	F	F	F	F					
	6	1	1	S	F	F	F	E	7	7	8	8	1
		1	1	SRH	F	F	F	F	B	B	C	4	0
				B	F	F	F	F					
				GB	F	F	F	F					
	7	1	1	S	F	F	F	F	D	D	E	2	0
		1	1	SRH	F	F	F	F	E	E	F	1	0
				B	F	F	F	F					
				GB	F	F	F	F					
	8	1	1	S	F	F	F	E	7	7	7	8	1
		1	1	SRH	F	F	F	F	B	B	B	C	0
				B	F	F	F	F					
				GB	F	F	F	F					
	9	1	1	S	F	F	F	F	D	D	D	E	0
		1	1	SRH	F	F	F	F	E	E	E	F	0
L SRH, SRH, SR	10			B	F	F	F	F	E	E	E	F	-
				GB	F	F	F	F					
				S	F	F	F	F					
RESULT				SRH	F	F	F	F					

TABLE A1-3. UNSIGNED MULTIPLY (UMPY) EXAMPLE WITH THE FOLLOWING OPERANDS:

Multiplier = X'FFFF'
Multiplicand = X'1111'

Prior to execution of the Multiply micro-instruction the following registers have been loaded by the micro-program as follows:

MDR = X'1111'
ARL = X'2222'
CARRY Flag = 0

		SRX 14	SRX 15		SRH				SRL				SRL 16
	1	0	0	-	0	0	0	0	F	F	F	F	0
				B	0	0	0	0					
				GB	0	0	0	0					
				S	E	E	E	F	F	F	F	F	1
	2	1	1	SRH	F	7	7	7	F	F	F	F	1
				B	F	7	7	7					
	3			GB	F	B	B	B					
				S	F	B	B	B	F	F	F	F	1
		1	1	SRH	F	D	D	D	F	F	F	F	1
				B	F	D	D	D					
				GB	F	E	E	E					
	4			S	F	E	E	E	7	F	F	F	1
		1	1	SRH	F	F	7	7	B	F	F	F	1
				B	F	F	7	7					
				GB	F	F	B	B					
	5			S	F	F	B	B	D	F	F	F	1
		1	1	SRH	F	F	D	D	E	F	F	F	1
				B	F	F	D	D					
				GB	F	F	E	E					
	6			S	F	F	E	E	7	7	F	F	1
		1	1	SRH	F	F	F	7	B	B	F	F	1
				B	F	F	F	7					
				GB	F	F	F	B					
	7			S	F	F	F	B	B	B	F	F	1
		1	1	SRH	F	F	F	D	D	D	F	F	1
				B	F	F	F	D					
				GB	F	F	F	E					
	8			S	F	F	F	E	E	E	F	F	
		1	1	SRH	F	F	F	F	B	B	B	F	
				B	F	F	F	F					
				GB	F	F	F	F					
	9			S	F	F	F	F	D	D	D	F	1
		1	1	SRH	F	F	F	F	E	E	E	F	
A SRH, SRH, MOR, SR	10			B	F	F	F	F	E	E	E	F	
				GB	F	F	F	F					
				S	1	1	1	0					
RESULT				SRH	1	1	1	0					

TABLE A1-4. SIGNED MULTIPLY (MPY) EXAMPLE WITH THE FOLLOWING OPERANDS:

Multiplier = X'7FFF'
Multiplicand = X'FFFF'

Prior to execution of the Multiply micro-instruction the following registers have been loaded by the micro-program as follows:

MDR = X'FFFF'
ARL = X'FFFE'
CARRY Flag = 1

		SRH 14	SRH 15		SRH				SRL				SRL 16
	1	0	0	0	0	0	0	0	7	F	F	F	0
	2			B	0	0	0	0					
				GB	0	0	0	0					1
				S	0	0	0	1	B	F	F	F	1
		1	1	SRH	8	0	0	0	5	F	F	F	1
	3			B	8	0	0	0					
				GB	C	0	0	0					
				S	C	0	0	0	2	F	F	F	1
		1	1	SRH	E	0	0	0	1	7	F	F	1
				B	E	0	0	0					
	4			GB	F	0	0	0					
				S	F	0	0	0	0	B	F	F	1
		1	1	SRH	F	8	0	0	0	5	F	F	1
				B	F	8	0	0					
				GB	F	C	0	0					
	5			S	F	C	0	0	0	2	F	F	1
		1	1	SRH	F	E	0	0	0	1	7	F	1
				B	F	E	0	0					
				GB	F	F	0	0					
	6			S	F	F	0	0	0	0	B	F	1
		1	1	SRH	F	F	8	0	0	0	5	F	1
				B	F	F	8	0					
				GB	F	F	C	0					
	7			S	F	F	C	0	0	0	2	F	1
		1	1	SRH	F	F	E	0	0	0	1	7	1
				B	F	F	E	0					
				GB	F	F	F	0					
	8			S	F	F	F	0	0	0	0	B	1
		1	1	SRH	F	F	F	8	0	0	0	5	1
				B	F	F	F	8					
				GB	F	F	F	C					
	9			S	F	F	F	C	0	0	0	2	1
		1	1	SRH	F	F	F	E	8	0	0	1	0
L SRH, SRH, SR	10			B	F	F	F	F	8	0	0	1	-
SIGN				GB	F	F	F	F					
				S	F	F	F	F					
RESULT				SRH	F	F	F	F					

TABLE A1-5. UNSIGNED MULTIPLY (UMPY) EXAMPLE WITH THE FOLLOWING OPERANDS:

Multiplier = X'FFFF'
Multiplicand = X'FFFF'

Prior to execution of the Multiply micro-instruction the following registers have been loaded by the micro-program as follows:

MDR = X'FFFF'
ARL = X'FFFE'
CARRY Flag = 1

		SRX 14	SRX 15		SRH				SRL				SRL 16
	1	0	0	-	0	0	0	0	F	F	F	F	0
				B	0	0	0	0					
				GB	0	0	0	0					
				S	0	0	0	1	F	F	F	F	1
	2	1	1	SRH	8	0	0	0	7	F	F	F	1
				B	8	0	0	0					
				GB	C	0	0	0					
				S	C	0	0	0	3	F	F	F	1
	3	1	1	SRH	E	0	0	0	1	F	F	F	1
				B	E	0	0	0					
				GB	F	0	0	0					
				S	F	0	0	0	0	F	F	F	1
	4	1	1	SRH	F	8	0	0	0	7	F	F	1
				B	F	8	0	0					
				GB	F	C	0	0					
				S	F	C	0	0	0	3	F	F	1
	5	1	1	SRH	F	E	0	0	0	1	F	F	1
				B	F	E	0	0					
				GB	F	F	0	0					
				S	F	F	0	0	0	0	F	F	1
	6	1	1	SRH	F	F	8	0	0	0	7	F	1
				B	F	F	8	0					
				GB	F	F	C	0					
				S	F	F	C	0	0	0	3	F	1
	7	1	1	SRH	F	F	E	0	0	0	1	F	1
				B	F	F	E	0					
				GB	F	F	F	0					
				S	F	F	F	0	0	0	0	F	1
	8	1	1	SRH	F	F	F	8	0	0	0	7	1
				B	F	F	F	8					
				GB	F	F	F	C					
				S	F	F	F	C	0	0	0	3	1
	9	1	1	SRH	F	F	F	E	0	0	0	1	1
A SRH, SRH, MDR, SR	10			B	F	F	F	E					
				GB	F	F	F	F					
				S	F	F	F	E	0	0	0	1	-
RESULT				SRH	F	F	F	E					

TABLE A1-6. SIGNED MULTIPLY (MPY) EXAMPLE WITH THE FOLLOWING OPERANDS:

Multiplier = X'8000'
Multiplicand = X'8000'

Prior to execution of the Multiply micro-instruction the following registers have been loaded by the micro-program as follows:

MDR = X'8000'
ARL = X'0000'
CARRY Flag = 1

		SRX 14	SRX 15		SRH				SRL				SRL 16
	1	0	0	-	0	0	0	0	8	0	0	0	0
				B	0	0	0	0					
				GB	0	0	0	0					
	2			S	0	0	0	0	4	0	0	0	0
		0	0	SRH	0	0	0	0	2	0	0	0	0
				B	0	0	0	0					
				GB	0	0	0	0					
	3	0	0	S	0	0	0	0	1	0	0	0	0
		0	0	SRH	0	0	0	0	0	8	0	0	0
				B	0	0	0	0					
				GB	0	0	0	0					
	4	0	0	S	0	0	0	0	0	4	0	0	0
		0	0	SRH	0	0	0	0	0	2	0	0	0
				B	0	0	0	0					
				GB	0	0	0	0					
	5	0	0	S	0	0	0	0	0	1	0	0	0
		0	0	SRH	0	0	0	0	0	0	8	0	0
				B	0	0	0	0					
				GB	0	0	0	0					
	6	0	0	S	0	0	0	0	0	0	4	0	0
		0	0	SRH	0	0	0	0	0	0	2	0	0
				B	0	0	0	0					
				GB	0	0	0	0					
	7	0	0	S	0	0	0	0	0	0	1	0	0
		0	0	SRH	0	0	0	0	0	0	0	8	0
				B	0	0	0	0					
				GB	0	0	0	0					
	8	0	0	S	0	0	0	0	0	0	0	4	0
		0	0	SRH	0	0	0	0	0	0	0	2	0
				B	0	0	0	0					
				GB	0	0	0	0					
	9	1	1	S	0	0	0	0	0	0	0	1	0
				SRH	8	0	0	0	0	0	0	0	1
L SRH,SRH,SR	10			B	4	0	0	0	0	0	0	0	0
				GB	4	0	0	0					
				S	4	0	0	0					
RESULT				SRH	4	0	0	0					

TABLE A1-7. SIGNED MULTIPLY (MPY) EXAMPLE WITH THE FOLLOWING OPERANDS:

Multiplier = X'FFFF'
Multiplicand = X'8000'

Prior to execution of the Multiply micro-instruction the following registers have been loaded by the micro-program as follows:

MDR = X'8000'
ARL = X'000'
CARRY Flag = 1

		SRX 14	SRX 15		SRH				SRL				SRL 16
	1	0	0	-	0	0	0	0	F	F	F	F	0
				B	0	0	0	0					
				GB	0	0	0	0					
				S	8	0	0	0	7	F	F	F	1
	2	0	0	SRH	4	0	0	0	3	F	F	F	1
				B	4	0	0	0					
				GB	2	0	0	0					
	3	0	0	S	2	0	0	0	1	F	F	F	1
		0	0	SRH	1	0	0	0	0	F	F	F	1
				B	1	0	0	0					
				GB	0	8	0	0					
	4	0	0	S	0	0	0	0	0	7	F	F	1
		0	0	SRH	0	4	0	0	0	3	F	F	1
				B	0	4	0	0					
				GB	0	2	0	0					
	5			S	0	2	0	0	0	1	F	F	1
		0	0	SRH	0	1	0	0	0	0	F	F	1
				B	0	1	0	0					
				GB	0	0	8	0					
	6	0	0	S	0	0	8	0	0	0	7	F	1
				SRH	0	0	4	0	0	0	3	F	1
				B	0	0	4	0					
				GB	0	0	2	0					
	7	0	0	S	0	0	2	0	0	0	1	F	1
		0	0	SRH	0	0	1	0	0	0	0	F	1
				B	0	0	1	0					
				GB	0	0	0	8					
	8	0	0	S	0	0	0	8	0	0	0	7	1
		0	0	SRH	0	0	0	4	0	0	0	3	1
				B	0	0	0	4					
				GB	0	0	0	2					
	9	0	0	S	0	0	0	2	0	0	0	1	1
		0	0	SRH	0	0	0	1	8	0	0	0	0
L SRH,SRH,SR	10			B	0	0	0	0	8	0	0	0	-
				GB	0	0	0	0					
				S	0	0	0	0					
RESULT				SRH	0	0	0	0					

TABLE A1-8. UNSIGNED MULTIPLY (UMPY) EXAMPLE WITH THE FOLLOWING OPERANDS:

Multiplier = X'8000'
Multiplicand = X'FFFF'

Prior to execution of the Multiply micro-instruction the following registers have been loaded by the micro-program as follows:

MDR = X'FFFF' A = FFFF (UMPY) D = 4X3
ARL = X'FFFE' B = 8000
CARRY Flag = 1 D = 7FFFF 8000

	SRX 14	SRX 15		SRH				SRL				SRL 16
1	0	0	-	0	0	0	0	8	0	0	0	0
			B	0	0	0	0					
			GB	0	0	0	0					
			S	0	0	0	0	4	0	0	0	0
2	0	0	SRH	0	0	0	0	2	0	0	0	0
			B	0	0	0	0					
			GB	0	0	0	0					
			S	0	0	0	0	1	0	0	0	0
3	0	0	SRH	0	0	0	0	0	8	0	0	0
			B	0	0	0	0					
			GB	0	0	0	0					
4			S	0	0	0	0	0	4	0	0	0
	0	0	SRH	0	0	0	0	0	2	0	0	0
			B	0	0	0	0					
			GB	0	0	0	0					
5			S	0	0	0	0	0	1	0	0	0
	0	0	SRH	0	0	0	0	0	0	8	0	0
			B	0	0	0	0					
			GB	0	0	0	0					
6			S	0	0	0	0	0	0	4	0	0
	0	0	SRH	0	0	0	0	0	0	2	0	0
			B	0	0	0	0					
			GB	0	0	0	0					
7			S	0	0	0	0	0	0	1	0	
	0	0	SRH	0	0	0	0	0	0	0	8	0
			B	0	0	0	0					
			GB	0	0	0	0					
			S	0	0	0	0	0	0	0	4	0
8	0	0	SRH	0	0	0	0	0	0	0	2	0
			B	0	0	0	0					
			GB	0	0	0	0					
			S	0	0	0	2	0	0	0	1	0
9	1	1	SRH	0	0	0	1	8	0	0	0	1
10			B	0	0	0	1					
A SRH, SRH, MDR SR			GB	8	0	0	0					
			S	7	F	F	F	8	0	0	0	
RESULT			SRH	7	F	F	F					

TABLE A1-9. DIVIDE EXAMPLE WITH THE FOLLOWING OPERANDS:

Divisor = X'7FFF'
Dividend = X'3FFF 7FFF'

Prior to execution of the Divide micro-instruction the following registers have been loaded by the micro-program as follows:

SRH = X'3FFF'
SRL = X'7FFF'
ARL = X'8000'

CLOCK	CARRY SAVE FROM ALU			SRL
1		B	3FFF	
		GB	7FFE	
	C=0	S	FFFE	
		SRH	7FFE	FFFE
2		B	7FFE	
		GB	FFFD	
	C=1	S	7FFD	
		SRH	7FFD	FFFD
3		B	7FFD	
		GB	FFFB	
	C=1	S	7FFB	
		SRH	7FFB	FFFB
4		B	7FFB	
		GB	FFF7	
	C=1	S	7FF7	
		SRH	7FF7	FFF7
5		B	7FF7	
		GB	FFEF	
	C=1	S	7FEF	
		SRH	7FEF	FFEF
6		B	7FEF	
		GB	FFDF	
	C=1	S	7FDF	
		SRH	7FDF	FFDF
7		B	7FDF	
		GB	FFBF	
	C=1	S	7FBF	
		SRH	7FBF	FFBF
8		B	7FBF	
		GB	FF7F	
	C=1	S	7F7F	
		SRH	7F7F	FF7F
9		B	7F7F	
		GB	FEFF	
	C=1	S	7EFF	
		SRH	7EFF	FEFF
10		B	7EFF	
		GB	FDFF	
	C=1	S	7DFF	
		SRH	7DFF	FDFF
11		B	7DFF	
		GB	FBFF	
	C=1	S	7BFF	
		SRH	7BFF	FBFF

CLOCK	CARRY SAVE FROM ALU			SRL
12	C=1	B GB S SRH	7BFF F7FF 77FF 77FF	F7FF
13	C=1	B GB S SRH	77FF EFFF 6FFF 6FFF	EFFF
14	C=1	B GB S SRH	6FFF DFFF 5FFF 5FFF	DFFF
15	C=1	B GB S SRH	5FFF BFFF 3FFF 3FFF	BFFF
16	C=0	B GB S SRH	3FFF 7FFF FFFF 7FFF	7FFE

Legend:

B	B-Bus
GB	Gated B Bus
S	S-Bus
SRH	Shift Register High
SRL	Shift Register Low
SRX	Extension to Shift Register High

MEMORY ACCESS CONTROLLER

[redacted]

M73 SERIES
MEMORY ACCESS CONTROLLER
INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides the information necessary for installing the 02-349 Direct Memory Access Bus Controller (DMABC) and the 02-348 Memory Access Controller (MAC) in the Model 7/32 or 7/32 C Processor system. The DMABC is complete on one 35-528 printed circuit board and the MAC is complete on one 35-527 printed circuit board.

2. PHYSICAL CHARACTERISTICS

Dimensions	(DMABC or MAC)	15 3/4" X 14 7/8"
Weight	(DMABC or MAC)	2 1/2 pounds maximum

3. INSTALLATION

Refer to 01-087A20 7/32 or 01-097A20 7/32 C Installation Specification. Install the MAC or DAMBC using both Installation Specifications. The MAC or DMABC will not be operable unless the Processor is modified for the MAC or DMABC.

3.1 Back Panel Wiring of DMABC or MAC Slot

In Slot 4 of the Processor chassis remove the following strapping between the Terminals on CONN 0.

208	and	222
108	and	221
106	and	121
107	and	122
109	and	123
110	and	127
210	and	134
129	and	135
229	and	136
130	and	137
205	and	228

Also remove the following straps between Slot 4 and Slot 5 of the 0 Connectors

SLOT 4 CONN 0	SLOT 5 CONN 0
206	206
207	207
209	209

In addition, when installing a Memory Access Controller (35-527) into a 7/32 C Processor a wire must be added to the slot containing the MAC to ground the signal PSW111. Specifically, add a wire from 235 to 241 on connector 0 (slot 4).

3.2 Cabling (Figure 1)

The 17-311 and 17-312 cables are always required for a DMABC or MAC equipped system.

The 17-311 cable connects between CONN 2 of the MAC and CONN 2 of the Processor board in Slot 7 (CPU-A).

The 17-312 cable is a 10 inch cable that connects between CONN 1, Slot 4 of the CPU back panel to CONN 0 and CONN 1 of Slot 7 or Slot 3 on the Expansion back panel of the Processor chassis. If more than four memory modules exist in the local memory this cable must be installed in Slot 3 of the Expansion back panel. Prior to installing this cable, the Memory Bus must be cut between the slot excepting the cable and the next higher slot.

The Memory Bus on CONN 1 must be cut when installing a DMABC or a MAC. The back panel pins involved are:

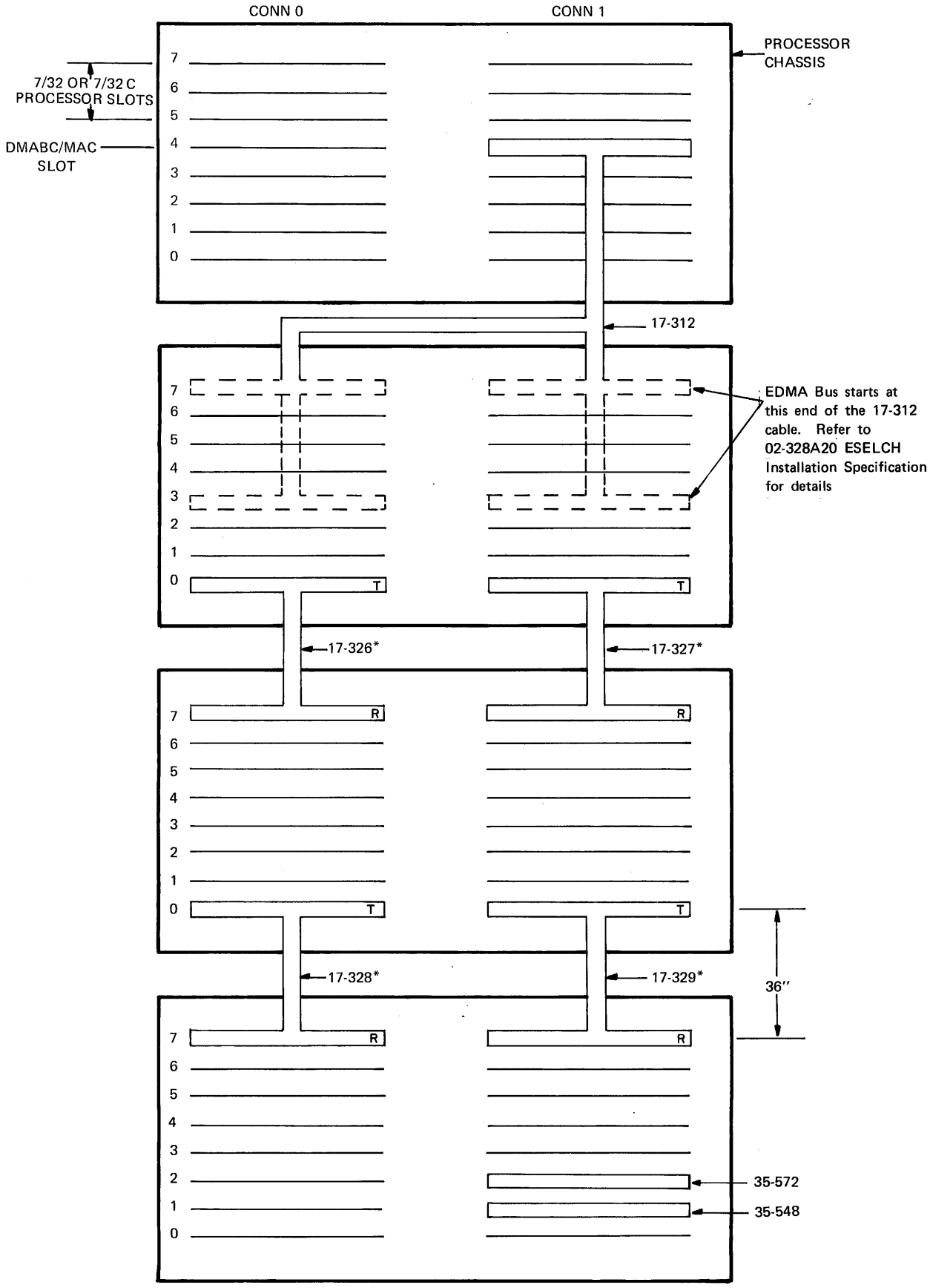
DESIGNATION	CONN 1	DESIGNATION	CONN 1
MD160	237		
MD150	137	WRT0	127
MD140	236	MS000	210
MD130	136	MS010	109
MD120	235	MS020	209
MD110	135	MS030	108
MD100	234	MS040	208
MD090	134	MS050	107
MD080	233	MS060	207
MD070	133	MS070	106
MD060	232	MS080	206
MD050	132	MS090	105
MD040	231	MS100	205
MD030	131	MS110	104
MD020	230	MS120	204
MD010	130	MS130	103
MD000	229	MS140	203
EXVT	129	MS150	102
VT	228	MS160	202

If an ESELCH is installed in Slot 4 or 6 in the Expansion back panel of the twin chassis, the Memory Bus must be cut on CONN 1 between Slot 7 of the Expansion back panel and Slot 0 of the Processor back panel. If there is an ESELCH in Slot 0 or 2 but not in Slot 4 or 6, the Memory Bus must be cut on CONN 1 between Slots 3 and 4 of the Expansion back panel. This configuration must be used if local memory consists of more than four memory modules. See 02-328A20 ESELCH Installation Specification for further information on installation of the ESELCH.

The 17-326, 17-327, 17-328 and 17-329 cables are required as a function of the physical configuration of the system.

The 17-326 and 17-327 cables are 5 inch cables containing the Input/Output (I/O) and DMA Bus signals for CONN 0 and CONN 1. Their function is to continue the I/O and DMA signals from the bottom slot of one chassis (Slot 0) to the top slot (Slot 7) of an Expansion chassis. The "T" designated connector is the Slot 0 side connection (Figure 1). If only the I/O signals are to be continued, refer to 02-328A20 ESELCH installation specification for information on which cables to use.

The 17-328 and 17-329 cables are 36 inch cables used to extend the DMA Bus only. The maximum length of the DMA Bus is 8 feet. The 17-328 cable is for extending the DMA signals between CONN 0s and the 17-329 cable is for extending the DMA signals between CONN 1s. The "T" designated connector of the 17-328 cable is the transmitting end of the cable (Figure 1).



*SEE CABLING INFORMATION, PARAGRAPH 3.2.

Figure 1. DMABC and MAC Back Connections

TO INSTALL MAC OR DMABC AND EDMA BUS

A. REMOVE WIRES:

SLOT 4 CPU CHASSIS

208-0400	to	221-0400
108-0400	to	222-0400
106-0400	to	121-0400
107-0400	to	122-0400
109-0400	to	123-0400
110-0400	to	127-0400
210-0400	to	134-0400
129-0400	to	135-0400
229-0400	to	136-0400
130-0400	to	137-0400
205-0400	to	228-0400

B. BETWEEN SLOTS 4 AND 5 REMOVE

206-0400	to	206-0500
207-0400	to	207-0500
209-0400	to	209-0500

C. REMOVE FOLLOWING MEMORY BUS WIRES BETWEEN SLOT RECEIVING 17-312 CABLE (SLOT 7 or 3) AND THE NEXT HIGHER SLOT

X = Slot 7 or 3
Y = Next higher slot

228-0X01	thru	237-0Y01
130-0X01	thru	137-0Y01
102-0X01	thru	109-0Y01
202-0X01	thru	210-0Y01
127-0X01	to	129-0401

D. TO INSTALL 17-312 CABLE TO SLOT 7, ALSO REMOVE FOLLOWING WIRES:

TEMPA		128-0701
TEMPB		227-0701
110-0701	to	127-0701

ADD THE FOLLOWING WIRES

227-0701	to	227-0601
128-0701	to	128-0601

E. ADD WIRES BELOW SLOT THAT RECEIVES 17-312 CABLE.

SLOT 7

129-0701	to	129-0601
129-0601	to	129-0501
129-0501	to	129-0401
129-0401	to	129-0301
129-0301	to	129-0201
129-0201	to	129-0101
129-0101	to	129-0001

SLOT 3

129-0301	to	129-0201
129-0201	to	129-0101
129-0101	to	129-0001

F. FOR EXTENDING EDMA BUS TO EXPANSION CHASSIS WITH 17-326 AND 17-327. OR 17-328 AND 17-329 CABLES

REMOVE WIRES:
TEMPA - 227-0701
TEMPB - 128-0701
110-0701 - 127-0701

ADD 129-0X01 ALL SLOTS
228-0X01 ALL SLOTS
136-0X00 ALL SLOTS
236-0X00 ALL SLOTS
227-0701 to 227-0601
128-0701 to 128-0601

NOTE

For MAC 35-527 (R03 or higher) or DMABC 35-528 (R02 or higher) or either M01 Board, the 17-326 cable must be R02 or higher and the 17-328 cable must be R03 or higher.

G. MODIFY CPU BOARDS PER SECTION 8.2 of 01-087A20.

H. RPC0/TPC0 DAISY CHAIN MODIFICATION

ADD 128-0003 to 105-0104 (CPU Back Panel)

REMOVE
RPC0/TPC0 Jumper (137-237) of CONN 0 in the last DMA (e.g. ESELCH) device to receive RPC0.
Jumper 237-0 of this slot and connector to Pin 128-0 of this same slot and connector.

3.3 Strapping

Strapping is required on the Processor boards when a DMABC or a MAC is installed. Refer to Section 8 of the 01-087A20 Model 7/32 or the 01-097A20 Model 7/32 C Installation Specification for details.

3.4 DMA Bus Terminator

Both ends of the EDMA Bus must be terminated. The DMABC or MAC end of the 17-312 cable is equipped with bus terminators. The far end of the bus must be terminated with the 35-548 printed circuit board at Slot 1 of CONN 1 in the last Expansion back panel which contains the EDMA Bus (Figure 1). The far EN0 of the Bus Hold line (BH0) from memory bank controllers on the DMA Bus must be terminated in the last (lowest priority) memory bank controller. Install the 35-572 Terminator Card at Slot 2 CONN 1 in the last expansion back panel that contains the EDMA Bus. See Figure 1.

3.5 MAC or DMABC Parity Option

To enable the MAC or DMABC parity option, remove, on the Processor back panel, the wire wrap between 200-0400 and 105-0400, and strap PAR on the MAC or DMABC to ground. Refer to 01-087A20, 7/32 or 01-097A20, 7/32 C Installation Specification for further information.

4. MAC SEGMENTATION AND STATUS REGISTER BLOCK ADDRESS STRAPPING

The MAC is strapped at the factory for a 256 byte block starting at address X'00300'. To change the starting address to X'00500' or X'00900' refer to Functional Schematic 02-348D08. The terminal designations shown on the schematic refer to the designations on the apparatus side of the MAC printed circuit board.

5. INSTALLATION CHECKS

To test the relocation and protect feature of the MAC, the 06-160 Memory Access Controller Test should be performed. To test the Selector Channel to the local memory port, the 06-161 Extended Selector Channel Test should be performed. To test the Processor to local memory port of the DMABC, the Series 32 Memory Test Parts 1, 2, and 3 (06-156F01, F02, and F03) should be performed.

M73 SERIES
MEMORY ACCESS CONTROLLER MAINTENANCE SPECIFICATION

1. INTRODUCTION

The 02-349 Model 7/32 and 7/32 C Direct Memory Access Bus Controllers (DMABC) (Figure 1) interface the Multiplexed Direct Memory Access (DMA) Bus to the Local Memory Bus, the local Memory Bus to the Multiplexed DMA Bus, and the 7/32 or 7/32 C Processor to the Local Memory Bus (Figure 1). The DMABC also resolves DMA Bus contention among the DMA Bus devices. The maximum length of the DMA Bus is eight feet and a maximum of seven devices plus the DMABC can be connected to the DMA Bus.

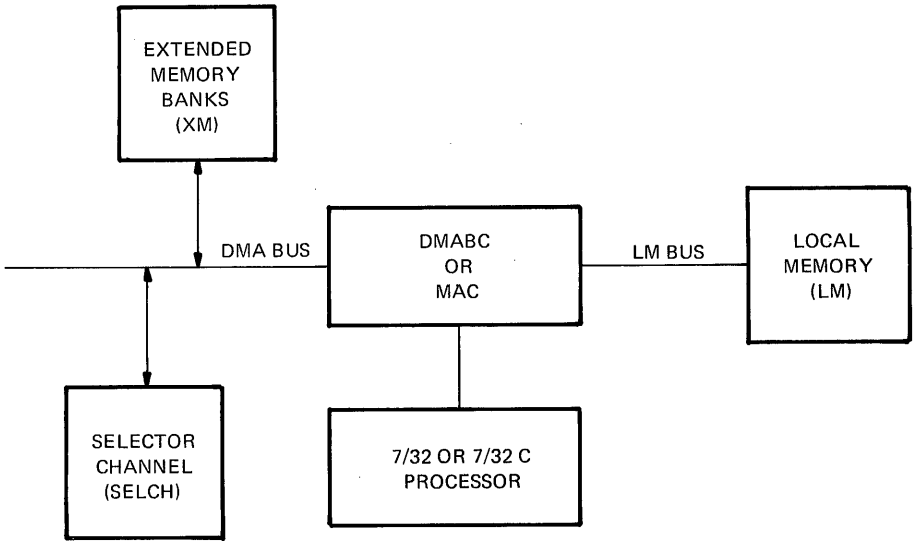


Figure I. DMABC/MAC System block diagram

No programming is required for the DMABC. To the Processor the DMABC is transparent and all memory locations are accessible from the CPU and non-memory devices on the DMA Bus.

The 02-348 Memory Access Controller (MAC) performs the function of the 02-349 DMABC as described previously, but the MAC also provides the memory relocation and protect feature for Processor initiated memory references. The relocation and/or protect is controlled by bits in the Processor's Program Status Word.

If the MAC is disabled, i.e., the relocation and protect is not being used, the MAC is transparent to the Processor. All memory locations are accessible to the Processor except a strappable block of 256 bytes which is reserved for loading the Segmentation Registers (SR) and reading or clearing the interrupt status register which are part of the relocation and protect logic.

If the MAC is enabled, all memory locations are accessible to the Processor. For DMA devices, all memory can be addressed regardless of the state of the MAC.

Both the DMABC and MAC are each complete on a single printed circuit board and each occupies one slot in the chassis.

2. SCOPE

This specification describes the operation of the 02-349 Direct Memory Access Bus Controller and the 02-348 Memory Access Controller.

3. BLOCK DIAGRAM ANALYSIS

Figure 2 is a block diagram of the DMABC and MAC. For the DMABC option, the block "Relocation and Protect" is removed and the memory address bits are strapped to the Memory Bank Decoder and the Latch Register. The memory access through the DMABC and MAC is described first followed by the relocation and protect feature of the MAC. Note that the bus control logic for the DMABC and MAC are identical.

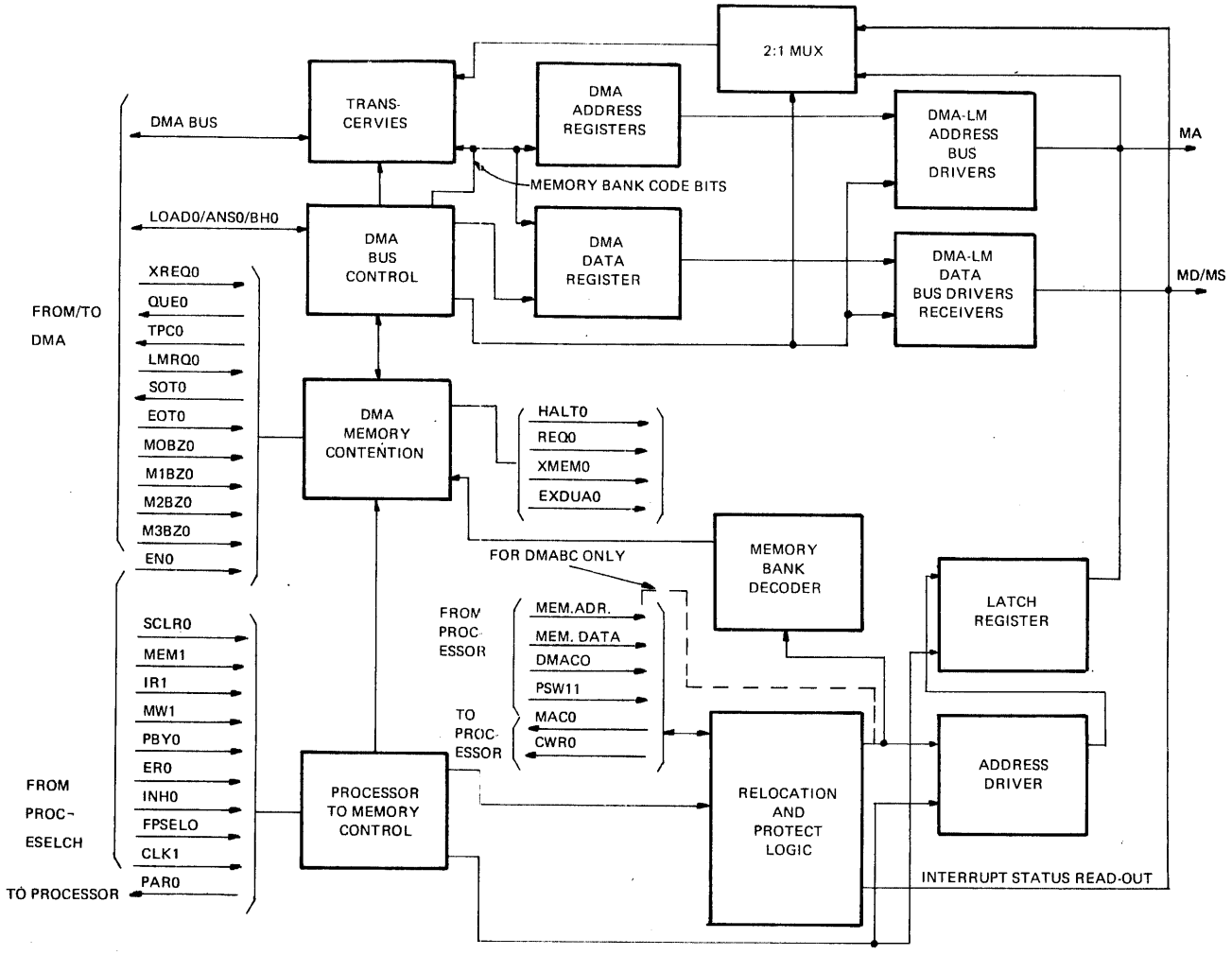


Figure 2. DMABC/MAC Block Diagram

3.1 Processor Memory Access

The DMABC and MAC are synchronized with the Processor by means of the Processor Clock (CLK1). The Processor indicates a pending memory reference on the falling edge of CLK1 by Memory (MEM1), Instruction Read (IR1), or Memory Write (MW1). At the same time the Processor supplies to the DMABC and MAC the 12 most significant memory address bits for the memory reference. In the DMABC, these bits input to the Memory Bank Decoder and the Latch Register. In the MAC, these bits may or may not be modified by the Relocation and Protect, the output of which inputs to the Memory Bank Decoder and the Latch Register. The Memory Bank Decoder decodes one of four 256 Kilobyte banks of memory. The Latch Register stores the 12 memory address bits as supplied by the Processor or modified by the Relocation and Protect, if the local Memory Bus is not busy, and if the Processor is not waiting for a previous memory reference to be completed (EXDUA0 inactive).

The 12 most significant bits of the 19 bit local Memory Address Bus are driven by the address drivers if the Processor is Selected (FPSEL0). If this condition prevails, the Processor drives the remaining seven bits of the memory address. If a DMA Bus device is accessing local memory (FPSEL0 inactive), the address drivers are disabled until such time that the local Memory Bus becomes available to the Processor.

If a local memory bank reference has been decoded, the Processor starts the local memory time on the leading edge of CLK1. For a write to memory, the Processor drives the memory data lines. For a read from local memory, the memory module logic gates the memory data lines when the read-out is available.

If the Memory Bank Decoder recognizes a memory bank other than local, the Latch Register is loaded and the address drivers output the Latch Register as before. The DMABC and MAC activate the Extended Memory line (XMEM0) which prevents the Processor from initiating the local memory timing. In the DMA hierarchy, the Processor has the lowest priority. The DMA memory contention logic allows the Processor memory reference instruction to be executed if the DMA Bus is not being used, no other device wants DMA Bus occupancy (REQ0), the Decoded Memory Bank (M1BZ0, M2BZ0, and M3BZ0) is available and the DMABC or MAC is not busy. The controller would be busy if it had not completed the execution of a previous Processor memory reference. If the controller is not busy it enables the extended data unavailable (EXDUA0) to the Processor during CLK1, and XMEM0 is removed after CLK1. When the Processor is allowed to use the DMA Bus, the DMABC or MAC is made busy and is placed in a Wait state.

For a Processor memory write to Extended Memory (XM), the DMA Bus control enables the 2:1 Multiplexor which is driven from the local memory address and data bus, and selects the address. The contention logic enables the busy line of the memory to be accessed while the bus control enables the driver portion of the transceivers on the DMA Bus. 80 nanoseconds after the address and the read/write information are on the bus, the Load line (LOAD0) is gated for 80 nanoseconds and now the multiplexor selects local Memory Bus data. 80 nanoseconds after the data is on the DMA Bus, LOAD0 is again gated as before. LOAD0 is sent by the addressed device to input the state of the DMA Bus. The controller then removes EXDUA0 and exits from the busy and Wait state.

For a processor memory read from XM, the address, read/write information, and LOAD0 are transmitted as for a write. After this transmission the DMABC or MAC removes itself from the DMA Bus if the bank addressed is a deferred response. For an immediate response bank, the memory controller activates the Bus Hold line (BH0) in which case the DMABC or MAC does not disconnect from DMA Bus. Whether or not the bank is an immediate response byte, the DMA Bus control monitors the memory bank code bits. When a memory outputs data, is also sends with it, two encoded bits that identify the answering bank. 80 nanoseconds after a memory outputs data and code bits, it gates the Answer line (ANS0) for 80 nanoseconds and transmits an End of Transmission (EOT0) signal. If the DMABC or MAC detects its addressed bank answering, on ANS0, it loads the data into the DMA Data Register. The bus control then gates the Data Register contents to the local Memory Data Bus, EXDUA0 is removed and the controller exits from the busy and Wait state.

When the DMABC or MAC enters the Wait state, an internal time-out is initiated that is set for approximately 50 microseconds. If a Processor to XM access is not executed within the time-out, the bus control logic simulates an ANS0. The DMA Data Register contents are then undefined, but they are not gated to the local Memory Data Bus.

3.2 DMA Bus Requests

All DMA Bus connected devices except memories can generate a request to use the bus only if the memory bank to be accessed is not busy. Memory Busy lines (M0BZ0, M1BZ0, M2BZ0 and M3BZ0) connect to all devices including memories. Each line is exclusive to a memory bank. A Request line (XREQ0) common to all devices is activated by the device if the bank that it wants to access is not busy. If the DMABC or MAC contention logic is idle, an active XREQ0 causes the controller to transmit a 30 nanosecond wide QUE0 pulse followed in 60 nanoseconds by a 120 nanosecond wide Transmit Priority Chain pulse (TPC0).

The priority chain line propagates through the DMA devices in daisy chain fashion. The DMABC or MAC generated TPC0 is received at the terminals of the first device on the DMA Bus as a Receive Priority Chain pulse (RPC0). If the receiving device does not have a request queued, it sends a TPC0 to the next device on the bus. However, if the device has a queued request, it will not generate a TPC0 to the next device.

The highest priority request queued device captures RPC0, and becomes selected. This process of setting up and queuing is performed independent of any DMA Bus activity. During and after TPC0 the contention logic monitors DMA Bus activity. If the bus is not busy, a Start of Transmission (SOT0) 60 nanosecond wide pulse is sent to the selected device to grant it the DMA Bus. In the meantime, the contention logic is available to queue another device.

3.3 DMA Device to Memory

After a selected device has been told to start, it outputs 19 bits of address plus read/write information, and lowers the Memory Busy line (MXBZ0) of the bank to be accessed. 80 nanoseconds after the address, it brings the Load line down (LOAD0) for 80 nanoseconds and an End of Transmission signal (EOT) in the case of a memory read. The device disconnects its drivers from the bus and monitors the memory code bits and the ANS0 lead identically as described for a Processor to XM read. In the case of a memory write the device does not send EOT0 with the address LOAD0, but rather after the address LOAD0 it outputs data. 80 nanoseconds after the data output it pulses LOAD0 and EOT0. At the end of the address LOAD0 the device releases its hold on the MXBZ0 line, by which time the accessed memory keeps the line active until it determines that it is available to be accessed again.

When a deferred response memory has data ready for transmission, it must request use of the DMA Bus, get queued, selected, and started. Once started, the memory bank outputs data, two bits for trouble indication and the two coded bits to identify the responding memory. When it gates ANS0, the device that addressed the bank loads the DMA data on receipt of ANS0. The bank also pulses EOT0 which the DMABC or MAC recognizes as a completed DMA Bus transmission.

If local memory is to be accessed by a DMA device, it sends to the DMABC or MAC a Local Memory Request (LMRQ0) when it captures the priority chain pulse. The DMABC or MAC then generates a Request (REQ0) and HALT0 to the Processor which activates the Enable line (EN0). As long as HALT0 remains active the Processor cannot gain access to the local Memory Bus or release EN0. HALT0 is removed by DMABC or MAC when SOT0 is issued to the device. For a DMA initiated read from local memory the contention logic does not relinquish the DMA Bus until the local memory data is transmitted to the bus.

3.4 MAC Relocation and Protect

A block diagram of the relocation and protect feature of the MAC is shown in Figure 3. In the MAC, the memory address on which the bus control logic operates is that derived from the adder.

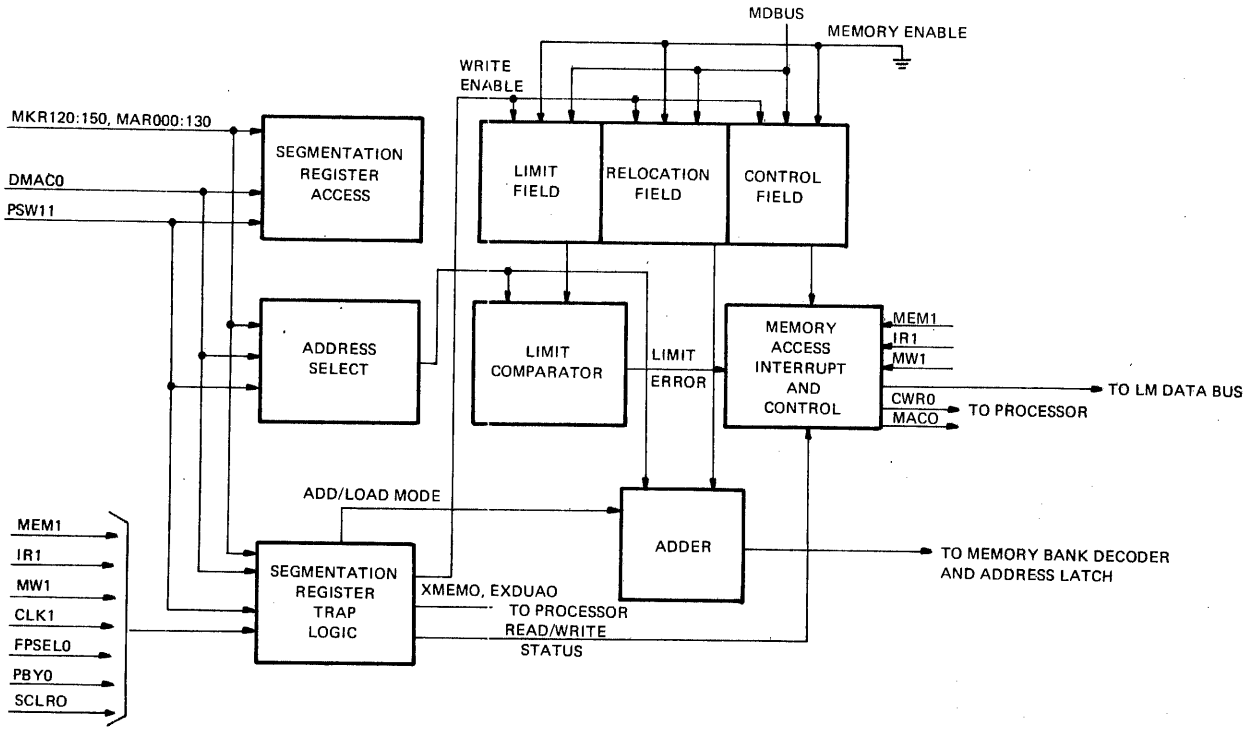


Figure 3. Relocation and Protect Block Diagram

Whether or not the 12 most significant bits of the memory address from the Processor are modified by the adder is controlled by the Disable MAC (DMAC0) signal from the Processor and the state of the System Clear (SCLR0) line. On a power up operation, SCLR0 overrides the state of DMAC0 and all memory reference addresses are sent through the adder unmodified until such time that the Processor accesses the segmentation Registers or the interrupt status register. After this the relocation and protect logic is under control of the DMAC0 line. DMAC0 is a function of the state of Bit 21 of the current Program Status Word (PSW) of the Processor. With Bit 21 low, DMAC0 is low and the MAC is disabled. With Bit 21 high, DMAC0 is high and the relocation and protect feature of the MAC is enabled.

The relocation and protect logic contains 17 hardware registers. Of the 17 registers, 16 are Segmentation Registers and contain relocation protection and control information. The remaining register, Number 17, is the memory access interrupt status register which contains the type of protect violation that has occurred on MAC generated interrupts.

These 17 registers are assigned absolute memory locations. Memory reference instructions are used to load the Segmentation Registers and to read or clear the interrupt status register. The 17 registers can be accessed with memory reference instructions only when the MAC is disabled (DMAC0 is low). The memory locations assigned to the registers is a block of 128 halfwords starting at X'00300', X'00500' or X'00900' - a strappable option. With the MAC disabled memory locations corresponding to the assigned block cannot be accessed by the Processor, but with the MAC enabled, all memory locations can be accessed.

Each Segmentation Register is 32 bits wide and contains three fields - Segment Limit Field (Bits 0:11), Segment Relocation Field (Bits 12:23), and Segment Control Field (Bits 24:27). The remaining bits are not used. These registers are loaded from the local Memory Data Bus.

The interrupt status register is 32 bits wide. Bits 0:26 are unassigned and must be zero. Bits 27:31 have the following meaning when set:

Bit	Meaning
27	Invalid address
28	Non-Present Address
29	Write Protect Violation
30	Write/Interrupt Condition
31	Execute Protect Violation

The Segmentation Registers are assigned the first 32 halfword addresses of the strapped block, and the interrupt status register the next two addresses. If unassigned address of the strapped block are accessed, Segmentation Registers are not loaded, the interrupt status register is not cleared or read out and the memory location is not accessed.

With the MAC enabled, all memory reference instruction addresses are modified by the contents of the relocation field of the accessed Segmentation Register (SR). The MAC uses the 12 most significant memory address bits from the Processor. Four of the bits select one of the 16 Segmentation Registers. Bit 11 of the current PSW determines which group of four bits that the MAC must use. With MAC enabled and PSW Bit 11 zero, the first four bits of the Processor supplied Memory Address (MXR120:150) perform SR selections. If PSW Bit 11 is one with MAC enabled, the next group of four bits (MAR000:030) are used for SR selection. (A strap option is provided whereby MAR040:070 can be used for SR selection rather than MXR120:150 with the MAC enabled and PSW Bit 11 a zero.)

An accessed SR inputs the contents of its limit, relocation, and control fields; to the comparator, the adder and the memory access interrupt logic respectively.

In the 02-348 MAC, the four most significant bits of the limit field are not used, and registers are not provided for storing them. The comparator compares the eight limit field bits with the bits derived from the address select. This block transmits all 12 Processor memory address bits to the adder if MAC is disabled. With the MAC enabled and PSW Bit 11 low, MA00:07 are presented to the comparator and adder. If an enabled MAC sees PSW high, MA04:07 are the input bits to the comparator and adder. The comparator generates a limit error if the limit field is less than but not equal to the address out of the Address Select logic.

The 12 bits of the relocation field are added to the address out of the Address Select logic. The adder output drives the Memory Bank Decoder and the Latch Register.

The four bits of the control field, the limit error and the memory reference description (MEM1, IR1, and MW1) check the validity of the pending memory access. An interrupt is generated if a violation is detected. On and after an interrupt all memory write operations are changed to memory reads except on a Write/Interrupt condition where a write is allowed but an interrupt is still generated. The conversions of writes to reads is inhibited when the MAC is disabled.

The cause of an interrupt is stored in the interrupt status register. With the MAC disabled, the interrupt is cleared whenever the Processor accesses the interrupt status register. The contents of the status register are read with a Processor memory read reference of the interrupt register assigned memory location, and the contents are cleared with a memory write to the same location. System Clear (SCLR0) also clears the interrupt status register.

4. FUNCTIONAL DIAGRAM ANALYSIS

4.1 Introduction

This section covers Functional Schematics 02-348D08. Note that in INTERDATA functional schematics, the last character in a mnemonic symbol designates the logic level when the signal is active. That is, MA030 is Memory Address Bit 3 which is active when at a logical zero (0) level as indicated by the last character of MA030.

As has been noted in the block diagram analysis, the DMABC is a MAC minus the relocation and protect feature. In the analysis that follows, what is described for the DMABC also holds true for the MAC with any exceptions noted. The functional analysis first discusses the bus control logic of the DMABC and MAC, and finally the relocation and protect feature of the MAC.

4.2 Processor to Local Memory Bus

The Processor to DMABC or MAC interface is synchronized to the Processor's clock and memory timing. The Clock (CLK1)(Sheet 3) is used directly, inverted (CLK0), and double inverted (CLK1A0). This is a 62.5 nanoseconds wide pulse with a 250 nanosecond repetition period as shown in Figure 4. Local memory timing is generated and controlled by the Processor. The two memory timing signals Early Read (ER0) and Inhibit (INH0) with which the interface is concerned are shown with respect to CLK1 for a 1 microsecond core memory (Figure 4). The falling edge of Early Read (ER0) is the start of a core memory cycle and the rising edge of Inhibit (INH0) is the end of the cycle. In the interface, (Sheet 3) ER0 (3M2) sets the the Enable Memory D flip-flop (EOM0) (3J3) and the end of INH0 toggles it reset. System Clear (SCLR0A) directly clears the EOM flip-flop on a power up/down or initialize. An active EOM0 indicates that local memory is busy. Memory addresses must be settled at the back panel of the memory module when ER0 goes active and the address must not be changed until INH0 is removed. Memory data must be settled when INH0 goes active and must not be changed until INH0 goes high.

The DMABC and MAC are informed of a pending Processor memory reference instruction with the Memory reference (MEM1), the Memory Write (MW1), and the Instruction Read (IR1 for MAC) signals from the Processor. These signals are generated on the falling edge of CLK1 before ER0. In addition to the memory reference signals, a Processor busy signal (PBY0) is supplied, which is ANDed with MEM1 (3H1) to produce a Gated Memory reference (GMEM1)(3H1). The gated memory reference and MW1, if the memory is not enabled (EOM0)(3J2), develop Memory Read (MRD1)(3M1) or Memory Write (MWR1)(3M1) on the falling edge of CLK1. Active GMEM1 and MW1 (3H1) raise MWR1, but an inactive MW1 and GMEM1 raise MRD1. On the same clock edge the Read and Set signal (RDSET0) (3L2) from the Processor is toggled into a separate D flip-flop (3L2). Both this flip-flop and that for MRD1/MWR1 are directly cleared with SCLR0A. These flip-flops develop the Write signal (WR0)(3R1) on Processor to extend memory accesses. The Write signal (WRT0) (5M7) for the Processor to LM accesses is controlled by the Processor, and OR ties to that of the DMABC or MAC generated WRT0 for DMA to LM accesses (Sheet 5).

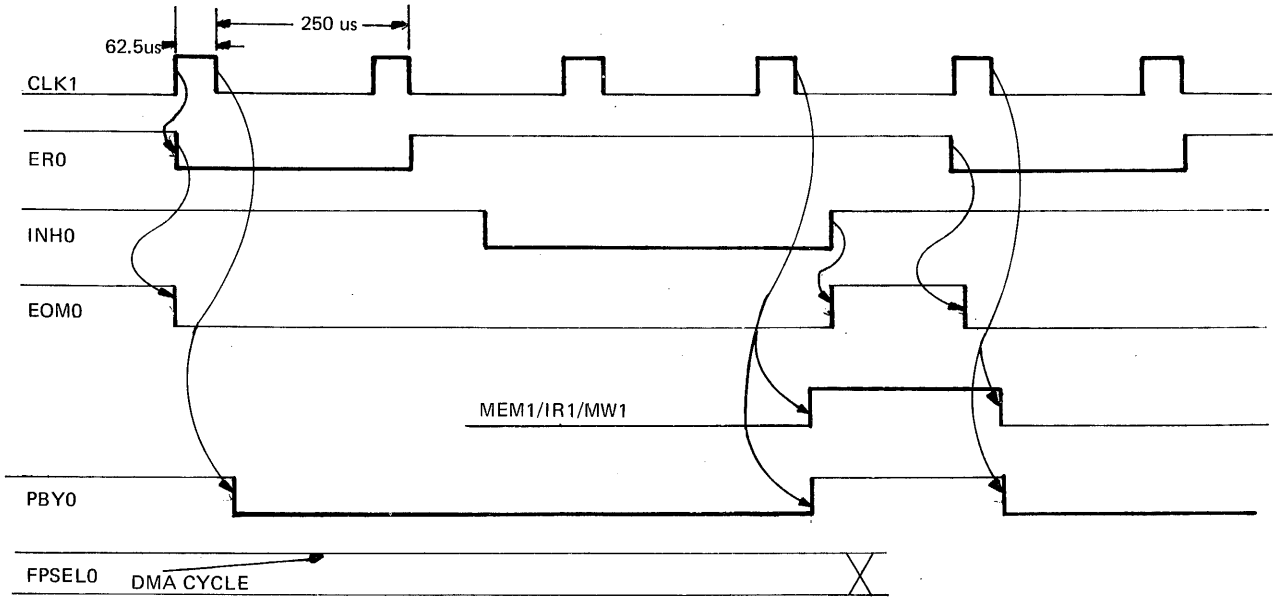


Figure 4. Processor - DMAC/MAC Synchronizing Signals

At all times the most significant bits of the Processor supplied Memory Address (MXR120:150; MAR000: 070) are fed into the DMABC or MAC (Sheet 1). In the DMABC, the inverted states are wired to the Memory Bank Decoder and the data input of the Latch Register. In the MAC, the adder outputs are decoded and latched. The data is latched by the Load Memory Address Slave lines (LMASA1 and LMASB1) (3M3), which are active if EOM0 and CLK0 are high and the interface does not have a previous still-to-be-executed memory reference to XM; i.e., EXDUA0, extended data unavailable is inactive. The "1" latch outputs (XAD141, XAD151, and AD001:071) connect to the local Memory Address Bus drivers (Sheet 4) that are enabled when the Processor is permitted to use the local Memory Bus (FPSEL1 high). XAD121 and XAD131 do not appear on the LM Address Bus because LM is limited to a maximum of 256 Kilobytes. However, the Memory Bank Decoder (Sheet 6) uses these signals to determine if a bank other than LM is to be addressed. The seven least significant Memory Address bits (MA080:140) (Sheets 4 and 5) and the Memory Data lines (MD000:150) (Sheet 2) are driven directly by the Processor.

The "0" output of the Latch Register is the "A" input of the 2:1 inverting multiplexor (Sheets 1 and 5). The remaining memory address bits connect to the multiplexor from the LM Bus. Local memory data bus lines connect to the "B" input of the multiplexor. The output (EMX121:151 and EMA001:151) connect to the drivers of the DMA Bus transceivers (Sheets 4 and 5).

4.3 Processor to Memory

ALU121 and ALU131 (6G4) during GMEM1 (Sheet 6) determine if a local or an extended memory bank is to be accessed. If both ALU signals are inactive an LM access is pending, but if either is active the DMABC or MAC will have to acquire the DMA Bus to address extended memory.

The state of FPSEL0 (7L6) from the Processor determines whether or not the DMABC or MAC outputs the Latch Register contents to the LM Address Bus. When a DMA device is using the LM Bus, FPSEL0 is high and FPSEL1 disables the latch bus drivers (Sheet 4). The drivers are always enabled when FPSEL0 is active. FPSEL0 enables/disables bus drivers (Figure 4) only when the local memory is not busy. On a Processor local memory access, if the Processor is selected (FPSEL0), the DMABC or MAC drive XMA140, XMA150 and MA000:070 of the LM Address Bus from the Latch Register. The Processor controls the remaining address lines (MA080:140). The Processor starts the memory timing (ER0) on the leading edge of CLK1, and EOM0 (3H2) goes active. Memory Data lines (MD000:150) (Sheet 2) are driven by the Processor on a write and by the LM bank on a read. On the rising edge of INH0, EOM0 goes high. The memory cycle is completed.

If, during GMEM1, ALU121 or ALU131 are active, an extended memory bank must be accessed. An Extended Memory signal (XMEM0) to the Processor inhibits the start of local memory timing (Sheet 6). XMEM0 and CLK1A direct set a flip-flop (6K3) to enable Extended Data Unavailable (EXDUA0) (6N3), if the DMABC or MAC is not busy (MACBZ0) (6M2). This flip-flop is cleared by a System Clear (SCLR0C). The controller is busy if it has not completed a previous Processor to extended memory access. EXDUA0 informs the Processor that data is unavailable and that extended memory is busy. To acquire the DMA Bus, the controller must determine if the memory bank to be accessed and the DMA Bus are idle and if a higher priority DMA device has requested the DMA Bus. XAD12 and XAD13 from the Latch Register are decoded (6A4) into memory bank 1, 2, or 3. Each bank has a busy line (M0BZ0, M1BZ0, M2BZ0, or M3BZ0) and in the DMABC and MAC they connect to a transceiver. If during CLK1A the decoded memory bank is busy, or if the DMA Bus is busy (BUBZ0) (7M9), or if a DMA request is pending (PMD low) (7K8), the controller waits. When none of these conditions exist, a flip-flop sets (6K2) that enables MACBZ0 (6L2) and Processor Wait (CPUW1) (6L2). This flip-flop is cleared on a System Clear (SCLR0C). As a result, if IN0SC1 is high, ENA0 and ENB0 enable the 2:1 multiplexers, the transceivers for the DMA Bus, and BUBZ0 (Sheets 1, 4, 5, and 7).

CPUW1 also enables an Oscillator (GOOS1) (6R2) which indicates a sequence (Sheet 7) for communicating over the DMA Bus. With the Processor selected (FPSEL0) and GOOS1 active, P0SC1 is a square wave of a 80 nanosecond period (Figure 5) which toggles a three stage Johnson ring counter on the falling edge of POSC1. This counter is cleared by System Clear (SCLR0B). The memory busy transceiver is enabled when PA0 and PC1 (6C1) are low to activate the MXBZ0 line (Sheet 6) decoded from XAD12 and XAD13. During this interval the select address lines (SLADA0 and SLADB0) select the address and WR0 (3M6) inputs of the 2:1 multiplexor to drive the DMA Bus for 160 nanoseconds. The Load Address (LAD0) (5A6) is active for 80 nanoseconds and drives the LOAD0 line of the DMA. For a memory write the multiplexor transmits data from MD000:150 to the transceivers when SLADA0 and SLADB0 are removed. During the Processor State 4 (PST41), Load Data (LDAT0) drives LOAD0 for 80 nanoseconds. The first falling edge of POSC1 after PST41 is activated removes EXDUA0, and the second edge removes CPUW1 and MACBZ0, to disable the multiplexors, transceivers, and oscillator.

For a memory read from extended memory after the address LOAD0 has been gated, INOSC1 goes low to disable the oscillator, the multiplexors, and transceiver drivers. The DMABC and MAC monitor DMA lines DMX141 and DMX151, the answering memory bank coded bits, and XAD12 and XAD13, the code bits of the responding bank. If a match exists when ANS0 goes active, an Answer Match (ANMA0) (6G5) enables INOSC1 to start the oscillator. The DMA Bus is loaded into the DMA data register on the falling edge of ANS0. During PST41, POSC1 gates the data register (GMSA1, GMSB1) to the local Memory Bus. The counter then disables EXDUA0, CPUW1, MACBZ0, ENA0, ENB0, and GOOS1 as it did for a write to extended memory.

An active CPUW1 and MACBZ0 initiate a time-out (Sheet 6) of approximately 50 microseconds. A false answer pulse (FANS0) (6R8) is generated to enable INOSC1 and to prevent the Processor from hanging up if it fails to receive an answer within the time-out.

4.4 DMA Bus Occupancy

The DMABC and MAC control DMA Bus occupancy on a request basis. When a device requests use of the DMA Bus (XREQ0), the controller initiates a sequence that resolves request contention between devices by freezing the request status, selects the highest priority requesting device and turns the bus over to the selected device at the proper time.

Across the top of Sheet 7 is the basic sequencing logic. It consists of a 2-2-3-4 AND/OR inverter that enables or disables a 60 nanosecond period square wave oscillator whose output toggles a three-stage Johnson ring counter. The counter is initialized to the reset state by System Clear (SCLR0B). In the idle or initialize state of the counter, Control State 0 (CST01) is active (Figure 6). In the idle state, an XREQ0 starts the oscillator. A nominal 30 nanosecond QUE0 pulse is derived to freeze the request status. QUE0 goes active on the first negative transition of the counter toggle and is removed by setting a flip-flop (initialized reset by SCLR0B) on the first positive transition of the toggle. After 30 nanoseconds, this is followed by the transmission of a 120 nanosecond priority chain pulse (TPC0) to select the highest priority requesting device. TPC0 propagates through the DMA devices in daisy chain fashion. TPC0 from the controller is received at the first device as RPC0. If this device has not requested service, it will transmit a TPC0

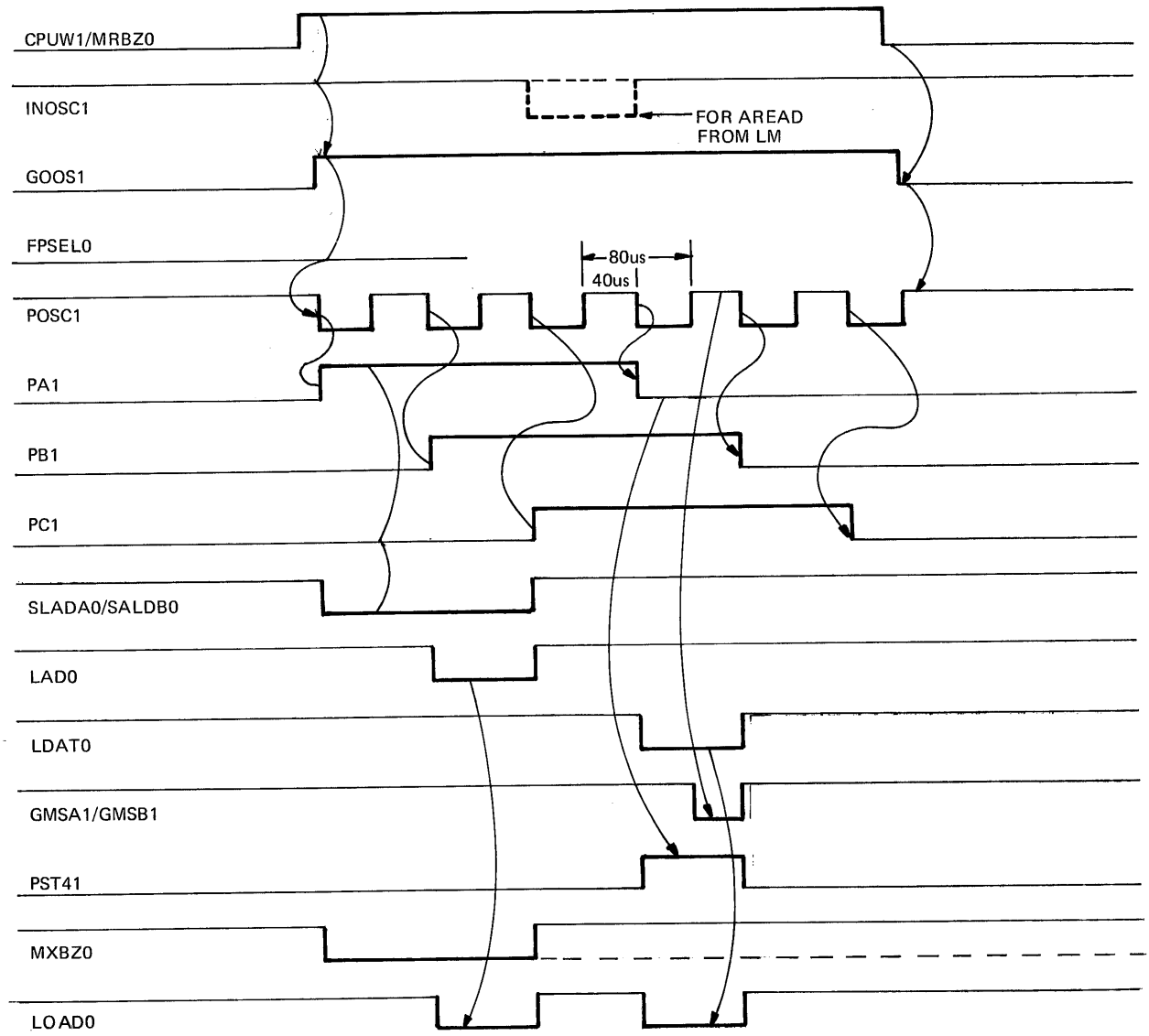


Figure 5. Processor to DMA Sequence

to the next lower priority DMA device. However, if the device had requested service, it inhibits transmission of TPC0 to the next device. If during the latter half of TPC0 or Control State 3 (CST31) a previous DMA Bus transfer has not been completed, the oscillator is stopped. After the completion of this transfer or if none existed, the counter toggles to remove TPC0. If the DMA Bus is busy or if the local memory is busy (EOM1) and the pending request is not destined for local memory (LMRQA0 high) and the controller is in the wait condition (CPUW1), the oscillator is inhibited. At this time, the oscillator is also inhibited if the pending request is for local memory (LMRQ1) and the DMA data register is not available to accept new data. However, when none of these conditions exist, the DMABC or MAC sends a 60 nanoseconds wide Start of Transmission pulse (SOT0) to the selected device. In the DMABC and MAC, the start pulse direct sets FEOT1 high and enables bus busy (BUBZ0)(Sheet 7). The counter toggles to the idle state and SOT0 is removed. The End of Transmission flip-flop (initialized clear by SCLR0B) remains set until the controller receives an End of Transmission (EOT0) from the device currently using the DMA Bus. SOT0 enables the selected device which removes its request signal.

4.5 DMA Bus Transfer

If the destination of a DMA transfer is not to local memory or the Processor, the transfer is executed without any intervention by the DMABC or MAC. During such a transfer the Processor can access local memory until a local memory request (LMRQ0) is queued.

When a request is slated for local memory, this is made known by the device when it becomes selected by lowering LMRQ0 (Figure 6). This request is latched in the controller (Sheet 6) and the Processor is sent a request (REQ0) and HALT0. HALT0 prevents the Processor from initiating local memory timing for a possible Processor to local memory access. In response to REQ0, the controller receives an Enable signal (EN0). When the contention logic outputs, SOT0, the counter flip-flop CB1 signal drops and the HALT0 condition is removed. The enabled device outputs address and read/write information followed by a LOAD0, and the DMA Bus is Loaded (DLDA1) into a buffer address register (Sheets 4 and 5) and bus busy (BBZ0) is activated. BBZ0 overrides the state of the FEOT flip-flop to hold the bus busy (BUBZ0) active even where FEOT is reset by EOT0 from the currently selected device. For a write into memory, DA151 low, the device outputs data followed by LOAD0. The falling edge of LOAD0 activates LDDA1, LDDB1, LDDC1 and LDDD1 to toggle the state of the DMA Bus into the data buffer register (Sheet 2) and to make the Buffer Register Unavailable (BRU1).

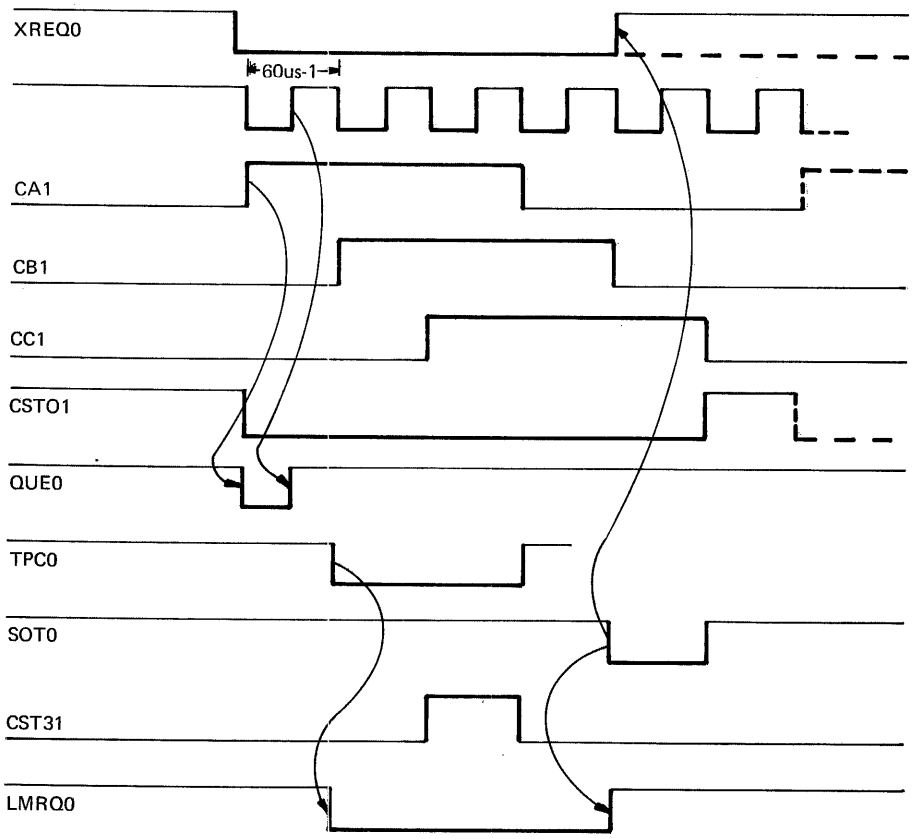


Figure 6. DMA Bus Request Sequence

With HALT0 removed the Processor is free to raise EN0 and FPSEL0. The rising edge of EN0 resets the LMRQ flip-flop and a high FPSEL0 enables the DMA to local memory bus drivers but disables those associated with the Processor (Sheets 4 and 5). During the time that local memory is idle (EOM1 low) the DMA buffer address register is loaded into the bus driving logic register. When memory timing starts, EOM1 and FPSELA0 enable the data register drivers (GMSA1, GMSB1) (Sheet 7). For a write to memory, DI51 is low to inhibit the logic of the direct set inputs of the data registers.

The rising edge of ER0 during a DMA to LM cycle toggles a flip-flop that initiates a time delay (Sheet 6) which disables DLDA1, LDDA1, LDDB1, LDDC1, LDDD1, LRQ0 and clears the flip-flop that initiated the delay. The timer resets 210 nanoseconds after the rising edge of ER0. While it is set, it maintains BRU1 (6J9) active. When FPSEL0 goes active, local memory is available for Processor use. However, if the contention logic has queued another local memory request in time to steal the next cycle, FPSEL0 remains high. Note that all registers in the DMA to LM write are initialized clear as a function of System Clear (SCLR0).

On a DMA read from local memory, DAI51 becomes active when the address is loaded (Sheet 6). CLMDA0 and CLMDB0 clear the data register when local memory is idle (EOM0 high) and the DMA port selected (FPSEL0 high). With FPSEL0 and DA151 high, DMA read is active and DMRDA1 and DMRDB1 (Sheet 7) enable the direct set input logic of the data register. After memory timing is initiated, the rising edge of ER0 enables the oscillator. ENOSC0 is the output of a flip-flop which is initialized set on System Clear (SCLR0B). ENOSC0 enalbes the 2:1 transceivers ENA0, ENB0 and GOOS1. ENA1 keeps the Bus Busy (BUBZ0) active, and the Go Oscillator level (GOOS1) enables the oscillator (Sheet 7) the output of which enables the load oscillator signal LOSC1 to toggle on the rising edge of a two state Johnson ring counter (Sheet 6).

The counter was forced direct cleared before ENOSC0 went active. With the direct clear inputs high, LOSC0 can now toggle the counter. The first transition of LOSC1 is a falling edge which has no effect on the cleared state of the counter (Figure 7). On the first two rising edges, first LA1 and then LB1 are toggled set. Load Answer (LANS0) is transmitted through the data enabled channel of the multiplexor through the transceivers to generate ANS0. If the Processor detects a parity error, it activates ERR0 (Sheet 1) which is transmitted as DMX130 when the LM data read-out is sent to the device. When LA is toggled reset, LANS0 and ENOS0 are disabled and LA and LB revert to the forced cleared state.

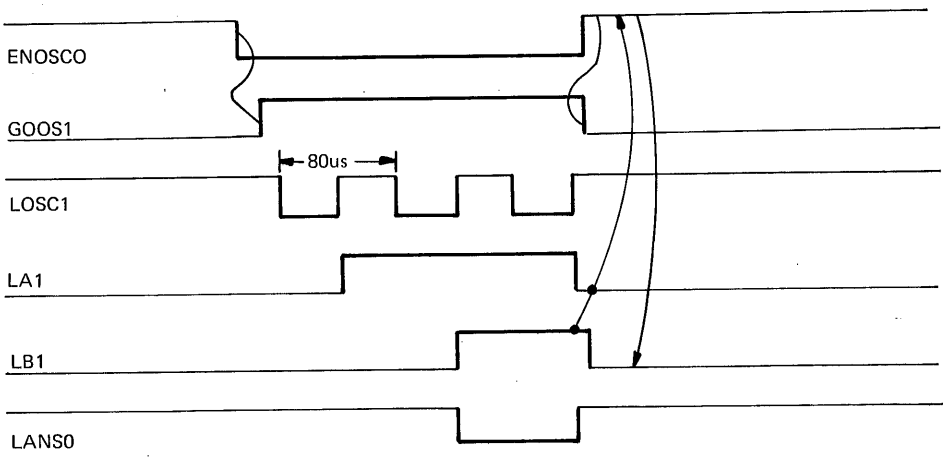


Figure 7. LM to DMA Answer Sequence

4.6 DMA/Processor Contention

The timers on Sheet 7 are adjusted to generate a 30 nanosecond pulse, SAMP1, delayed 170 nanoseconds from the rising edge of CLK1A (Figure 8). The function of CLK0 is to insure that a false SAMP1 is not caused during initiation of the timers. SAMP1 samples XREQ0 before the leading edge of CLK1 when a Processor memory access starts. If XREQ0 is active on the rising edge of SAMP1, the Processor mode level (PMD1) is driven low on the falling edge SAMP1 by the two contention flip-flops which are initialized clear by System Clear (SCLR0B). A high PMD1 is one of the conditions that must be satisfied for a Processor to gain access to the DMA Bus.

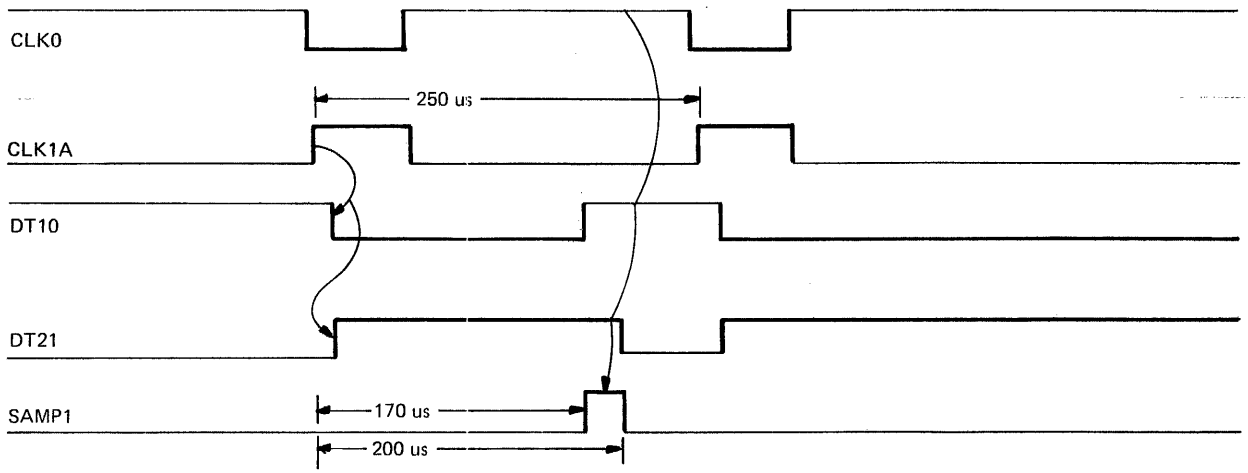


Figure 8. SAMP1 Generation

4.7 Parity

For a DMABC or MAC configured system, the memory banks (local and extended) must all be equipped with parity or they must be void of parity. Without parity, terminal MPAR is tied to P5V via a resistor, and with parity MPAR is strapped to ground. MPAR0 to the Processor will then always be high for no parity or low for parity.

4.8 MAC - Relocation and Protect (Sheets 1, 2, 3)

4.8.1 MAC Disabled. The RUN flip-flop (Sheet 3) is initialized reset by System Clear (SCLR0A). A cleared RUN overrides disable MAC (DMAC0) from the Processor by forcing inhibit MAC (INMAC0) active. In this state, the relocation and protect logic is disabled. INMAC0 enables the Processor address ports of the 2:1 multiplexors and places the four bit ALUs in the load mode. As a result, the ALU outputs are the inverted states of MXR120:150, MAR000:070 (Sheet 1). In addition, INMAC0 inhibits the J input logic of the interrupt status register and the address decoding for trapping segmentation or interrupt state register references (Sheet 3).

In the disabled mode, the MAC functions as a DMABC with one exception. On every gated memory reference MAC checks if the Processor memory address falls into the 128 halfword block reserved for its 17 hardware registers. Sheet 3 shows the strapping terminals available for optionally selecting the block address to begin at X'00300', X'00500' or X'00900'. A match indicates a Segmentation Register Trap (SRTR0) and Extended Memory (XMEM0) is actviated (Sheet 6). If the Processor is selected (FPSEL0) and local memory is idle (EOM0 high) RUN and FSR are toggled set on the trailing edge of TRCLK1. The set state of FSR generates EXDUA0 and is used for decoding MA080:140, MWR1, and MDR1. If a write into Segmentation Registers is decoded, TRCLK1 gates the write odd or even lines (WRO0:WRE0). With the MAC disabled. The outputs of the 4 to 1 multiplexors (Sheet 2) are MA100:130 which select one of the 16 Segmentation Registers in the enabled stack. WRO0 or WRE0 pulse the Write Enable (WE) of the register logic and the state of the Memory Data bus lines (MD000:150) are stored in the selected register of the stack. On the falling edge of TRCLK1, FSR0 and EXDUA0 are removed.

If a Memory Read (MRD1) of the interrupt status register has been decoded, then on the TRCLK1 following the setting of FSR, Read Status (RSTA1) gates the states of lines IR271:311 (Sheet 3) through local memory data drivers (Sheet 2) to the Processor. For a Memory Write (MWR1) in the status register, the same clock gates the Clear Status line (CSTA0) which directly clears the interrupt status registers. The status registers are also forced clear by a cleared RUN flip-flop. The interrupt flip-flop is cleared (CLKNT0) whenever the status register is accessed or the RUN is not set.

4.8.2 MAC Enabled. With the RUN flip-flop set, DMAC0 controls the enabling/disabling of the relocation and protect logic. A high DMAC0 disables INMAC0 which places the ALU logic in the add mode. Now every Processor memory reference is processed through a selected Segmentation Register.

Segmentation Register selection is controlled by DMAC0 and PSW111 in the 4:1 multiplexors (Sheet 2). In the fullword mode (PSW111 low) and MAC enabled, port "3" of the multiplexor is selected. This port is strapped to MXR120:150 for selecting one of sixteen address Segmentation Registers. This port can be strapped to MAR040:070 - a custom application which will not be covered here. In the halfword mode (PSW111 high) port "2" is selected which connects to MAR000:030. The multiplexors are always enabled and therefore register selection is only a function of DMAC0 and PSW111.

The output of the selected Segmentation Register consists of the Limit Field (L001:071), the Relocation Field (XR121:151, R001:071) and the control Field (SC241:271). The limit field inputs to the four bit magnitude comparators, the relocation field to the four bit ALUs, and the control field to the status checking logic.

The 2:1 multiplexors (Sheet 1) select the memory address bits that feed the ALU and the magnitude comparator. If the MAC is disabled, the inverted states of the 12 address bits (MXR120:150, MAR000:070) pass through the multiplexors. For the fullword mode with MAC enabled, MAR00:07 are transmitted and 0s are transmitted for MXR12:15. In the halfword mode only MAR04:07 are transmitted and 0s are transmitted for MXR12:15, MAR00:03. For the custom application described previously, 0s are substituted for all 12 address bits. MAR041:071 always feed the magnitude comparator, but PAR001:031 are the output of their multiplexor.

4.8.3 Limit Check. The magnitude of PAR001:031, MAR041:071 is compared with the contents of the magnitude of the limit field. If the limit field is less than but not equal to the memory address, a Limit Error (LIME1) is generated. LIME1 is supplied to the status checking logic.

4.8.4 Relocation. The four bit ALUs and the look ahead carry generator derive the sum of the relocation field and the memory address supplied by the multiplexors. The output of the ALU feeds the memory Latch Register (Sheet 1), and ALU Bits 121 and 131 the memory bank decoder (Sheet 6).

4.8.5 Control Field. With the MAC inhibited (INMAC0 active) the "J" input logic to the interrupt status register (IR27:31) is disabled. This register can only be toggled set (on the leading edge of TRCLK1) and only directly cleared.

On a gated memory reference (GMEM1) a limit error (LIME1) raises the "J" input of IR27 and if the presence bit (SC271) is not active, the "J" input of IR28 is raised. If the execute protect bit (SC291) is high during an instruction fetch (IR1), the "J" input of IR31 is high. For write protection a high SC261 and MW1 enable the "J" input of IR29, but if the request is write/interrupt protected (SC261 low and SC251 high) on a MW1, the "J" input of IR30 is enabled. A high on any of the "J" inputs at the time of the leading edge of TRCLK1 toggles set the corresponding IR flip-flop and the Interrupt flip-flop (INT). The Interrupt flip-flop generates a MAC interrupt (MAC0). The true output of the interrupt status register feeds the local memory data drivers (Sheet 2).

An active "J" input on IR27, 28, 29 or 31 is gated by CLK1 as a change write to a read (CWR0) to the Processor. In addition, if IR271, 281, 291 or 311 is active, MW1 is forced low, MRD1 high and CWR0 is gated on every Processor memory reference if MAC is enabled. With MAC disabled, INMAC0 inhibits the interrupt status checking, inhibits the states of the status register from controlling MW1, MRD1 and CWR0 and inhibits MAC0.

5. TIMING ADJUSTMENTS

The oscillator for the queue sequence (Sheet 7) is adjusted by removing the output of the 2-2-3-4 AND NOR logic (a strap between A50 Pin 8 and A10 Pin 10 on the 35-527 M01 or 35-528 M01 or between A01 Pin 8 and A13 Pin 9 on the 35-527 M00 or 35-528 M00) and setting the oscillator capacitor for a 60 nanosecond period square wave on the Johnson ring counter toggle.

The oscillator controlled by GOOS1 (Sheet 7) is adjusted by grounding the INOSC1 and CPUW1 AND gate, and with the processor idle adjust the oscillator capacitor for a 80 nanosecond period POSC1.

SAMP1 is adjusted by synching to CLK1A and varying the corresponding potentiometers for DT10 and DT21 to generate SAMP1 as shown in Figure 8.

NOTE

For MAC 35-527 (R03 or higher) or DMABC 35-528 (R02 or higher) or either M01 Board, replace the SAMP1 adjustment by the following: Place the Processor in a loop to perform a Write to extended memory. Adjust the rising edge of the $\overline{Q}$ output of the one shot (7D7) to be 500ns from the falling edge of SOT0. See Figure 9.

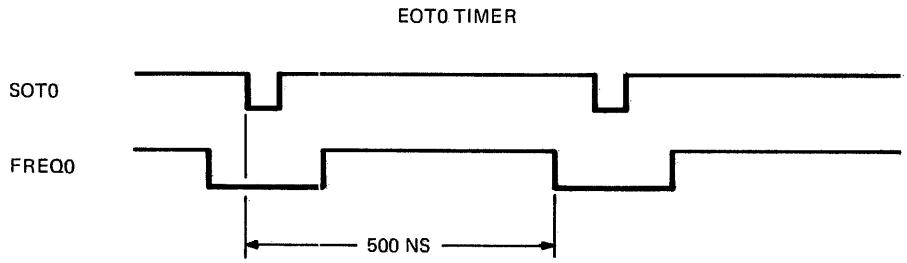


Figure 9. EOT0 Generation (M01 Only)

All other timing adjustments are set at the manufacturing plant.

6. MNEMONICS

The following list provides a brief description of each mnemonic found in the Memory Access Controller (MAC). The 02-348D08 source of each signal is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
AD001:071	Address bits from Latch Register	Sheet 1
ALU121:151	Four most significant bits from Adder	Sheet 1
ANAM0	Answer Match	6J4
ANS0	DMA Answer Control line	5D8
BBZ0	Bus Busy	6G6
BH0	Bus Hold	5D8
BRU1	Buffer Register Unavailable	6J9
BUBZ0	Buffer Busy	7M9
CA0	Control State flip-flop A	7K3
CB1	Control State flip-flop B	7KB
CLINT0	Clear Interrupt flip-flop	3R8
CLK1	Processor Clock	3H2
CLMDA0 CLMDB0	Clear DMA Memory Data Register	6J5
CPUW1	Central Processor Unit Wait	6L2
CST01	Control State 1	7N3
CST31	Control State 3	7N4
CSTA0	Clear Status Register	3R8
CWR0	Change Write to a Read	3K4
DGNDA:E	Grounds for DMX 120:150, DMA 000:160, Load 0, ANS0 and BH0	Sheet 4
DLOA1	DMA Load Address	6F6
DMAC0	Disable MAC	3M6
DMA000:160	Part of DMA Multiplexed Bus	Sheets 4 and 5
DMRDA1 DMRDB1	DMA Memory Read Local Memory	7N8
DRD1	DMA Read	5M5
EMA001:151 EMX121:151	Data from DMABC or MAC for DMA Multiplexed Bus	Sheets 1, 4, and 5

MNEMONIC	MEANING	SCHEMATIC LOCATION
ENA0 ENB0	Enable Transceivers and 2:1 Multiplexors	6N1
EN0	Enable	6A6
ENOSC0	Enable Oscillator	6R6
EOM0	Enable Memory	3K3
EOT0	End of Transmission	7F8
ER0	Early Read	3H2
ERR0	Error	1M2
EXDUA0	Extended Data Unavailable	6N3
FANS0	Fake ANS0	6R8
FEOT	End of Transmission flip-flop	7K8
FPSEL0	Processor Select	7L6
FSR	Segmentation Register flip-flop	3F8
GMEM1	Gated Memory Reference	3N4
GMSA1 GMSB1	Gate Memory Strobe	7J6
GNDF	Ground for Memory Bus Transceiver	6B2
GOOS1	Go Oscillator	6N2
GPAR	Gate Parity	7N6
HALT0	Halt initiation of Local Memory Timing	6J7
INH0	Inhibit-Local Memory Timing Signal	3H3
INMAC0	Inhibit MAC	3N6
INOSCI	Inhibit Oscillator	7J5
IR1	Instruction Read	3A5
IR271 281 291 301 311	Interrupt Status Register Outputs	Sheet 3
L001:071	Limit Field	Sheet 2
LDAT0	Load Data	7J5

MNEMONIC	MEANING	SCHEMATIC LOCATION
LDDA1 B1 C1 D1	Load Data	6J8
LAD0	Load Address	7J5
LANS0	Load Answer	6R7
LIME	Limit Error	1F9
LMASA1 LMASB1	Load Memory Address Slave Register	3M3
LMRQ0	Local Memory Request	6A6
LOAD0	Load	5D8
LOSC1	Load Oscillator	7E5
MA000:140	Part of Local Memory Address Bus	Sheets 4 and 5
MAC0	MAC Interrupt	3N5
MACBZ0	MAC Busy	6L2
MAR000:140	Memory Address bits from Processor	Sheets 1 and 2
MD000:160	Local Memory Data Bus	Sheet 2
MEM1	Memory Reference	2L4
MRD1	Memory Read	3M1
MW1	Memory Write from Processor	3H1
MWR1	Memory Write	3M1
M0BZ0 M1BZ0 M2BZ0 M3BZ0	Memory Bank 0 Busy Memory Bank 1 Busy Memory Bank 2 Busy Memory Bank 3 Busy	6B3
PA0	Processor flip-flop A	6F7
PAR0	Parity	369
PAR001:031	Processor Address Bits 0, 1, 2, and 3	1E4
PBY0	Processor Busy	3L4
PC1	Processor flip-flop C	7H3
PMD1	Processor Mode	7J8
POSC1	Processor Oscillator	7E3
PST41	Processor State 4	7J7

MNEMONIC	MEANING	SCHEMATIC LOCATION
PSW111	Processor Status Word Bit 11	2A7
QUE0	Queue Pulse	7N5
R001:071	Part of Relocation Field	Sheet 2
RDSET0	Read and Set	3L2
REQ0	Request	6D6
RSTA1	Read Status Register	3M9
SAMP1	Sample	7F7
SCLR0	System Clear	7A5
SC241:271	Segmentation Register Control Field	3L8
SLADA0	Select Address A	7J4
SLADB0	Select Address B	7J5
SOT0	Start of Transmission	7N4
SRTR0	Segmentation Register Trap	3J7
TRC0	Transant Priority Chain Pulse	7N3
TRCLK1	Trap Clock	3E9
WR0	Write Extended Memory	3R1
WRE0	Write Even Segmentation Register	3M7
WRO0	Write Odd Segmentation Register	3M7
WRT0	Write Local Memory	5M6
XAD121:151	Extended Address Bits from Latch Register	1K3
XDUA0	Extended Data Unavailable	6N3
XMA140 150	Extended Local Memory Address Bits	4N3
XMBK1	Extended Memory Bank	6R4
XMEM0	Extended Memory	6K4
XR121:151	Part of Relocation Field	2M8
XREQ0	DMA Request	7F8

EXTENDED SELECTOR CHANNEL

[redacted]

M73-105
EXTENDED SELECTOR CHANNEL INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides the necessary information for the installation of the 02-328 Extended Selector Channel (ESELCH) (Product Number M73-105) in a Model 7/32 or 7/32 C or 8/32 Processor System. The Extended Selector Channel is complete on one 35-508 printed circuit board.

2. PHYSICAL CHARACTERISTICS

2.1 Dimensions

15 3/8" x 14 7/8"

2.2 Weight

2 1/2 pounds maximum

3. INSTALLATION

The ESELCH may be installed in any even numbered chassis slot (i.e., 0, 2, 4, or 6) of the Extended Direct Memory Access (EDMA) Bus. In a 7/32 or 7/32 C Processor, the EDMA Bus starts at either Slot 3 or Slot 7 of the Expansion back panel of the twin chassis. See 02-348A20, 7/32 or 7/32 C Memory Access Controller (MAC) Installation Specification for details. For a 8/32 Processor, the EDMA Bus starts at Slot 2 of the lower CPU chassis. The EDMA Bus can be extended to other Expansion chassis through cables but the bus length is limited to eight feet. Seven DMA devices (in addition to the MAC) may be installed on the EDMA Bus. The seven devices may all be ESELCHs with no extended memory interfaces or custom DMA devices.

3.1 Back Panel Wiring

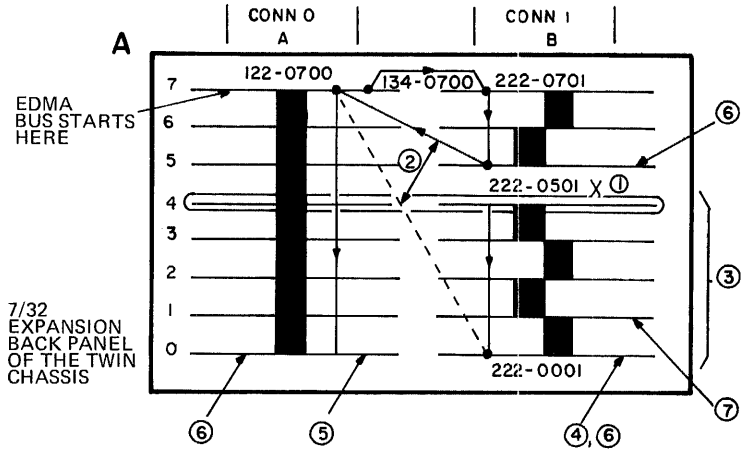
At the time of installation it is necessary to cut the Multiplexor Bus wiring between the even numbered slot accepting the ESELCH and the next higher numbered slot on the one (1) connector only. The Receive Acknowledge/Transmit Acknowledge (RACK0/TACK0) "daisy chain" wiring on the back panel is rerouted according to Figure 1A. The lower numbered card slots in the chassis become part of the private ESLECH Bus on the one (1) connector only.

To install an ESELCH in Slot 4:

1. Remove all wires from Connector One (1), between Slots 4 and 5, on Pins 11 through 26, Rows 1 and 2 (see back panel map on Functional Schematic 02-328D08, Sheet 1).
2. Remove the wire between 222-0001 and 122-0700.
3. Remove the RACK0/TACK0 jumper between Pins 122 and 222 on both the zero (0) and one (1) connectors and RPC0/TPC0 jumper between Pins 137 and 237 on zero (0) connector of Slot 4.
4. Connect 122-0700 to 222-0501.

5. Install the ESELCH into Slot 4 of the chassis. The private ESELCH Bus now appears on the Connector One (1) side of Slots 4, 3, 2, 1 and 0. All slots on the Connector Zero (0) side and Slots 7, 6, and 5 on Connector One (1) side remain as standard Multiplexor Bus slots.

To install an ESELCH in any other even numbered slot of a universal expansion chassis, a simular procedure is follov Refer to Figure 1 (B, C, D, E, and F).



NOTE: THE CIRCLED NUMBERS ON ILLUSTRATIONS A, B, C, D, E, AND F REFER TO THE CORRESPONDING NUMBERS IN THE FOLLOWING INSTALLATION PROCEDURES.

TO INSTALL A SELECTOR CHANNEL IN SLOT 4 OF THE 7/32 EXPANSION BACK PANEL OF THE TWIN CHASSIS

① CUT THE MULTIPLEXOR BUS.

② JUMPER RACK0/TACK0 AS SHOWN, REMOVE DASHED JUMPER.

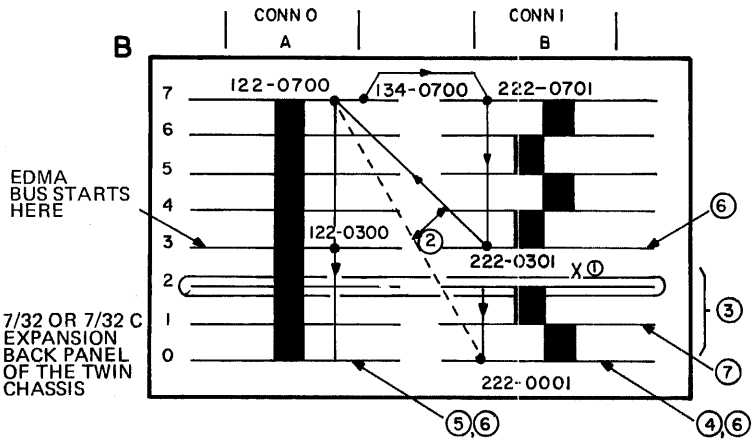
③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN 1) SIDE ONLY ALL SLOTS ON THE CONNECTOR ZERO (CONN 0) SIDE AND SLOTS 7, 6 AND 5 ON THE CONNECTOR ONE SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑥ INSTALL I/O TERMINATORS 35-433R01 HERE.

⑦ INSTALL EDMA BUS TERMINATOR 35-548 HERE.



TO INSTALL A SELECTOR CHANNEL IN SLOT 2 OF THE 7/32 EXPANSION BACK PANEL OF THE TWIN CHASSIS

① CUT THE MULTIPLEXOR BUS

② JUMPER RACK0/TACK0 AS SHOWN, REMOVE DASHED JUMPER.

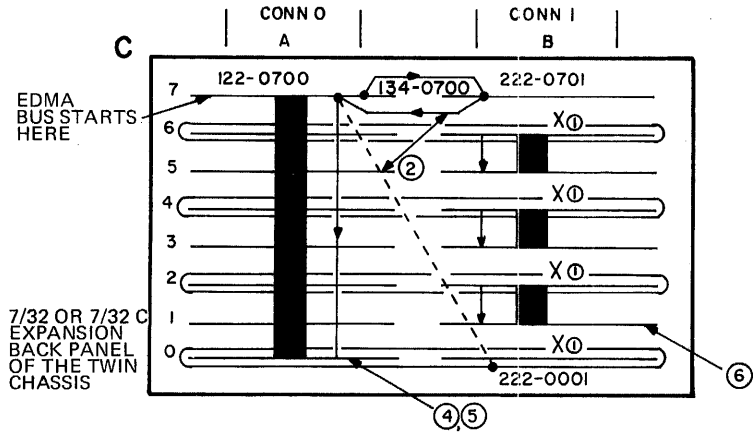
③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN 0) SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑥ INSTALL I/O TERMINATORS 35-433R01 HERE.

⑦ INSTALL EDMA BUS TERMINATOR 35-548 HERE.



TO INSTALL 4 SELECTOR CHANNELS (IN SLOTS 6, 4, 2, AND 0) OF THE 7/32 EXPANSION BACK PANEL OF THE TWIN CHASSIS

① CUT THE MULTIPLEXOR BUS IN FOUR PLACES.

② JUMPER RACK0/TACK0 AS SHOWN, REMOVE DASHED JUMPER.

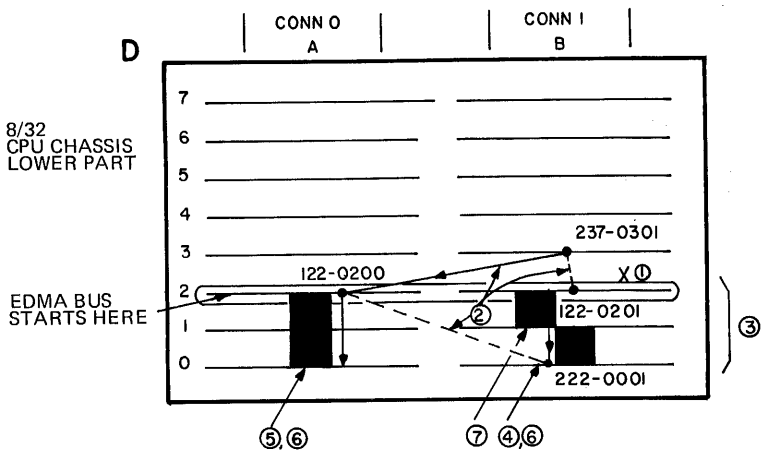
③ EACH SELCH EXCEPT THE ONE IN SLOT 0 HAS ONE SLOT AVAILABLE ON IT'S PRIVATE BUS. THE PRIVATE BUSSES CAN BE EXTENDED TO OTHER CHASSIS BY INSTALLING CABLES IN SLOT POSITIONS 0, 1, 3, AND 5 ON CONNECTOR ONE (CONN1) SIDE.

④ ALL SLOTS ON THE CONNECTOR ZERO (CONN 0) SIDE REMAIN AS THE STANDARD MULTIPLEXOR BUS. THIS BUS CAN BE EXTENDED BY INSTALLING A CABLE HERE.

⑤ INSTALL I/O TERMINATOR 35-433R01 HERE.

⑥ INSTALL EDMA BUS TERMINATOR 35-548 HERE.

Figure 1. Backpanel Modifications



TO INSTALL A SELECTOR CHANNEL IN SLOT 2 OF THE 8/32 CPU CHASSIS LOWER PART

① CUT THE MULTIPLEXOR BUS.

② JUMPER RACK0/TACK0 AS SHOWN, REMOVE DASHED JUMPER.

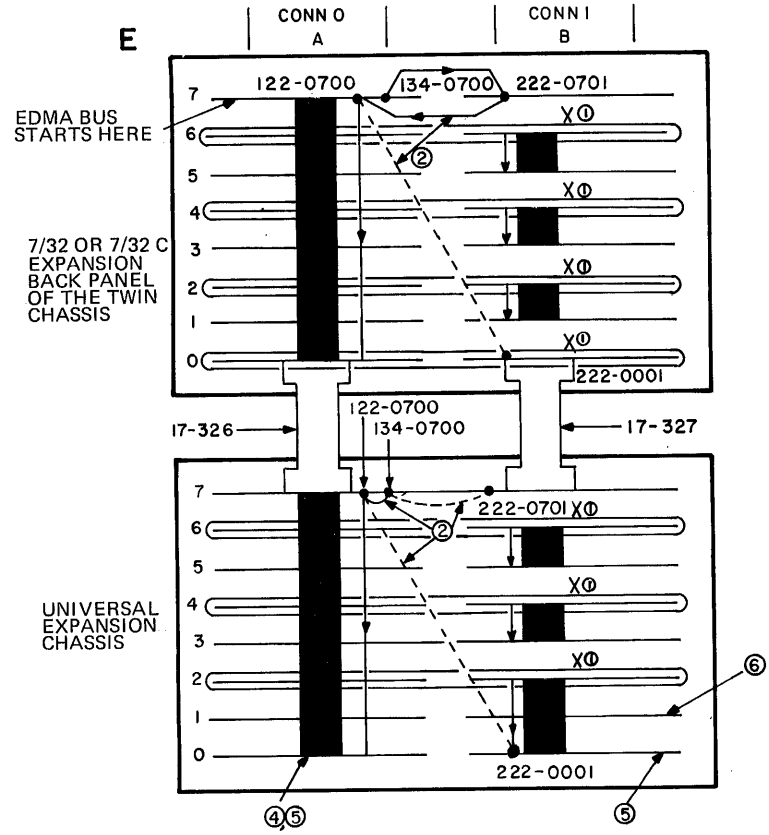
③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN 0) SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑥ INSTALL I/O TERMINATORS 35-433R01 HERE.

⑦ INSTALL EDMA BUS TERMINATOR 35-548 HERE.



TO INSTALL 7 SELECTOR CHANNELS IN SLOTS 6, 4, 2 AND 0 OF 7/32 EXPANSION BACK PANEL OF THE TWIN CHASSIS AND 2, 4, 6 OF EXPANSION CHASSIS.

① CUT THE MULTIPLEXOR BUS IN 7 PLACES.

② JUMPER RACK0/TACK0 AS SHOWN, REMOVE DASHED JUMPER.

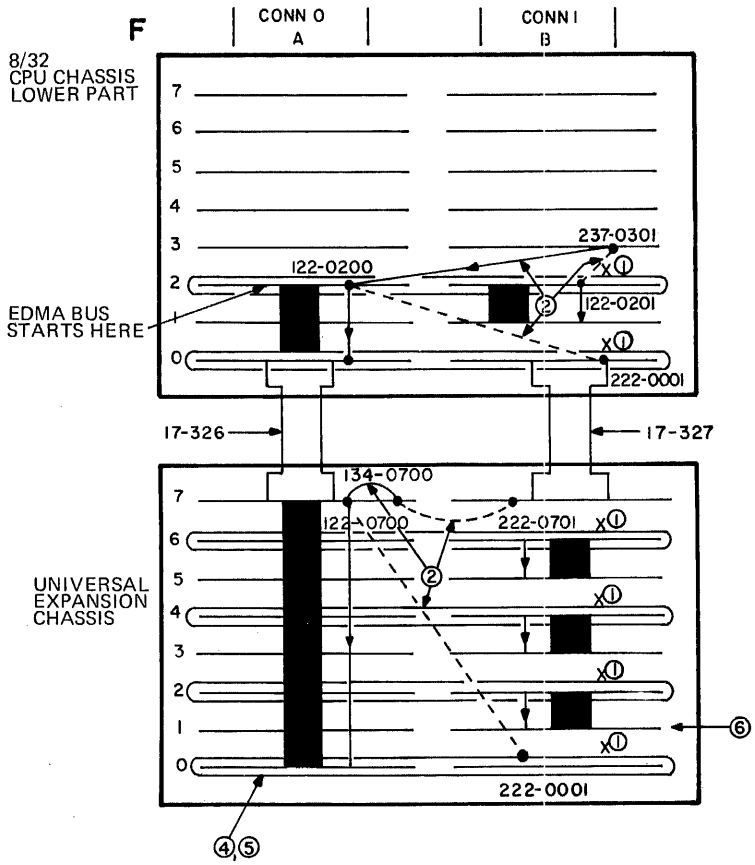
③ EACH SELCH EXCEPT THE ONE IN SLOT 2 OF UNIVERSAL EXPANSION CHASSIS HAS ONE SLOT AVAILABLE ON IT'S PRIVATE BUS. THE PRIVATE BUSSES CAN BE EXTENDED TO OTHER CHASSIS BY INSTALLING CABLES IN SLOT POSITIONS 1, 3, AND 5 OF JUMBO CHASSIS AND 0, 3, 5 OF EXPANSION CHASSIS ON CONNECTOR ONE (CONN 1) SIDE.

④ ALL SLOTS ON THE CONNECTOR ZERO (CONN 0) SIDE REMAIN AS THE STANDARD MULTIPLEXOR BUS. THIS BUS CAN BE EXTENDED BY INSTALLING A CABLE HERE.

⑤ INSTALL I/O TERMINATORS 35-433R01 HERE.

⑥ INSTALL EDMA BUS TERMINATOR 35-548 HERE.

Figure 1. Backpanel Modifications (Continued)



TO INSTALL 6 SELECTOR CHANNELS IN SLOTS 0 AND 2 OF THE 8/32 CPU LOWER CHASSIS AND 0, 2, 4, AND 6 OF THE UNIVERSAL EXPANSION CHASSIS.

① CUT THE MULTIPLEXOR BUS IN 6 PLACES.

② JUMPER RACK0/TACK0 AS SHOWN, REMOVE DASHED JUMPERS.

③ EACH SELCH, EXCEPT THE ONE IN SLOT 0 OF THE EXPANSION CHASSIS, HAS ONE SLOT AVAILABLE ON ITS PRIVATE BUS. THE PRIVATE BUSSES CAN BE EXTENDED TO OTHER CHASSIS BY INSTALLING CABLES IN SLOT POSITIONS 1 OF CPU LOWER CHASSIS AND 0, 1, 3, 5, OF THE EXPANSION CHASSIS ON THE CONNECTOR ONE (CONN 1) SIDE.

④ ALL SLOTS ON THE CONNECTOR ZERO (CONN 0) SIDE REMAIN AS THE STANDARD MULTIPLEXOR BUS. THIS BUS CAN BE EXTENDED BY INSTALLING A CABLE HERE.

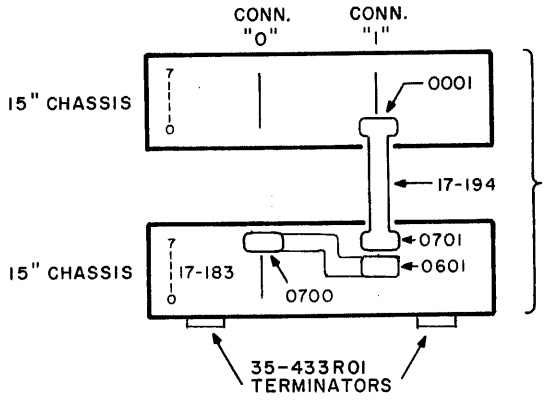
⑤ INSTALL I/O TERMINATOR 35-433R01 HERE.

⑥ INSTALL EDMA TERMINATOR 35-548 HERE.

Figure 1. Backpanel Modifications (Continued)

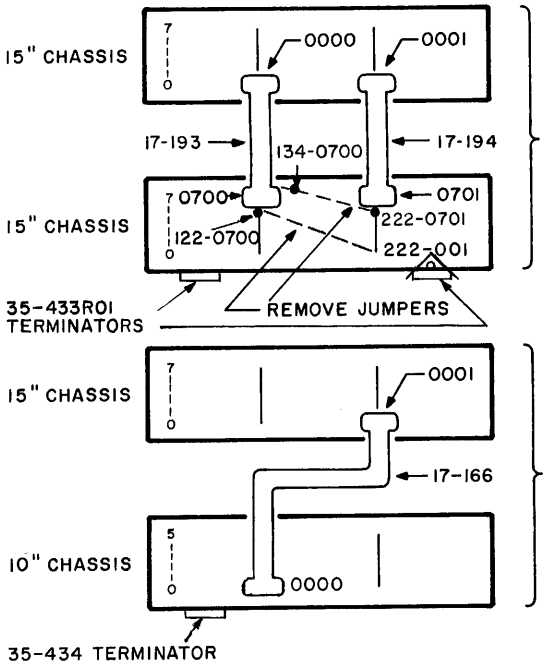
3.2 Cabling

The cabling necessary for the ESELCH depends on the systems physical configuration. When the ESELCH Bus does not extend outside the twin chassis, no cabling is required. When the ESELCH Bus must be extended to another chassis, a number of cable configurations can be used, see Figure 2. Care should be taken to minimize bus lengths and not exceed 30 inches (three expansion chassis).



(A) CONNECTS TWO ADJACENT 15" CHASSIS. THE PRIVATE SELCH BUS APPEARS AT BOTH CONNECTORS 0 AND 1 OF THE LOWER CHASSIS. NOTE THE DATA CHANNEL DOES NOT APPEAR IN THE LOWER CHASSIS.

Figure 2. Cabling



(B) USED TO CONNECT TWO ADJACENT 15" CHASSIS. THE MULTIPLEXOR BUS APPEARS AT CONNECTOR 0, AND THE SELCH BUS APPEARS AT CONNECTOR 1. WHEN USING THIS CONFIGURATION, THE FOLLOWING WIRING CHANGES TO THE RACK0/TACK0 DAISY CHAIN MUST BE MADE TO THE LOWER CHASSIS: REMOVE 134-0700 TO 122-0701 AND 222-0001 TO 122-0700 AND ADD 134-0700 TO 122-0700.

(C) CONNECTS THE PRIVATE SELCH BUS TO A 10" CHASSIS ONE OR TWO CHASSIS AWAY.

Figure 2. Cabling (Continued)

The termination of the 17-312 cable, at Slot 7 or Slot 3, on the Expansion back panel designates the start of the EDMA Bus. Refer to Figure 3. If any slot (on the one side) is to be used for an ESELCH, add contiguous wire straps as follows:

Slot 7	Slot 3
129 - 0701	129 - 0301
129 - 0601	129 - 0201
129 - 0501	129 - 0101
129 - 0401	129 - 0001
129 - 0301	
129 - 0201	
129 - 0101	
129 - 0001	

through the appropriate chassis.

4. ADDRESS STRAPPING

The preferred address of the ESELCH is X'0F0' (10 bit address). The controller is strapped for this address at the factory. To change the address, refer to Functional Schematic 02-328D08.

5. STRAP OPTIONS FOR ADDRESS SPACE ALLOCATION

Address space allocation for the four memory banks is determined by strap options in the ESELCH. Each memory bank's address space must be zero or a multiple of 64K bytes up to a maximum of 1,024K bytes for a 8/32 Processor or a maximum of 256K bytes for a 7/32 or 7/32 C Processor. Address assignment must be contiguous and the four memory banks are assigned address space in ascending order.

On the ESELCH printed circuit board, there are two decoders, A03 and A04, which decode the extended address bits (four most significant address bits). Each output of the decoders allocates 64K bytes of memory. The 16 outputs with wire wrap stakes are marked 0:15. The four wire wrap stakes next to them are marked M00, M10, M20, and M30. These denote the four memory banks. The address space allocation should be strapped according to system configuration. All non-existent memory locations should be strapped to the stake marked NE (Non-Existent Memory). See Figure 4. Address Allocation

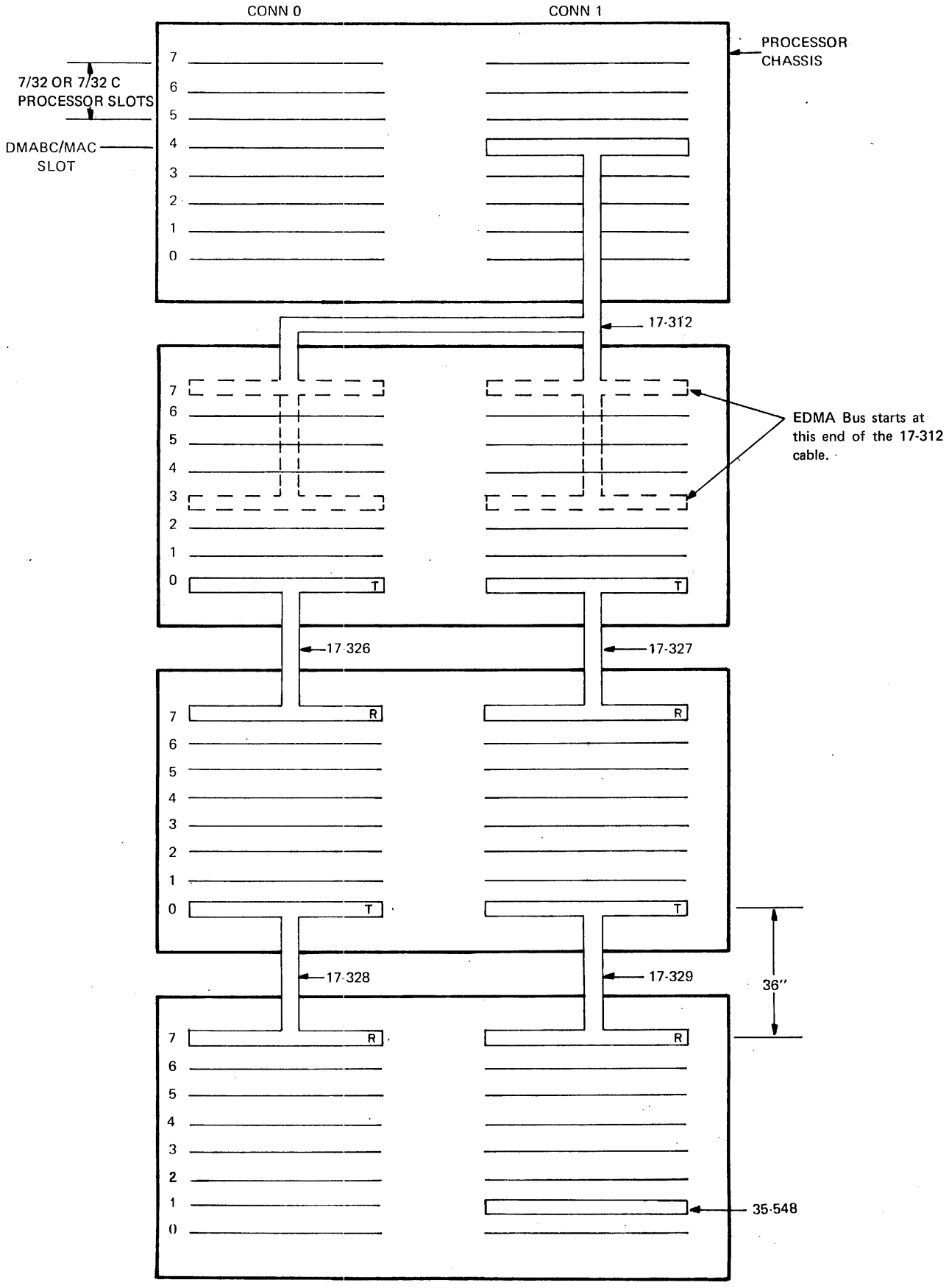


Figure 3. DMABC and MAC Back Connections

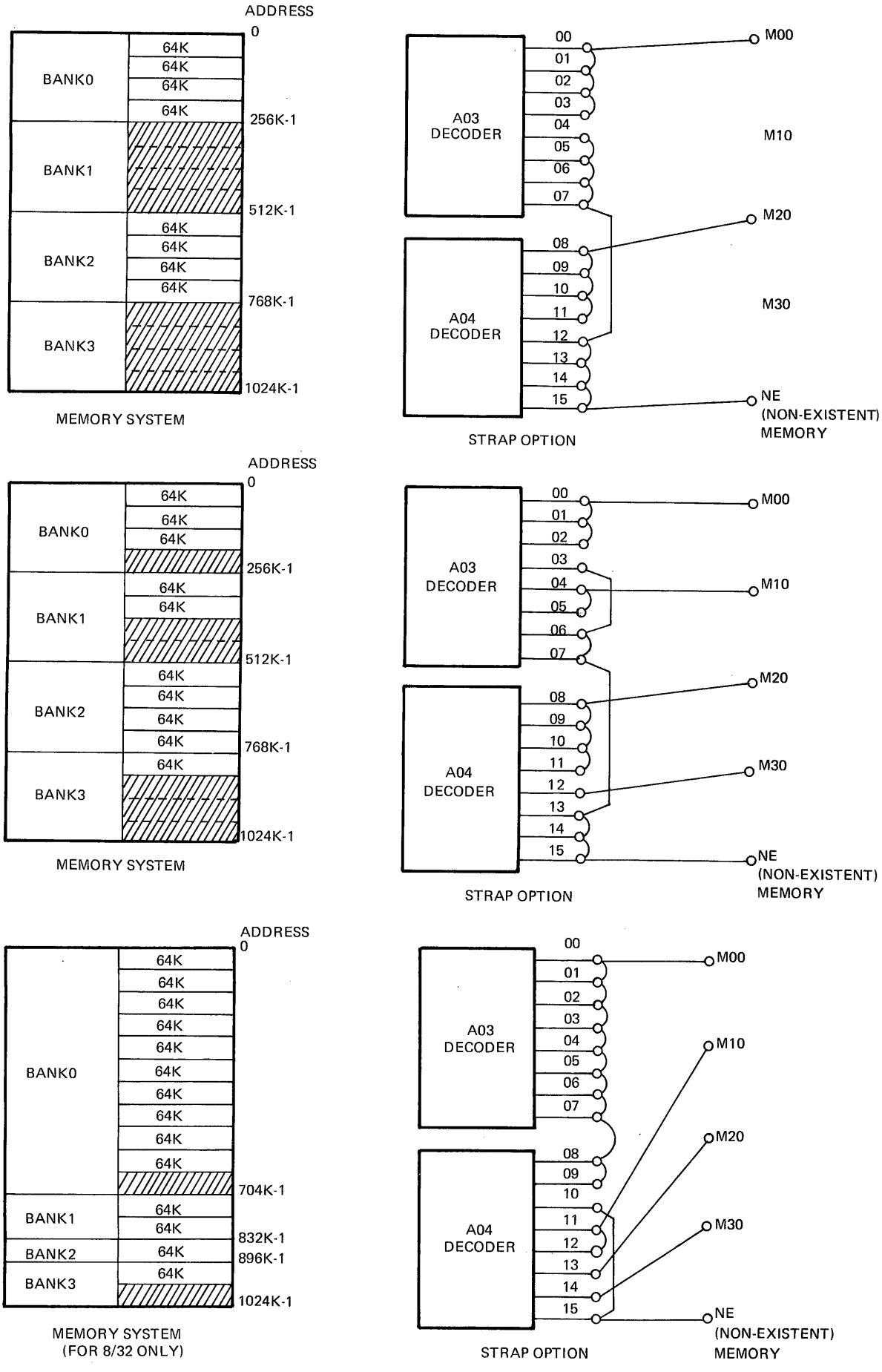


Figure 4. Address Allocation

6. INSTALLATION CHECKS

The ESELCH is factory tested using a special high speed device. Therefore, field checks are contingent upon the user having the appropriate hardware and software available with which to exercise the ESELCH. Test Program 06-161, shipped with the ESELCH, may be used if an INTERDATA Magnetic Tape or a Removable Cartridge Disc system is installed on the ESELCH's private bus.

7. CONFIGURATION

The ESELCH may be installed in any chassis within the same system cabinet as the Processor. The total number of DMA devices must be seven or less. This includes ESELCHs, memory interfaces, or custom DMA devices using the Universal EDMA Bus Interface.

8. MODEL 7/32, MODEL 7/32 C, AND MODEL 8/32 STRAPPING

For use with the Model 7/32 and 7/32 C, strap E2 to E3 (M01 only).

For use with the Model 8/32, strap E2 to E1 (M01 only).

NOTE

If 35-508M01 ESELCH is used for a 7/32 or 7/32 C Processor, Strap E3 to E2. For an 8/32 Processor, Strap E1 to E2. If 35-508M00R12 ESELCH is used for 7/32 or 7/32 C Processor, Strap E3 to E2.

NOTE

The 35-508M01R02 (or higher) ESELCH is required for 8/32 Systems. The 35-508M00 or M01 may be used with 7/32 or 7/32 C Systems.

M73-105
EXTENDED SELECTOR CHANNEL MAINTENANCE SPECIFICATION

1. INTRODUCTION

The 02-328 Extended Selector Channel (ESELCH) (Product Number M73-105) is Direct Memory Access port which provides block data transfer between a device controller and memory. Once initiated, the transfer is independent of the Processor. The Processor sets up the device controller, loads the ESELCH with the starting and the final addresses of the memory block, specifies the type of operation (Read or Write), and issues a GO command. The ESELCH then handles the transfer without further direction by the Processor.

The Extended Selector Channel is complete on one printed circuit board and occupies one slot in a system chassis. The ESELCH provides the drivers, receivers, and termination resistors for the private ESELCH Bus. This bus originates at Connector One (1) of the ESELCH slot and extends to each lower numbered slot in the system chassis on the Connector One (1) side only. The private ESELCH Bus can be extended to other chassis, as required. For installation information, refer to the 02-328A20 Extended Selector Channel Installation Specification.

2. SCOPE

This specification describes the operation of the ESELCH in its various modes, i.e., Setup, Memory Read, Memory Write, and Termination. Where necessary, this specification references the Multiplexor Channel Bus and Extended Direct Memory Access Bus operations. These busses are described in detail in the Architectural and Product Line Standards, Extended Direct Memory Access Bus, Publication Number 43-005.

3. BLOCK DIAGRAM ANALYSIS

Refer to the ESELCH block diagram on Sheet 1 of Functional Schematic 02-328D08, and the ESELCH Flow Chart, Figure 1, during the following analysis. Before initiating a data transfer via the ESELCH, the device controller and the ESELCH must be set up. The set up procedure is implemented by the Processor via the Multiplexor Bus (MPX-Bus). When the ESELCH is in the idle mode, the MPX Bus is tied directly to the private ESELCH Bus through the ESELCH. This allows the Processor to communicate directly with any device on the private ESELCH Bus.

To prepare the ESELCH for data transfer, the Address Register (AR) and Auxiliary Address Register (AAR) must be loaded with the starting address in memory where the transfer is to begin, and the Final Address Register (FAR) must be loaded with the address of the last memory location to be accessed. These registers are loaded from the eight least significant Data Lines D080:150 by four or six consecutive Data Availables (DA) from the Processor.

The first two or three Data Availables load the starting address and the last two or three Data Availables load the final address. The Address Register is incremented by two after each halfword is transferred to/from the device. Data transfer is terminated when the Auxiliary Address Register is equal to the Final Address Register or when the Auxiliary Address Register increments past its maximum value, X'FFFFF'.

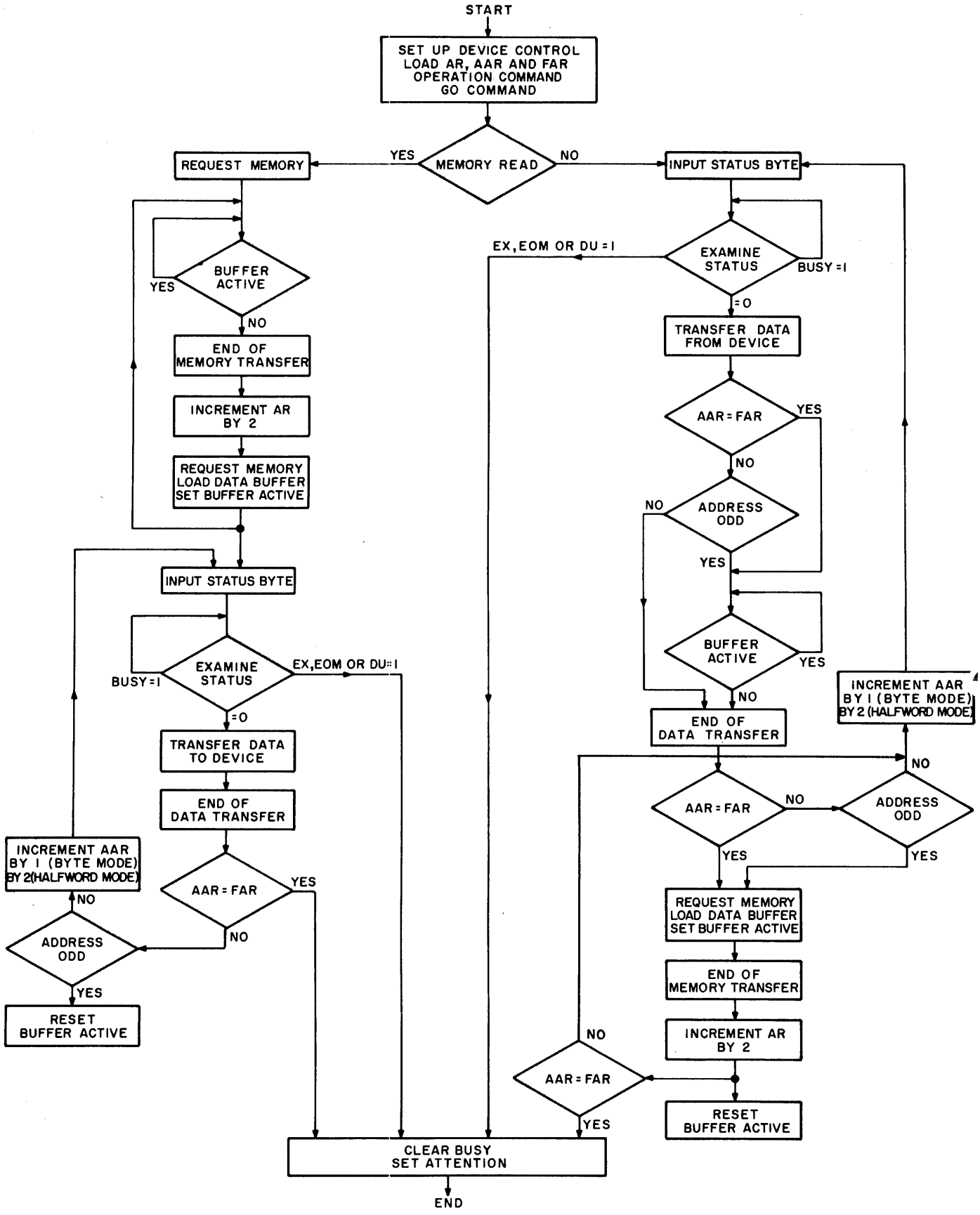


Figure 1. Flow Chart

Data transfer is begun by the Processor issuing a GO command to the ESELCH. Transfer to/from the device is now independent of the Processor. The GO command also prevents communication between the Processor and any device on the private ESELCH Bus until the transfer is terminated and the ESELCH is addressed.

Data transfer is controlled in the move data circuit by inspection of the four least significant bits of the status byte presented by the active device on the private ESELCH Bus. When any one of the three least significant bits are set (EX, EOM, or DU) the transfer is terminated. Bit 12 (Busy) regulates the rate of data transfer. In the Memory Read mode, the actual data transfer begins with a Memory Request (XREQ0) as soon as a GO command is issued. When the memory request is serviced by the Processor, the ESELCH EDMA Bus control circuit activated Select (SEL), which gates the contents of the Address Register onto the EDMA Bus. An Answer (ANS0) signal is then sent out by the Processor to gate a halfword of data from memory into the Data Register. At the termination of the memory transfer, the data is loaded from the Data Register to the Data Buffer and the Address Register is incremented.

Once the Data Buffer is loaded, data transfer to the device over Private Data Lines PD000:150 is initiated and, when applicable, a request is made to fetch the next halfword from memory. This cycle continues until either a match is detected between the contents of the Auxiliary Address Register and the contents of the Final Address Register, or until the transfer is aborted due to an error condition.

In the Memory Write mode, the data transfer sequence described previously for Memory Read mode is reversed. That is, two bytes of data are loaded into the Data Register from the device prior to a memory request and the data flow is from the device to the Data Register, Data Register to the Data Buffer, and finally to memory.

The branch gate circuit and the move data circuit control the flow of data between memory and the device. The branch gate circuit supervises the overall data flow, while the move data circuit performs the handshaking between the ESELCH and the active device on the private ESELCH Bus.

Upon termination of the data transfer, the program is notified via an interrupt and by the inactive state of the ESELCH Busy flip-flop which is presented to the program as Bit 12 of the ESELCH status byte. Extended Selector Channel Status and Command Byte Data is shown on Table 1.

TABLE 1. EXTENDED SELECTOR CHANNEL STATUS AND COMMAND BYTE DATA

BIT NUMBER	8	9	10	11	12	13	14	15
STATUS BYTE			MEMORY MAL-FUNCTION	MEMORY PARITY FAIL	BUSY			
COMMAND BYTE		EXTENDED ADDRESS READ	READ	GO	STOP	SELCH STATUS		

BUSY	This bit is set by command GO. It remains set while the ESELCH is in the process of transferring data. It is cleared by Initialize, Command STOP, normal termination, and error abortion. When this bit is cleared, an interrupt is generated.
MEMORY MALFUNCTION	This bit is set when the memory interface recognizes a malfunction. It is stored in the ESELCH for subsequent evaluation by the Processor, however, the transfer is not interrupted. It is cleared by Initialize or Command GO.
MEMORY PARITY FAIL	This bit is set when the memory interface recognizes a parity failure. It is stored in the ESELCH for subsequent evaluation by the Processor, however, the transfer is not interrupted. It is cleared by Initialize or Command GO.
READ	This command changes the mode of the ESELCH from Write to Read. In Read mode, data is transmitted from the active device on the ESELCH and written into memory. Whenever a data transmission has been completed, the ESELCH is placed in the Write mode. Each time a Read operation is required, a Read command must be issued.
GO	This command initiates a data transmission. This command can be issued at the same time the Read/Write mode is established.
STOP	This command halts any data transmission in progress, and initializes the ESELCH for starting a new operation. It should be given when the ESELCH terminates.
SELCH STATUS	When this bit is set, the ESELCH status is returned every time on an SR or SS instruction to the ESELCH. When reset, the current SELCH definition applies. (i.e., when the ESELCH is idle, the device status is returned with the BUSY bit forced to a zero. When the ESELCH is transferring data, only the BUSY bit is returned. The ESELCH becomes idle only after Initialize or any I/O instruction to the ESELCH is executed.)
EXTENDED ADDRESS READ	When this bit is set, the ESELCH returns a three byte final address to the Processor if RD or RDR followed by RH or RHR instructions are executed. The most significant byte is returned first. When this bit is reset, the ESELCH returns a two byte final address to the Processor if two successive RD or RDR instructions are executed. The most significant byte is returned first. Before issuing RD or RH instructions to read the final address, a Command STOP should be issued to insure that the ESELCH is in the initial state.

4. FUNCTIONAL DIAGRAM ANALYSIS

4.1 Introduction

This section relates to Functional Schematic 02-328D08, Sheets 2 through 9. Note that in INTERDATA functional schematics, the last character in the mnemonic symbol designates the logic level when the signal is active. For example; D080 is Data Line Number 8 (D08). The last character (0) indicates that when D08 is active, the line is at a logical zero level.

4.2 ESELCH Control Circuit

In the idle mode (the ESELCH is in the idle mode after Initialize or any I/O instruction to the ESELCH is executed), the ESELCH Address (3M9), Busy (4E3), and Multiplexor-ESELCH (MSC) (4E4) flip-flops are reset and the private ESELCH Bus is tied directly to the Multiplexor Bus. This allows the Processor to communicate, via the Multiplexor Bus, with any device on the private ESELCH Bus. When data is transferring from the Processor to the device in the byte mode, DLG (2A3) is low. This disables the inputs to A168 and A156 transceivers (2B4 and 2B7). Data D080:150 (2A5 and 2A8) passes through A168, A156, and inverters at 2D3:2D9 and become DA081:151 (2E3:2E9). Since the ESELCH is idle, BSY1 (2H1) is low. This causes STROBE1, STROBE2, SELA and SELB of the A46, A47, A34, and A35 Multiplexors (2L4:2L9) to become active, thus DA081:DA151 can pass through these multiplexors. At this time DLG1A (2N3) is low because DLG1 (2N2) is low. This enables the A48 and A36 transceivers (2N4 and 2N7) and Data D081:151 passes through these transceivers and is sent to the device as PD080:150 (2N5:2N9).

When data is transferring from the device to the Processor, the selection lines of eight multiplexors at 3C4:3N4 are all inactive (zero is selected), thus PD081:151 can pass through these multiplexors and arrive at the input to transceivers A168 and A156. At this time DLG1 is high. This enables the transceivers and the data passes through as D080:150 to the Processor. Figure 2 shows the details of 19-118 transceivers.

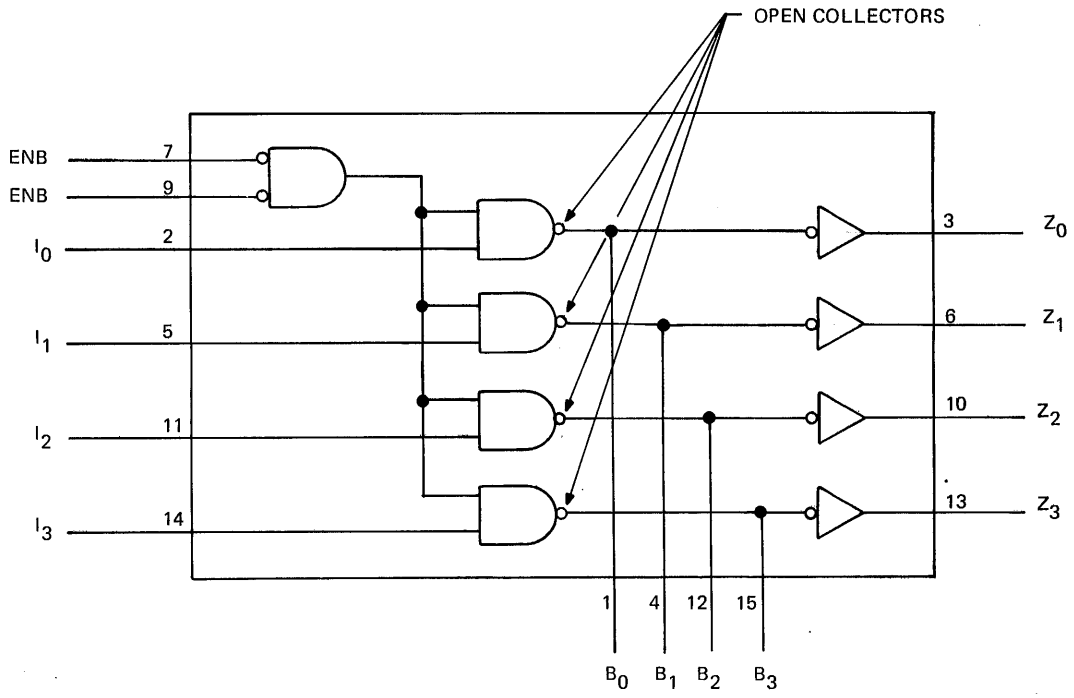


Figure 2. 19-118 Transceiver

To communicate with the ESELCH, it must first be addressed. The ESELCH Address (X'0F0' preferred) is placed on Data Lines D060:150 (2A5:2A8) and the Address control line is activated (ADRS0) (4K7). The ESELCH Address is decoded by the eight input NAND gate (2H6) and the Address flip-flop is set (3M9). The Address flip-flop set output (AD1) (3M8), when active, prevents the control signals on the MPX-Bus from passing onto the private ESELCH Bus by holding the Control Line Gate inactive (CLG1 and CLGA1) (2G2). SGAD0 (4M7) controls the Private Address (PADRS0) (4N7) such that when the ESELCH is being addressed, PADRS0 does not become active. This allows the ESELCH to be addressed without resetting the Address flip-flop on the active device on the private ESELCH Bus.

The loading of the Address Register (AR), Auxiliary Address Register (AAR), and the Final Address Register (FAR) is accomplished by four or six consecutive Data Availables (DAs) from the Processor. The Load/Unload Sequencer (6C3) controls the loading of these registers and the unloading of the Auxiliary Address Register. The Sequencer is set to its initial state by the termination of the last data transfer, a STOP command, or a System Clear (SCLR0) (3K9). The Address Registers on Sheet 6 (6F1:6F8) and the Final Address Registers (FX, FH, and FL) on Sheet 5 are connected as shown in Figure 3. If four consecutive Data Availables to the ESELCH (DAs) are executed by the Processor, the first DA loads DA081:151 into the Final Address Low Register (FL) and the second DA copies the contents of the FL Register into the Final Address High Register(FH) and a new DA081:151 is loaded into the FL Register and so on. After the fourth DA is executed, Bits 00:07 of the starting address are loaded in the Address High Register (AH) and Bits 08:15 of the starting address are loaded in the Address Low Register (AL). Bits 00:07 of the final address are loaded in the Final Address High (FH) Register and Bits 08:15 of the final address are loaded in the Final Address Low Register (FL). Counter A in the Load/Unload Sequencer is initially set at State 3 (0011). After four DAs are executed, Counter A is in State 7 (0111). At this time the D output of Counter A is still low. When Command GO is executed, NAND Gate C generates a Page Zero (PG00) signal to clear the Address Extended Register (AX) and the Final Address Extended Register (FX). The Command GO (3N6) generates a Set Auxiliary Address Register (SETAAR0) (3N6) to copy the starting address into the Auxiliary Address Register at 5B3:5N3. If six DAs to the ESELCH are executed by the Processor, the first four DAs act exactly the same way as before except that the fourth DA also generates a Load Final Address Extended (LFRX0) signal to load DA121:151 into Final Address Extended Register (FX). After the fifth DA is executed, the Extended, High, and Low Starting Address bits and the Extended, and High Final Address Bits are loaded in the AX, AH, AL, FH and FL Registers respectively. At this time, Counter A in the Load/Unload Sequencer is at State 8 (1000) and the D output is high. This inhibits any further data from loading into the AX, AH, and AL Registers. After the sixth DA is executed, the Extended Final Address bits in FH are thrown away and the High Final Address bits in the FL Register are copied into the FH Register and the Low Final Address bits are loaded into the FL Register. At this time all the address bits are loaded into the correct registers. The Command GO (3N6) generates a Set Auxiliary Address Register (SETAAR0) (3N6) to copy the starting address into the Auxiliary Address Register at 5B3:5N3.

If the Extended Address Read Command bit is reset, two Data Requests (DRs) are required to read back the final address from the Auxiliary Address Registers. Counter A145 (6C2) is initially set at State 3 (0011) and the C input of the A157 Decoder is low (6C4) because the A54 (6C7) flip-flop is reset by resetting the Extended Address Read Command bit. The first DR decodes State 3 of Counter A145 and activates the Unload Auxiliary Address Register High (UAARH0) (Sheet 6). Outputs from the Auxiliary Address Register (AAR041:111) (Sheet 3) pass through the Multiplexors at 3C4:3N4 and send the high bytes of the final address to the Processor. The second DR increments the counter to State 4 (100). Since input C of Decoder A157 (6C4) is set low, the zero state is decoded. It activates the UAARL0 and sends the low bytes of the final address to the Processor.

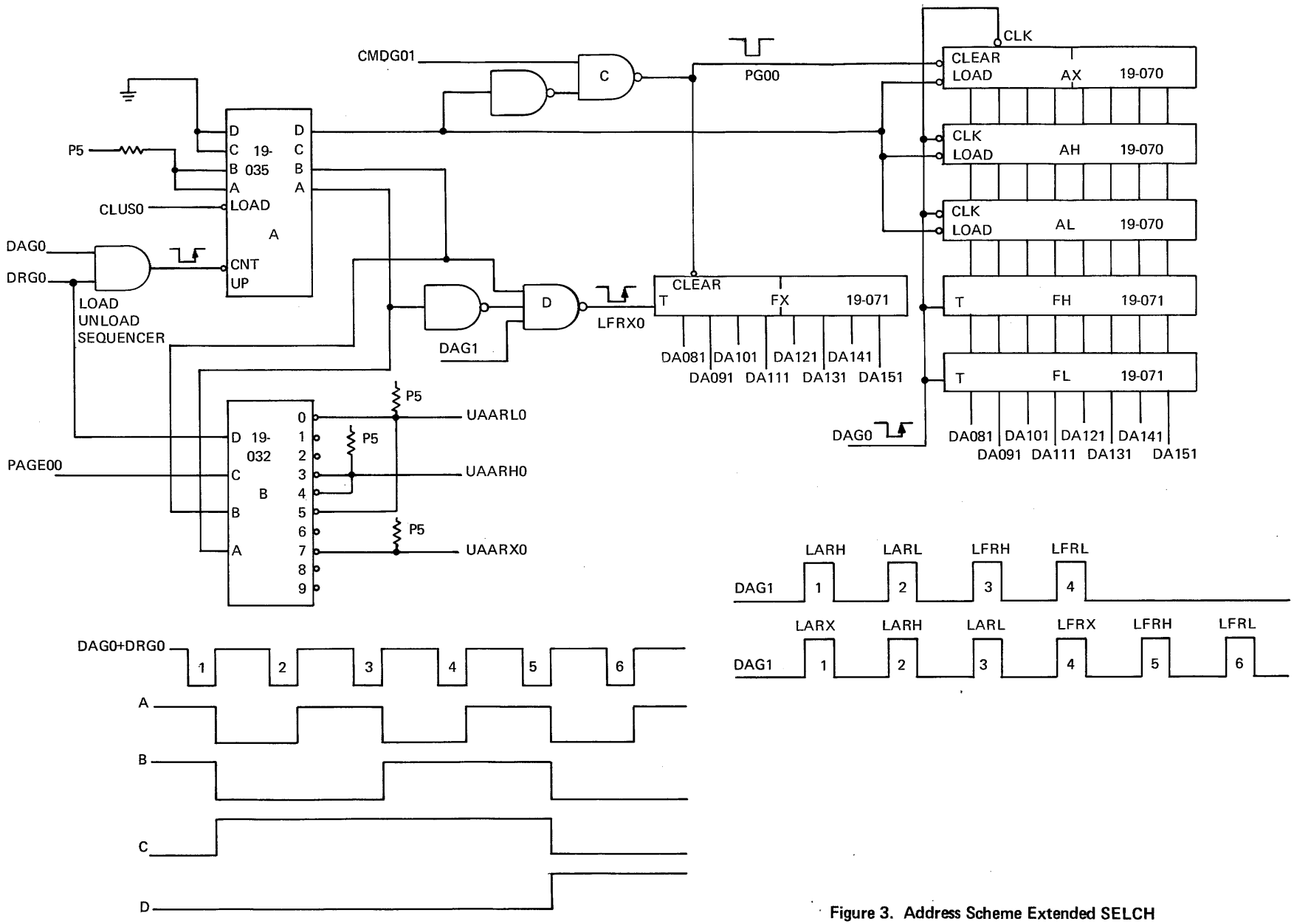


Figure 3. Address Scheme Extended SELCH

If the Extended Address Read Command bit is set, three Data Requests (DRs) are required to read back the final address from the Auxiliary Address Register. In this case, flip-flop A54 (6C7) is set and input C of Decoder A157 (6C4) is high. The remainder of the operation is the same as described previously.

If a Memory Write operation is desired, an Output command with Bit 10 set must be issued to set the Write flip-flop (4E6). Since the Write flip-flop is reset by the Data Available/ Requset Gate (DARG1) (4A6) whenever a DA or DR is sent to the ESELCH (set up procedure), no command is necessary to initiate a Memory Read operation.

Data transfer commences with a GO command from the Processor, which is an Output command with Bit 11 set. The GO command sets both the BUSY (4E3) and MSC (4E4) flip-flops. The setting of the BUSY flip-flop causes an End of Busy Set pulse (EBS1) (4N3) to be generated. This pulse is generated from the falling edge of BSY0 (4F3), and is used by the branch gate circuit to initiate the transfer cycle. The busy latch circuit remains set until the ESELCH detects the termination of transfer and its state is presented to the program via Bit 12 of the Sense Status byte.

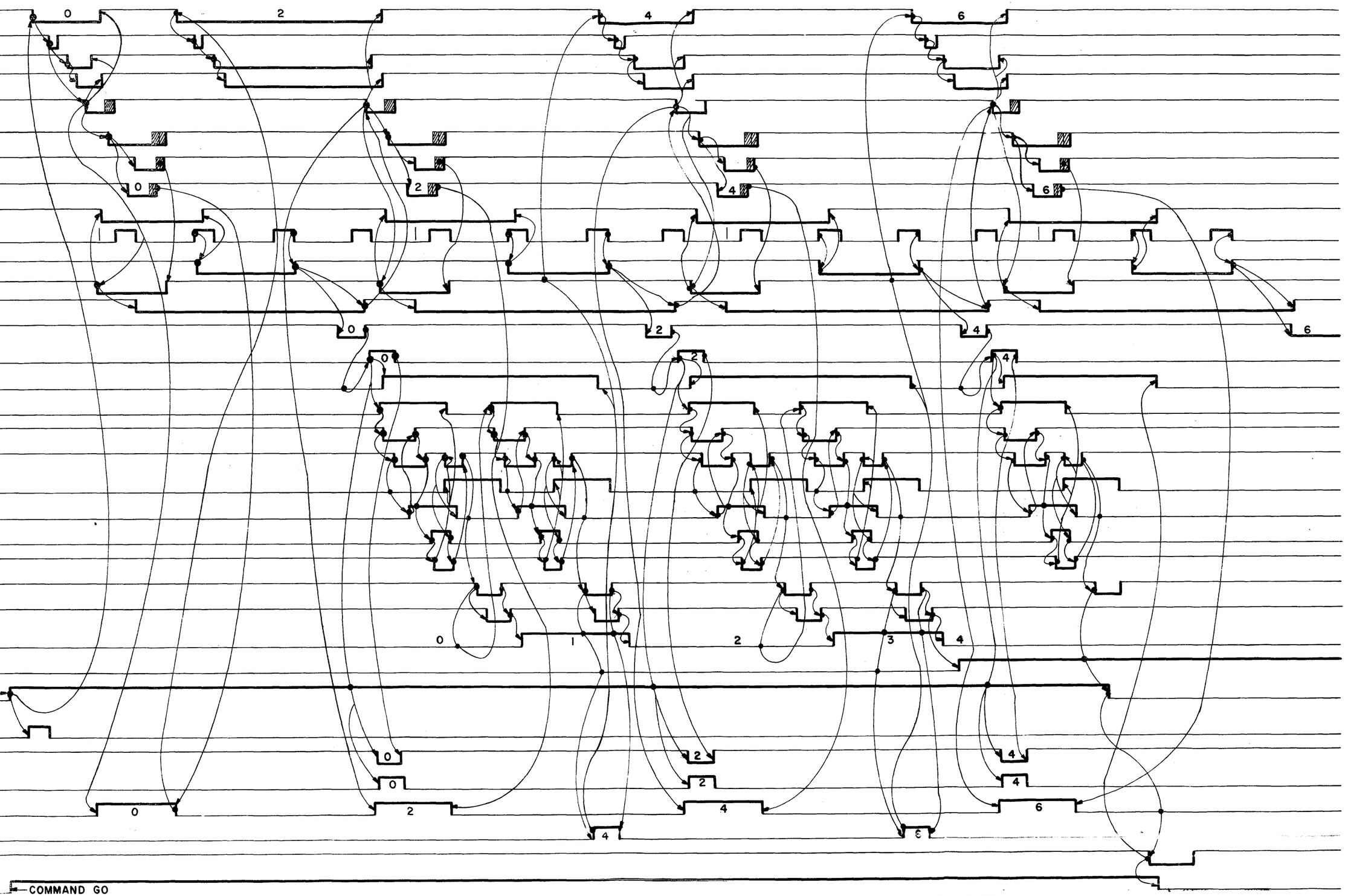
The Multiplexor ESELCH Control (MSC) flip-flop is reset by SCLR0A (4A5) or by addressing the ESELCH i.e., Set Gate active (SGAD1) (4A5), when the Busy flip-flop is reset. The resetting of the MSC flip-flop, MSC0 active, clears any pending interrupt in the ESELCH (8C5).

4.3 Extended Direct Memory Access Bus Control Circuit

Extended Direct Memory Access Bus Control timing relationships are shown in Figures 4 and 5 timing diagram for Memory Read Byte mode and Memory Write Byte mode respectively. An ESELCH request for memory is started by activating Set Request (XREQ0) (9M2). XREQ0 is activated by the branch gate circuit (8M1:8M8) when either the ESELCH bus has received a halfword of data from the device or, in the Memory Read mode, whenever the Memory Data Register (MDR) is available to accept the next halfword.

If the Select flip-flop (9G2) A62 is reset, the memory is not busy (M0BZ0:M3BZ0) (9F6) and if REQ1 (9M3) is active, XREQ0 is active. When the EDMA Bus receives the XREQ0, a Queue pulse (QUE0) (9A2) is sent to the ESELCH. The QUE0 pulse resolves contention for the bus by freezing the request status (9C2:9E2) It then sends a Receive Priority Chain pulse (RPC0) (9A3). The QUE0 pulse sets Contention flip-flop A39 (9E2) in all requesting devices. The highest priority queued device then captures the RPC0 pulse, sets the A62 flip-flop (9D2), and does not propagate the Transmit Priority Chain pulse (TPC0) (9H3) to the next device. If the ESELCH is requesting local memory, Local Memory Request Queued (LMRQ0) (9G1) is sent to the EDMA Bus at this time. If the EDMA Bus is not busy, a Start of Transmission pulse (SOT0) (9C9) is sent to the ESELCH. SOT0 then sets a Select flip-flop (9G2) which in turn removes XREQ0 and activates Memory Busy (MXBZ0) (9F6). Once the Select flip-flop is set, the SEL0 (9B7) enables the oscillator circuit (9D6) and the counter (9D8) starts counting. If it is in the Memory Read mode, Address MAX121:151 and MA001:151 (6G1:6G8) is presented to the EDMA Bus as DMX120:150 and DMA000:150 (6N1:6N7) and a Load (LOAD1) (9J8) signal strobes the address into the Processor. At the same time, an End of Transmission pulse (EOT1) (9L7) is sent to indicate to the EDMA Bus that the ESELCH has finished the transmission. EOT0A (9C4) fires a one-shot and resets the Select flip-flop and EDMA Bus control cycle is finished. In the Memory Write mode the operation is the same as in the Memory Read mode except that two consecutive LOAD1s (9J8) are sent. The first one is for the address and the second is for the data. Figure 6 shows the EDMA Bus control timing.

XREQO
QUEO
RPCO
LMRQO
SOTO
DATA BUS
LOADO
EOTO
*REQO
*CLKI
*ERO
MOBZO
BHO
ANSO
EMXI
BACTI
SXI
PSRO
PSYNO
DEVICE BUSYI
DXI
ENGI
PDAO
EDXO
TAARO
AARI9I
MCHI
COMMAND GO
DBSYI
EBSI
LDBO
LDBI
SELI
RBAI
SATNO
BSYI



*IN PROCESSOR

Figure 4. ESELCH Memory Read Byte Mode, Transfer Five Bytes

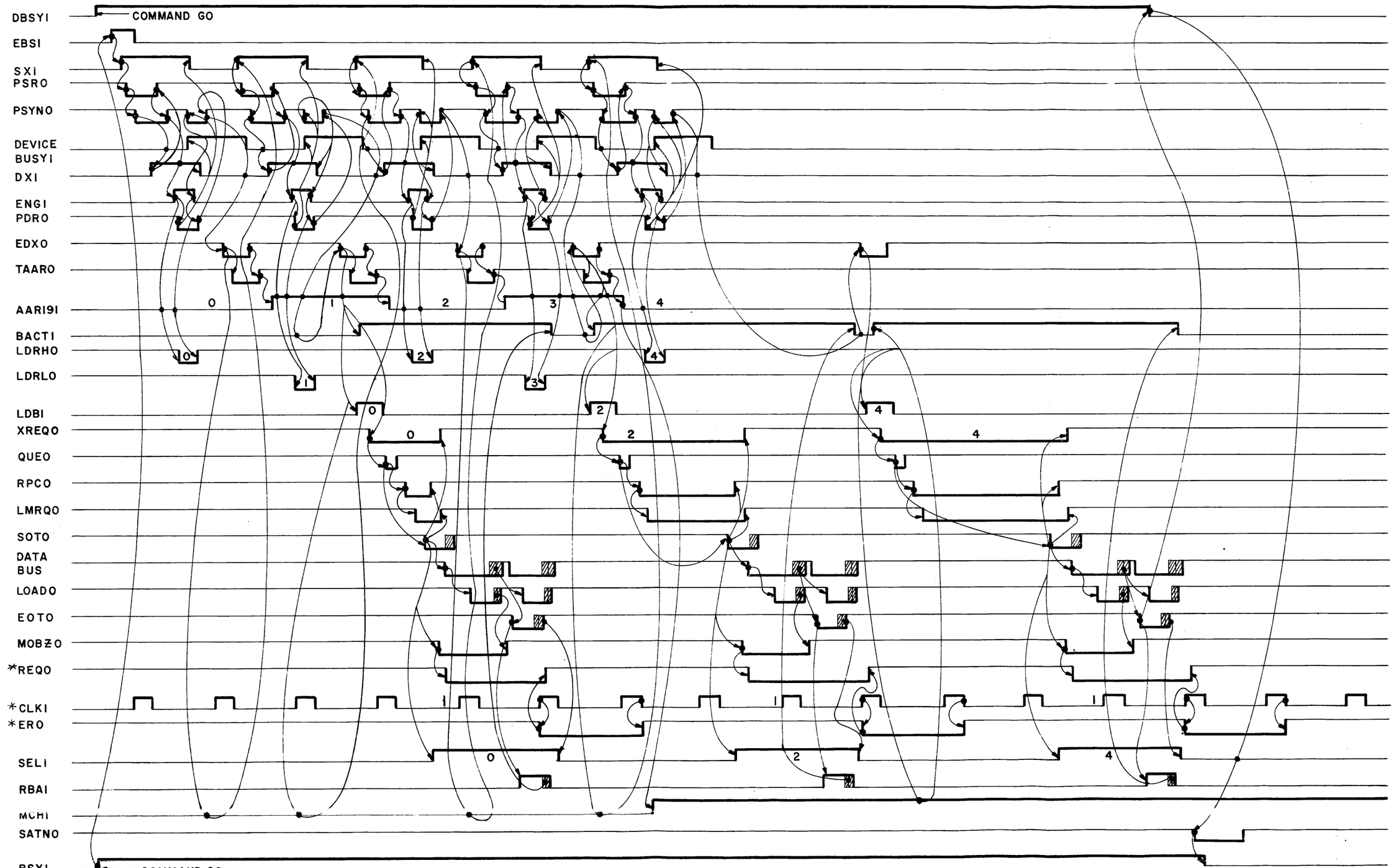
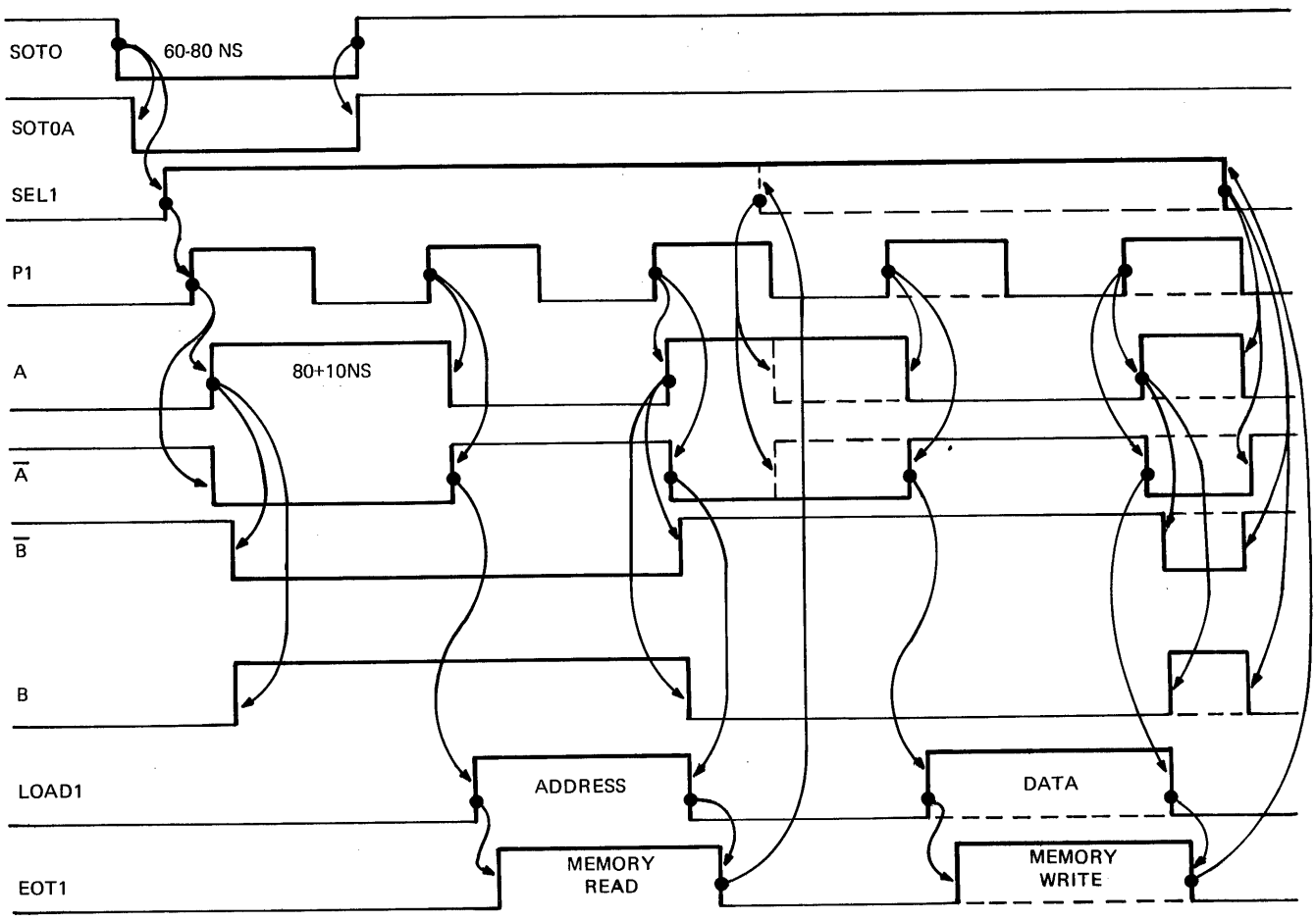


Figure 5. ESELCH Memory Write Byte Mode, Transfer Five Bytes



NOTE: DOTTED LINES FOR MEMORY READ

Figure 6. Extended Direct Memory Access (EDMA) Control Timing

4.4 Address Register and Auxiliary Address Register

The Address Register (6F1:6F8) and the Auxiliary Address Register (5B3:5N3) each consist of five four-bit counters. These registers are loaded by the Processor from Data Lines D080:150 (2A5 and 2A8), under control of the Load/Unload Sequencer (6C4) with the starting address from which the block transfers is to begin. The contents of the Address Register is gated onto the EDMA Bus Data Lines DMX120:150 and DMA000:150 (6N1:6N7) whenever the ESELCH is selected (SEL0A at 6L1 controls). The Address Register is incremented twice with each memory transfer by EOT0A and END0 (6D6). The Auxiliary Address Register (5B3:5N3) keeps track of the transfer between the ESELCH and device. This register is incremented, by one, for each byte of data transferred by Toggle Auxiliary Address Register (TAAR0)(5B1). When the transfer is in the Halfword mode, TARR0 is generated twice for each transfer. The outputs of the Auxiliary Address Register are used by the match circuit to determine the end of the data blocks. It's contents may be examined, via the program, by issuing two or three consecutive DRs to the ESELCH when the sequencer is initialized. In addition, AAR191 (4H8) is used in the Byte Transfer mode to determine whether the byte being transferred is odd or even, for byte steering. Carry Out from the most significant stage of the Auxiliary Address Register (5M1) terminates the transfer, clear Busy (4F1), when a transfer is attempted past the maximum address. This feature prevents 'wrap-around' in memory.

4.5 Final Address Register

The Final Address Register (FAR) is implemented by five quad latches (5B5:5N5). The register is loaded by SETAAR0 (5B1) when a GO command is executed. The outputs of this register are used exclusively by the match circuit to determine when the final address of the transfer is reached.

4.6 Memory Data Register and Data Buffer

The Memory Data Register (Sheet 7) is a 16-bit register composed of 16 edge triggered flip-flops. In the Memory Read mode, the data is toggled on the leading edge of Controlled Answer (CANS0) (7A9). During a Memory Write, data is toggled into the flip-flops on the trailing edge of the Load Data Register High (LDRH0) (7A9) or Load Data Register Low (LDRL0) (7H8).

As soon as the Memory Data Register is loaded, if the Data Buffer is empty as determined by the inactive state of the Buffer Active flip-flop (4G2), the contents of the Memory Data Register are loaded into the Data Buffer by Load Data Buffer (LDB1) (7A9). Information present in the Data Buffer is, in turn, either written into memory via EDMA Bus Data Lines DMA000:150 or sent to the device on Private Data Lines PD000:150.

4.7 Data Transfer Circuit

Refer to Figure 4 for Memory Read Byte mode timing diagram and Figure 5 for Memory Write Byte mode timing diagram. Both timing diagram show the timing of five byte transfer in the Byte mode.

A GO command to the ESELCH sets the Busy flip-flop (4E3) which generates the End of Busy Set pulse (EBS1) (4N3).

In the Memory Read mode, XREQ0 (9M2) is generated by Command GO (CMDG0) (9K4), thus a request for memory is initiated. When the halfword of data is present in the Memory Data Register, the End of Memory Transfer pulse (EMX1) (8L7) becomes active and the branch gate circuit once again requests memory and generates Set Status Transfer (SSX0) (8R4) and Load Data Buffer (LDB1) (9N8). These signals initiate the transfer to the device and load the Data Buffer respectively.

SSX0 sets the Status Request flip-flop (4C6) which activates the Private Status Request control line (PSR0) (4F6) to the active device on the private ESELCH Bus. This Status Request examines the four least significant bits of the status byte. If any of the three least significant bits (EX, EOM, or DU) are set, the transfer is terminated by resetting the Busy flip-flop (4E2). Assuming that each of these status bits remain reset for the remainder of this discussion. With Bit 12 (Busy) of the status byte reset, the Data Transfer flip-flop becomes set (4C8). Data transfer (DX0) (4D8) inhibits the generation of PSR0, which causes Private Sync (PSYN1) (4N4) from the device to become inactive. This enables Engage to go high (ENG1) (4G8), which allows the Private Data Available control line **(PDA0) (4J6) to become active.** The Private Data Available/Request signal (PDAR1) (4A6), generated whenever a Private Data Available (PDA0) or Private Data Request (PDR0) signal is active, clears the Status Request flip-flop. Upon receipt of Sync from the device, PSYN1 active, the Data Transfer flip-flop becomes reset and ENG1 goes low, disabling PDA0. When the Sync is removed by the device, an 80 nanosecond End of Data Transfer pulse is generated (EDX0) (4N9) which increments the Auxiliary Address Register and is used by the branch gate circuit to generate a SSX0 which starts the sequence again. When EDX0 and AAR191 are both active, Reset Buffer Active (RBA0) (8R3) is generated. It resets the Buffer Active flip-flop (4G2) and requests the memory again (9K4). This cycle continues until termination of the transfer is detected.

In the Memory Write mode, WT1 active (4F5), EBS1 (8K4) is used to generate SSX0, and the branch gate circuit directs the loading of a halfword of data into the Data Buffer before a memory request is made. The transfer of data from the device is the same as described in the Memory Read mode, except that ENG1 is used to generate the Private Data Request control line (PDR0) (4J5) rather than PDA0. Data from the device is loaded into the Memory Data Register on the trailing edge of either Load Data Register High (LDRH0) (4K8) or Load Data Register Low (LDRL0) (4J7), depending on which eight bits are being loaded. In the Halfword Transfer mode, both LDRH0 and LDRL0 are generated simultaneously. With WT1 active, the generation of EDX1 is delayed by activating the clear input to the one-shot (4L9) when the Buffer Active flip-flop is set (BACT1) (4G9), if either the transfer to the device is on an odd boundary or when a Match is detected (MCH0) (5H9). This prevents the reloading of the Data Buffer before the last halfword has been written into memory.

4.8 RACK0/TACK0 Contention Circuit

The ESELCH directs the propagation of the Acknowledge signal to lower priority devices on the Multiplexor Channel Bus as well as devices on the private ESELCH Bus. If the ESELCH Attention flip-flop (8C5) is set, the ESELCH captures the Receiver Acknowledge signal (RACK0) (8A4), places its device address on the data lines and returns Sync to the Processor, Attention Sync (ATSYN0) (8H3) active. If the Attention flip-flop is reset, RACK0 is propagated as either Private Transmit Acknowledge (PTACK0) (8G2) or Transmit Acknowledge (TACK0) (8G1). Since devices on the private ESELCH Bus have a higher interrupt priority than devices below the ESELCH on the MPX Bus; if the Private Attention line is active (PATN0) (8A3), PTACK0 is generated rather than TACK0. Note that when MSC1 is low (8C2), PATN0 is disabled so that a device on the private ESELCH Bus may not interrupt the Processor while the ESELCH is active.

4.9 Strap Options for Address Space Allocation

Address space allocation for the four memory banks is determined by strap options in the ESELCH. Each memory bank's address space must be zero or a multiple of 64K bytes up to a maximum of 1,024K bytes for the 8/32 Processor or a maximum of 256K bytes for the 7/32 or 7/32 C Processor. Address assignment must be contiguous and the four memory banks are assigned address space in ascending order.

In the ESELCH printed circuit board, there are two decoders, A03 and A04, (8C6, 8C7) which decode the extended address bits (four most significant address bits). Each output of the decoders allocates 64K bytes of memory. The 16 outputs with wire wrap stakes are marked 0:15. The four wire wrap stakes next to them are marked M00, M10, M20 and M30 (8D5, 8D8) denoting the four memory banks. The address space allocation should be strapped according to system configuration. All non-existent memory locations should be strapped to the stake marked NE (Non-Existent) Memory. See Figure 7 for details.

5. INSTALLATION CHECKS

Before attempting any maintenance or testing, insure that the necessary back panel modifications and ESELCH board option strapping have been made in accordance with the 02-328A20 ESELCH Installation Specification.

To insure a 2,000,000 Byte/Second transfer rate in the Halfword Transfer mode, it is necessary to limit the maximum delay between PDA0, PDR0, and PSR0 and the return of Sync from the device (PSYN0) to 50 nanoseconds. In addition, the EDMA Bus must have only one active DMAC (i.e., the ESELCH), the device must be ready for the next byte of data, Busy status bit reset, whenever a Status Request (SR) is made. Field testing of this device is contingent upon the user having the appropriate software and hardware available with which to exercise the ESELCHs. Refer to Test Program Description 06-161 a configured requirements. There are no adjustments associated with this device.

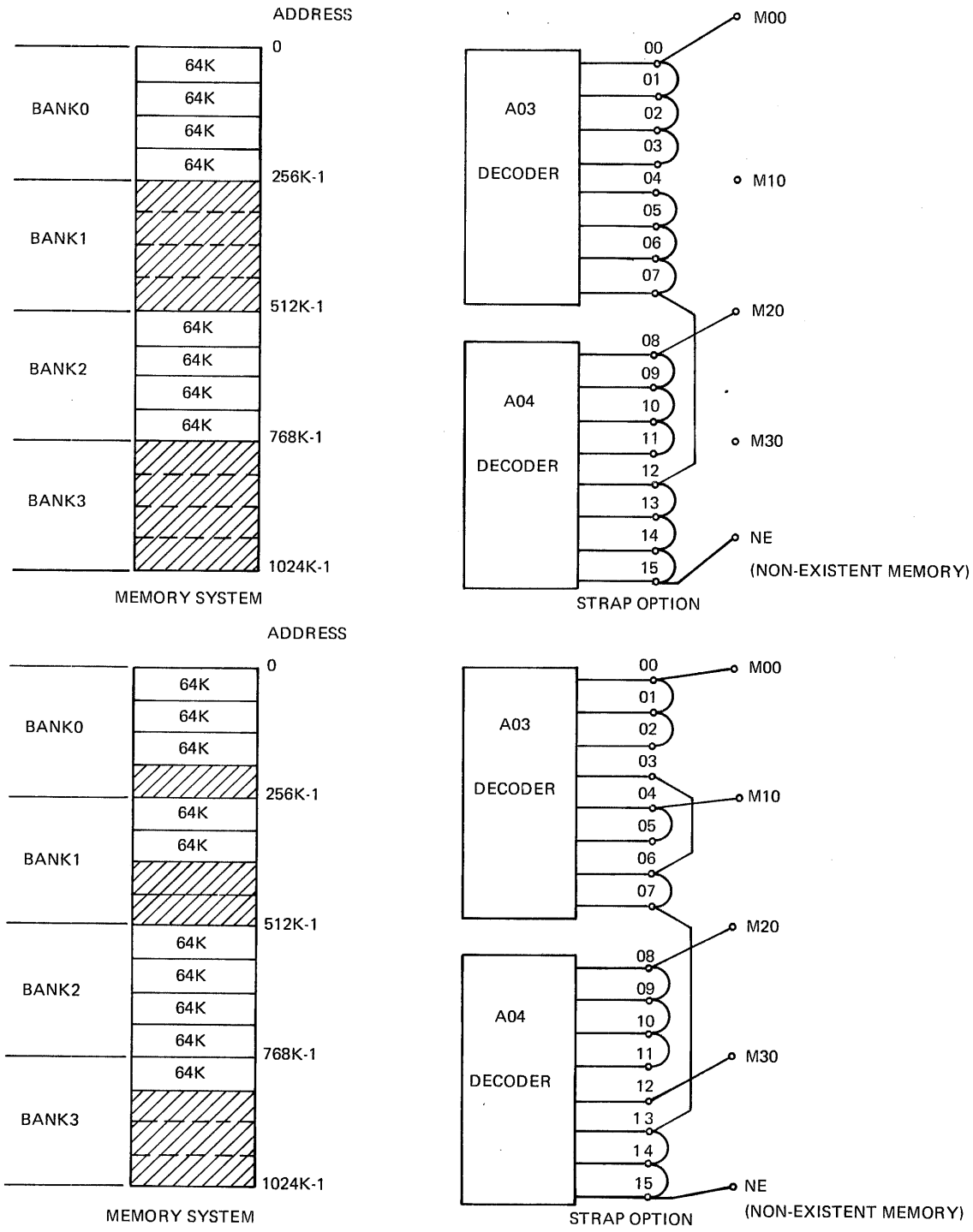


Figure 7. Address Allocation

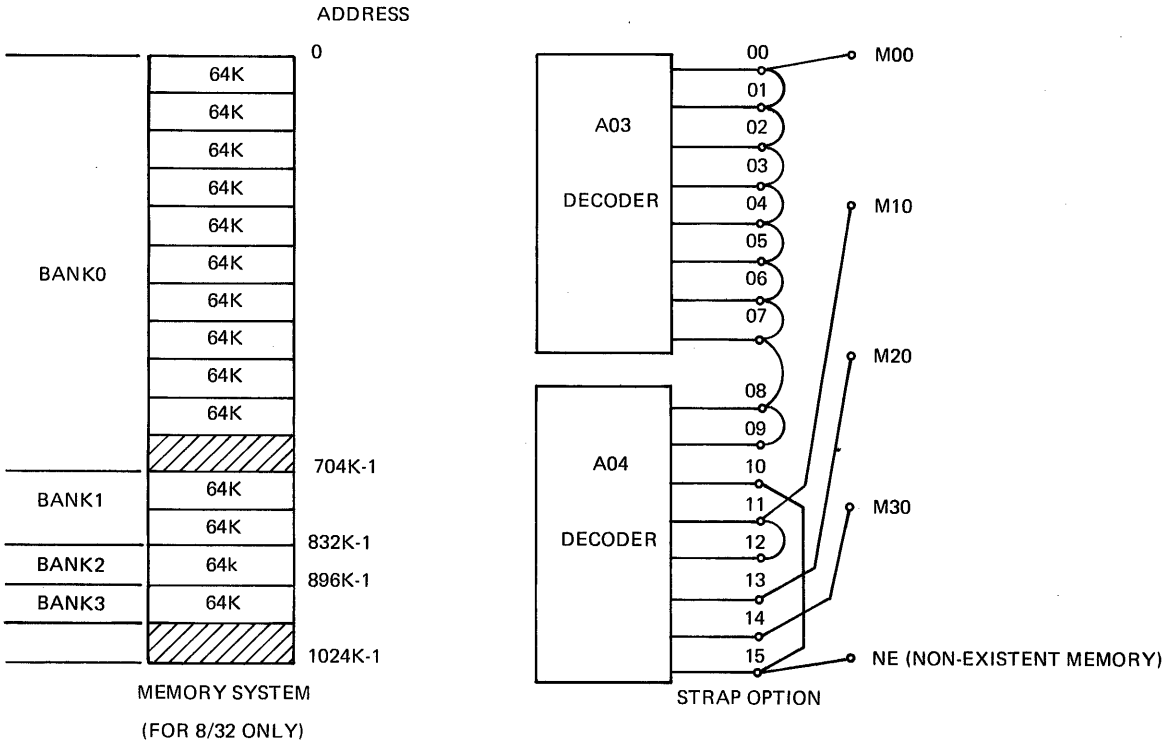


Figure 7. Address Allocation (Continued)

6. MNEMONICS

The following list provides a brief description of each mnemonic found in the ESELCH. The source of each signal on Functional Schematic 02-328D08 is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
AAR001:191	Outputs from the Auxiliary Address Register	5A6-5N6
AD1	Address-active when ESELCH is addressed	3N9
ADDA0	Address and Data Control-in Memory Read mode, LOAD0 strobes the address to the EDMA Bus. In Memory Write mode, the first LOAD0 strobes the address and the second LOAD0 strobes data to the EDMA Bus.	9J9
ADRS0	Address control line from MPX-Bus	4K7
ANS0	Answer control line-sends data from memory to ESELCH	6N9
ATN0	Attention-Attention to Processor	8E3
ATSYN0	Attention Sync-generated by an Acknowledge Attention from the Processor	8H3
BACT1	Buffer Active-indicates that valid data is present in the data buffer	4H1
BSY1	Busy-indicates data transferred in progress	4F3
CANS0	Controlled Answer-to insure that the answer is coming from the right memory.	8J6
CBSY0	Clear Busy-terminates transfer when a match or a non-existent memory is detected	8R5
CL070	Power Failure Clear	4K5
CLG1	Control Line Gate-gates private control lines	2G2
CLGA1	Control Line Gate-same as CLG1 except used to assure a 100 nanosecond delay between ADRS, CMD, DA, and the Data Lines	2G2
CLUS0	Clear Load/Unload Sequencer-clears sequencer	4F2
CMDGO0	Command GO-starts the whole sequence	4H4
CMD0	Command control line from MPX-Bus	4K6
CO0	Carry Out of the Auxiliary Address Register-Prevents memory wrap-around	5M1
D000:150	Data Lines from MPX-Bus	2A5-2A8 3A7-3A9
DA0	Data Available control line from MPX-Bus	4K6
DB001:151	Outputs from Data Buffer	7F1-7F8 7N1-7N8

MNEMONICS	MEANING	SCHEMATIC LOCATION
DBSY1:	Delayed Busy-to insure that the memory cycle is finished before sending out an interrupt	4L1
DLG1	Data Line Gate-gates data line and private data lines	2R2
DMA000:170	EDMA Bus Data Lines	6N2-6N9
DMX120:150	EDMA Bus Extended Data Lines	6N1
DR0	Data Request control line from MPX-Bus	4K5
DX1	Data Transfer-Data Transfer flip-flop	4D8
EBS1	End of Busy Set-signals the start of a ESELCH transfer	4N3
EDX0	End of Data Transfer-signals the end of a device transfer	4N9
EMX1	End of Memory Transfer-signals the end of a memory transfer	8L7
ENG1	Engage-gates either PDA0 or PDR0	4G8
EOT0	End of Transmission-to tell EDMA Bus that transmission is ended.	9L8
FH001:071	Final Address Register High-Final Address Bits 00:07	5G5-5K5
FL001:071	Final Address Register Low-Final Address Bits 08:15	5A5-5E5
GETBUS0	ESELCH gets the EDMA Bus in Memory Read mode	8J5
LDB1	Load Data Buffer-loads data into Data Buffer	8N8
LDRH	Load Data Register High-loads Data Bits 00:07	4K8
LDRL0	Load Data Register Low-loads Data Bits 08:15	4J7
LFRX0	Load Final Address Register Extended Bits 00:03	6D6
LMRQ0	Local Memory Request Queued	9G1
LOAD0	Load control line-loads Data or Address to EDMA Bus	6N9
M00:30	Memory Banks 0:3	8D6-8D8
M0BZ0:M3BZ0	Memory Busy	9F6
MA001:151	Memory Address Bits	6G3-6G7
MAX121:151	Extended Memory Address Bits	6G1
MCH1	Match-indicates a match between the Auxiliary Address Register and Final Address Register	5K9

MNEMONICS	MEANING	SCHEMATIC LOCATION
MMF1	Memory Malfunction	7K3
MSC1	Multiplexor-ESELCH Control flip-flop	4F5
PADRS0	Private Address control line to ESELCH Bus	4N7
PAGE01:11	Pages 01:11-encode M00:M30	8G6-8G7
PATN0	Private Attention from ESELCH Bus	8A3
PCL070	Power Failure Clear to ESELCH Bus	4N5
PCMD0	Private Command control line to ESELCH Bus	4N6
PD000:150	Private Data Lines-ESELCH Bus	2N5-2N9 3H7-3H9
PDA0	Private Data Available control line to ESELCH Bus	4J6
PDR0	Private Data Request control line to ESELCH Bus	4J5
PF1	Memory Parity Failure	7K4
PG00	Page Zero-indicates that four WDs are used to Set up Starting and Final Addresses, i.e., the Final Address is no greater than 64K Bytes.	6A1
PHW0	Private Halfword control line from ESELCH Bus	2D1
PSR0	Private Status Request control line to ESELCH Bus	4F6
PSYN0	Private Sync from the ESELCH Bus	4K4
PTACK0	Private Transmit Acknowledge to the ESELCH Bus	8H2
QUE0	Queue-to resolve contention for EDMA Bus	9A2
RACK0	Receive Acknowledge from MPX-Bus	8A4
RBA0	Reset Buffer Active-reset Buffer Active flip-flop	8R2
RBA0A	Controlled Reset Buffer Active-the leading edge clears the Buffer Active flip-flop in Memory Raed mode and the trailing edge clears the Buffer Active flip-flop in the Memory Write mode.	8R3
RPC0	Receive Priority Chain from EDMA Bus	9A3
SATN0	Set Attention flip-flop	4N1
SBACT1	Set Buffer Active-set Buffer Active flip-flop	8R6
SCLR0	System Clear-initialize signal	3K9
SDX0	Set Data Transfer flip-flop-if no error status	4F1

MNEMONICS	MEANING	SCHEMATIC LOCATION
SEL1	Select-ESELCH gets the EDMA Bus	9H2
SELSTS1	Selch Status Command Bits	4C3
SETAAR0	Set Axuiliary Address Register	3R6
SGAD0	Set Gate-sets Address flip-flop	2J6
SOT0	Start of Transmission-to tell the ESELCH to start transmitting an address and data to the EDMA Bus	9C9
SR0	Status Request control line from MPX-Bus	4K4
SSX0	Set Status Transfer-sets the Status Request flip-flop	8R4
SX1	Status Transfer-Status Request flip-flop	4D6
SYN0	Sync to MPX-Bus	3R7
TAAR0	Toggle Auxiliary Address Register-increments Auxiliary Address Register	8N2
TACK0	Transmit Acknowledge-to lower priority device on the MPX Bus	8H1
TPC0	Transmit Priority Chain from EDMA Bus	9J3
UAARH0	Unload Auxiliary Address Register High-unload Auxiliary Address Register Bits 04:11	6D4
UAARL0	Unload Auxiliary Address Register Low-unload Auxiliary Address Register Bits 12:19	6D4
UAARX0	Unload Auxiliary Address Register Extended-unooad Auxiliary Address Register Bits 00:03	6D5
WT1	Write flip-flop	4F5
XREQ0	Request-request EDMA Bus for service	9M2

TEST AID

M49-410
TEST AID
INFORMATION SPECIFICATION

1. INTRODUCTION

This Information Specification covers installation, operation, and maintenance of the M49-410 Test Aid (02-276) and the associated logic in the Processor. Refer to 02-276D08 for schematics of the M49-410 Test Aid.

2. GENERAL DESCRIPTION

The Test Aid consists of a switch display panel and a 17-283 logic card which attaches to the following boards:

35-446 CPU-HI Model 74 Processor
35-446F01 and 35-446F02 CPU-HI 7/16 Basic Processor
35-524 CPU-B Model 7/16 HSALU Processor
35-523F01 and 35-523F02 CPU-B Model 7/32
35-624F01, F02, F03 CPU-B Model 7/32C Processor

The Test Aid provides the ability to examine the address of the micro-code and to stop Processor clocks at option.

3. INSTALLATION

This section provides the information necessary to install the Test Aid on the Processor. The 02-276R01 or higher revision level Test Aid may be used on the Model 74, 7/16 Basic, 7/16 HSALU, 7/32, and 7/32 C Processors. The 02-276R00 Test Aid may be used on the Model 74 and the Model 7/16 Basic. The installation procedure is:

1. Remove the display from the chassis.

2. Place Test Aid logic card over pins on CPU-HI board or CPU-B board (installed in Slot 6 of the Processor back panel, refer to Figure 1) and press down until Test Aid logic card rests on spacers on the Processor board. The switch/display panel assembly may be placed on a table or mounted on the chassis as shown in Figure 2.

3. On the 7/16 HSALU Processor, a jumper must be installed between TP1 on the 35-544 CPU-B board and TP2 on the 35-522 CPU-A board.

4. On the 7/32, a jumper must be installed between TP1 on the 35-523F01 or F02 CPU-B board and TP2 on the 35-522 CPU-A board.

5. On the 7/32 C Processor, a jumper must be installed between TP1 on the 35-625F01, F02, or F03 CPU-B board and TP2 on the 35-624 CPU-A board.

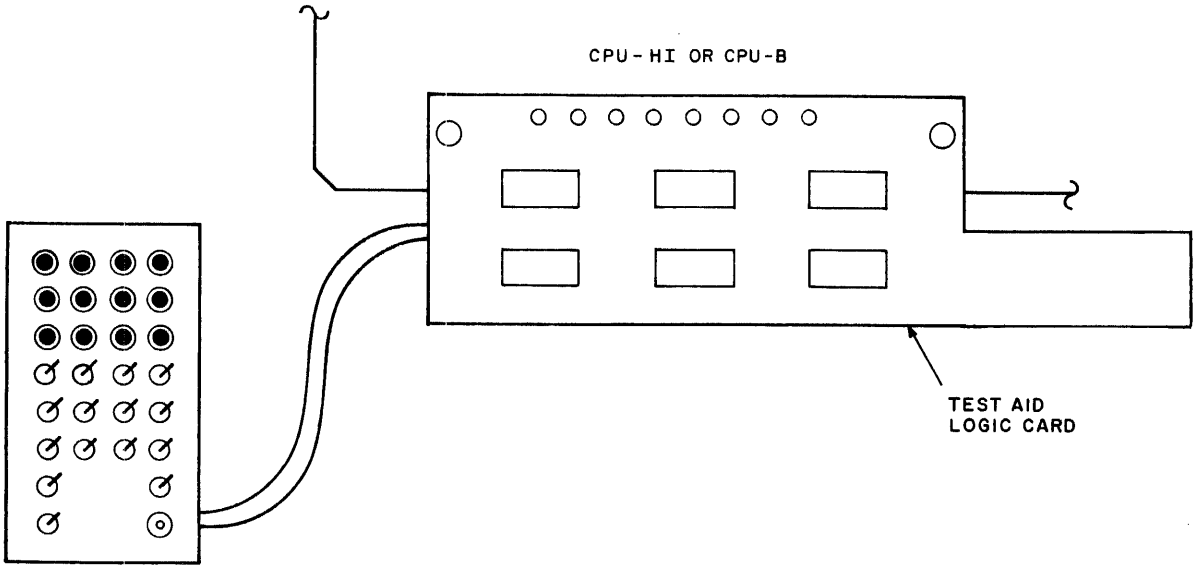


Figure 1. Test Aid Installation

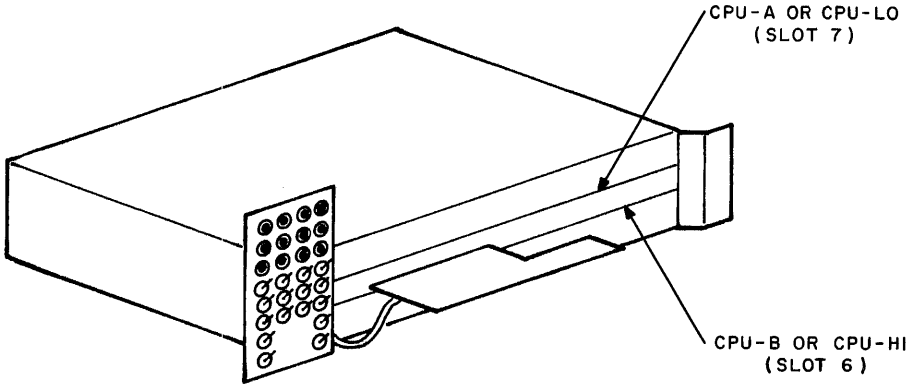


Figure 2. Switch Panel Mounting

4. POWER

Power and ground are supplied by the Processor board. There are no other power requirements.

5. OPERATION

Refer to Figure 3 during the operating description. The 12 Light-Emitting Diodes (LEDs) numbered 4:15 display the contents of the ROM Address Register. The numbers assigned to the LEDs correspond to the ROM Address Register bits. The 12 toggle switches labelled 4:15 provide the ability to set-up a match address. The Test Aid logic stops the Processor clocks when the selected "match address" is in the ROM Address Register and the Address Match switch is in the ON (up) position.

6. ADDRESS MATCH SWITCH

After selecting an address on the Address switches, place the Address Match switch in the ON (up) position. When the ROM Address Register of the Processor contains the "match address", the Processor clocks are stopped on the next clock. The Address Match switch feature can also be used to interrupt and continue micro-code loops. Follow the procedure for address matching. Select an address within a micro-code loop. Once the match has been found, depressing the Clock Advance (ADV) switch once allows the micro-code to go through the loop and match on the selected address again.

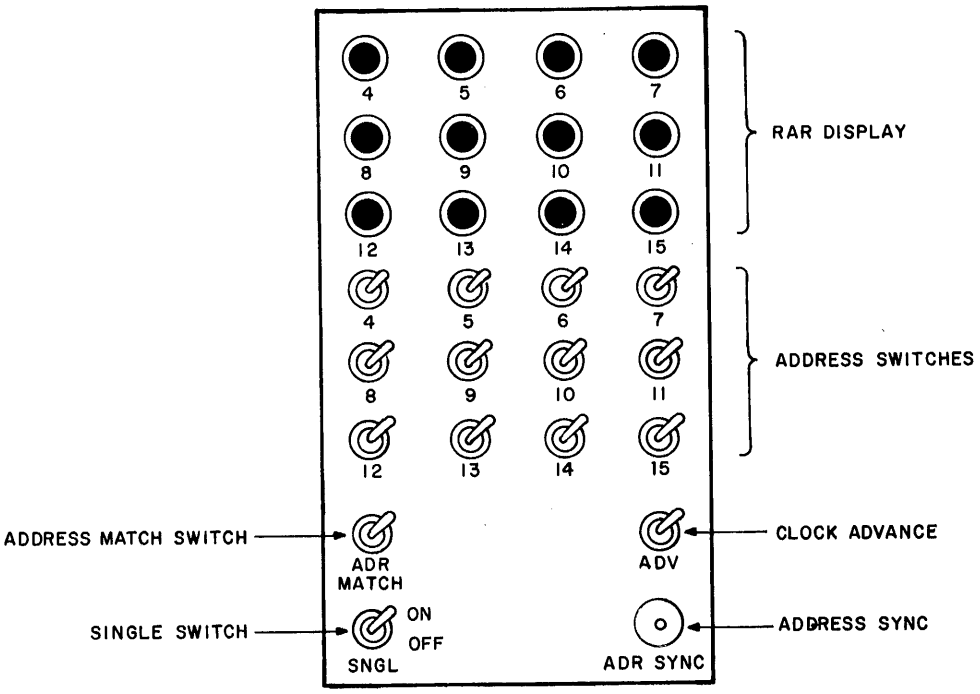


Figure 3. Switch Panel

NOTE

The LED display in most cases is one increment ahead of the match address. The micro-code instruction at the address selected has been executed or is one clock into execution when the match occurs and the Processor clocks stop.

7. CLOCK ADVANCE SWITCH

The Clock Advance switch allows the Processor to generate one clock each time it is depressed when the Address Match or Single switch is in the ON (up) position.

8. SINGLE SWITCH

When the Single switch is in the ON (up) position, the Processor clocks are stopped. With this switch ON, the micro-program may be executed one micro-instruction at a time by depressing the Clock Advance switch.

9. ADDRESS SYNC

Address Sync is a BNC connector whose output is a low going signal that becomes active when the Address switches and the contents of the ROM Address Register compare. The contents of the ROM (specified by the ROM Address Register) will not be loaded into the ROM Data Register until the next Clock which loads the ROM Data Register.

10. OPTION

Pins 'A' and 'B' are normally wired together. Pin 'A' is the output of a comparator that compares the ROM Address Register and the Address switches. When they compare, the signal on Pin A goes high (+5 VDC) causing Processor clocks to stop. Removing the wire between Pins 'A' and 'B' provides a means to bring in any high active signal on Pin 'B' to stop Processor clocks. To match on any high active signal, the Address Match switch must still be placed in the ON (up) position when a match is desired. Removing the wire between 'A' and 'B' will remove the capability to stop Processor clocks on address match. See Figure 4.

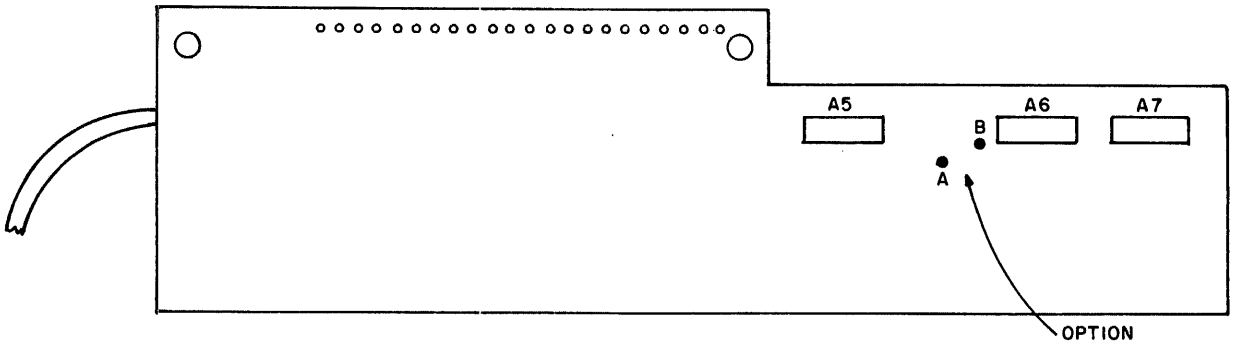
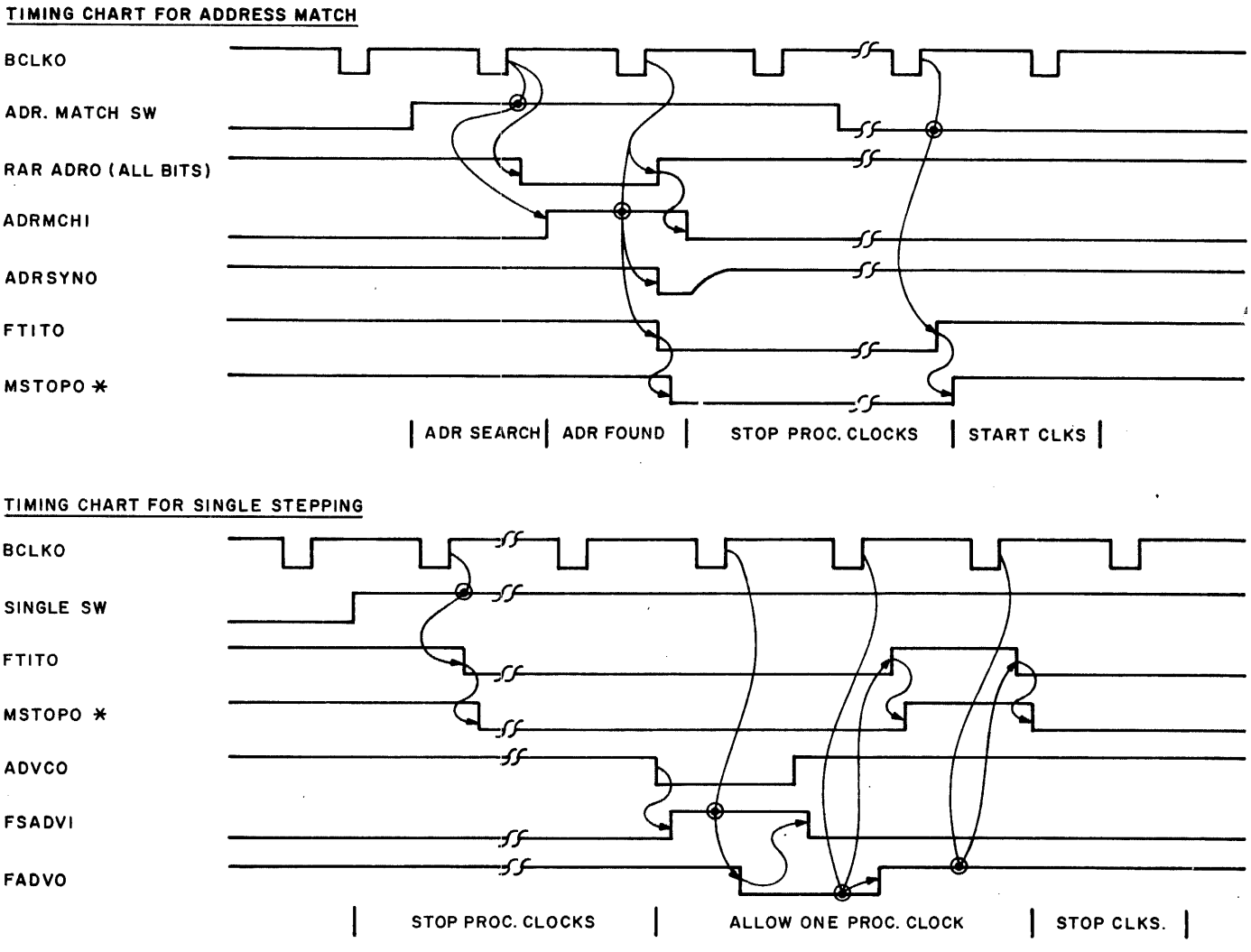


Figure 4. Option Connections

11. TEST AID MAINTENANCE

11.1 Timing

This section defines timing sequences (Figure 5) in the logic of the Test Aid and associated logic in the Processor. Refer to the Processor Functional Schematic, Clock Control sheet, for logic detail of the clock stop.



* MSTOPO IS A CLOCK STOPPING SIGNAL INTERNAL TO THE MODEL PROCESSOR.
WHEN ACTIVE ALL PROCESSOR CLOCKS EXCEPT CLKI, BCLKI AND BCLKO ARE STOPPED.

Figure 5. Test Aid Timing

11.2 Mnemonic Definitions

ADRMCH1 - This signal is active when the contents of the ROM Address Register and the Address switches are equal.

ADVC0 - Flip-flop output which goes active when the ADV switch is depressed, inactive when the ADV switch is released.

BCLK0 - Derived from the Processor. This is a clock that cannot be stopped by any clock stop in the Processor. BCLK0 width is typically 60 nanoseconds and the period is typically 250 nanoseconds.

FADV0 - When active, allows FTIT0 to be inactive for one clock period. If ADVC0 and BCLK0 are active at the same time, the FADV0 flip-flop sets.

FTIT0 - This flip-flop is reset by Single switch ON, Address Match switch ON, and a match address.

MCH04-150 - When active, indicates that a particular address switch has been selected.

RAR04-150 - ROM Address Register outputs which indicates the address of the micro-instruction to be executed on the next clock.

12. USE OF MODEL 70 EXTENDER BOARD (11-103) ON THE PROCESSOR

12.1 Hazards

All Model 70 extender boards, below revision level 11-103R02, when used to extend Processor boards, present two hazards.

1. All stiffening metal on the extender board when being plugged in becomes +5VDC. This hazard exists with either Processor board on the extender.

2. When the Test Aid is installed and the CPU-LO or CPU-A is on the extender board, a stiffening bar located on the underside of the extender board rests on top of the Test Aid logic card and forces it down possibly causing a short.

12.2 Modification

The following information describes how to modify the 11-103R01 extender board:

1. Pins 200-0, 200-1, 241-0 and 241-1 are tied into the ground bus of the extender board. These pins in the Processor are +5VDC. Both ends of the extender board tie these pins to the extender board ground but via feedthrough holes causing the ground bus to become +5VDC. Cut the copper between these feed-through holes and the extender board ground bus. Add a strap from the copper run of Pins 101-0, 101-1, 140-0 and 140-1 to the adjacent ground shield to restore the continuity of back panel ground to extender board ground.

2. Remove stiffening bar on underside of extender board. Three new clearance holes must be drilled so that the stiffening bar mounts horizontally rather than vertically. The original screws may bottom out; if so, use #4-40 x 5/8 screws. Refer to Figure 6.

   After this change is made, care should still be taken to insure that the Test Aid logic card is not shorting to the stiffening bar.

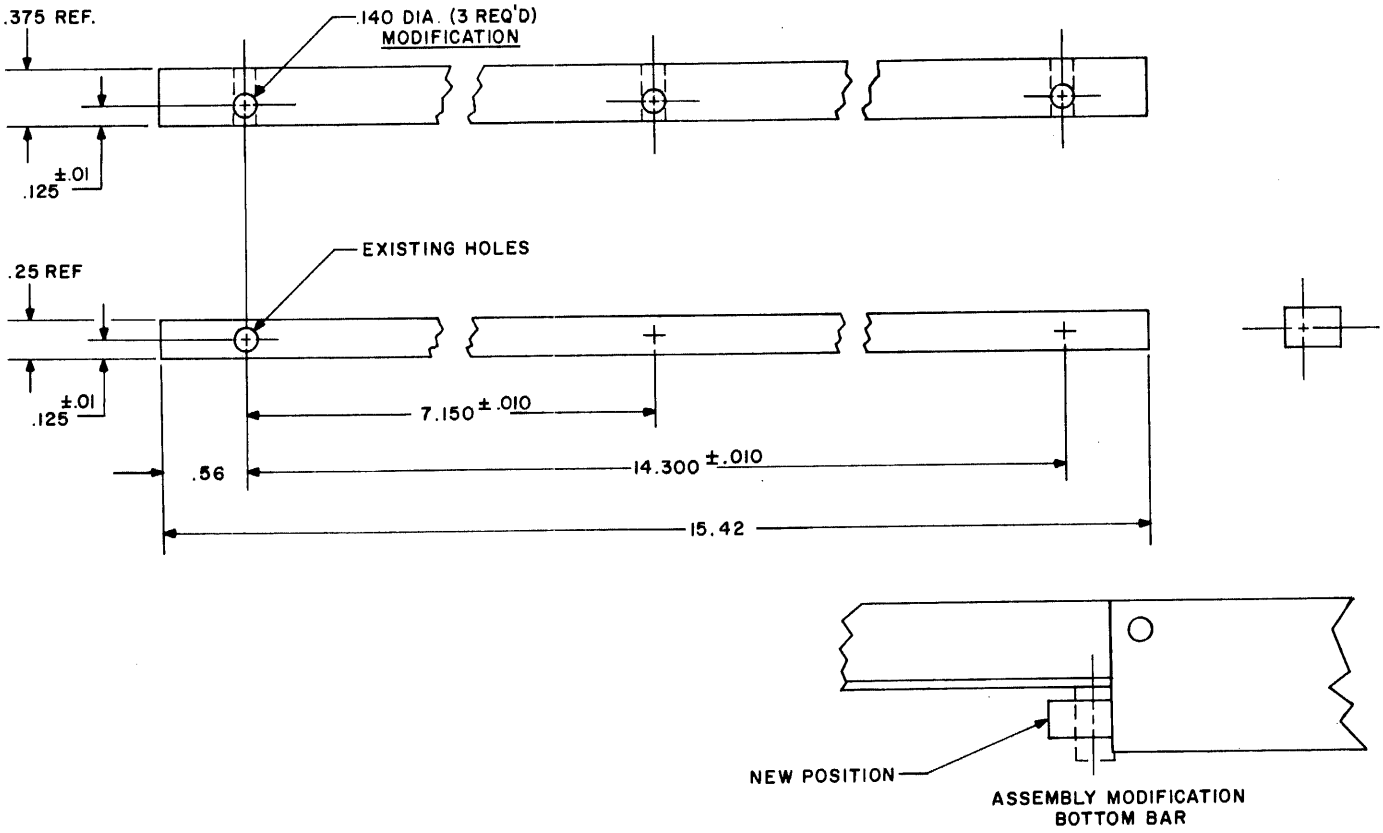


Figure 6. Stiffening Bar

MICRO-PROGRAMS

```
                        64  * IN ALL CASES WHERE A TRANSFER COULD OCCUR TO A                    73200650
                        65  * LISTING PAGE OTHER THAN THE CURRENT LISTING PAGE,                 73200660
                        66  * THE TARGET PAGE NUMBER IS SHOWN IN THE COMMENT FIELD.             73200670

000                     68          ORG   '000'                                               73200690
000     F0 0003         69          B     ILLEG           (P.3)                               73200700

                        71  * COMMON ENTRY POINT FOR ALL INSTRUCTIONS.                         73200720
                        72  *                                                                 73200730
                        73  * IN RESPONSE TO AN INSTRUCTION READ, A MAIN MEMORY              73200740
                        74  * READ IS INITIATED FROM THE LOCATION WHOSE ADDRESS              73200750
                        75  * IS (LOC). WHEN THE MEMORY DATA BECOMES AVAILABLE               73200760
                        76  * THE HALFWORD IS LOADED INTO THE USERS INSTRUCTION             73200770
                        77  * REGISTER.  IF NO INTERRUPT IS PENDING, CONTROL IS             73200780
                        78  * GIVEN TO ROUTINE "START" AT ROM ADDRESS '001'. IF             73200790
                        79  * AN INTERRUPT IS PENDING, CONTROL IS GIVEN INSTEAD             73200800
                        80  * TO ROUTINE "HELP" AT ROM ADDRESS '045'.                       73200810

                        82  *                                                                 73200830
                        83  *                                                                 73200840
                        84  * THE FLAG REGISTER IS CLEAR AND MAR & LOC                       73200850
                        85  * HAVE BEEN INCREMENTED BY TWO.                                  73200860
                        86  *                                                                 73200870
001     02 E00A          87  START   L     ARH,YSH,R1      (ARH,ARL)=CONTENTS OF GENERAL     73200880
002     01 E809         88          L     ARL,YSL,MRI     REGISTER SPECIFIED BY R2.         73200890
                        89  *                             VECTOR THROUGH DROM1. START       73200900
                        90  *                             MEMORY READ AND INCREMENT MAR     73200910
                        91  *                             AND LOC AGAIN BY TWO IF THE       73200920
                        92  *                             INSTRUCTION IS NOT RB OR SF.      73200930
```

INTERRUPT SUPPORT ROUTINES. 73200

```
                        94  * ILLEGAL INSTRUCTION OR PROTECT MODE VIOLATION *                    73200950
                        95
0005  50 A314            96  ILLEG   S     LOC,LOC,TWO     DECREMENT LOC BY TWO                73200970
0004  E4 4006            97            BT    RR,*+2          SKIP NEXT INSTRUCTION IF RR OR SF   73200980
0003  50 A314            98            S     LOC,LOC,TWO     DECREMENT BY TWO AGAIN              73200990
0006  83 0017            99            LI    MAR,'30'        (MAR)=ADDRESS OF ILLEGAL            73201000
                       100  *                                 INSTRUCTION INT. NEW PSW            73201010
0007  70 0010           101  COMIN2  C     OUT             CLEAR UTILITY, NO CONDITION         73201020
                       102  *                                 CODE BITS TO OR IN.                 73201030
                       103  *                                                                     73201040
                       104  * COMMON INTERRUPT HANDLER.  MAR CONTAINS ADDRESS OF                  73201050
                       105  * NEW PSW.  IF UTILITY SET, MR0(12:15) CONTAINS                       73201060
                       106  * CONDITION CODE FOR NEW PSW.  ENTER AT "COMIN1"                      73201070
                       107  * FROM QUEUE SERVICE INTERRUPT.                                       73201080
                       108  *                                                                     73201090
                       109  *                                                                     73201100
0008  00 3801           110  COMINT  L     MR1,PSWL        SAVE LOW PSW                        73201110
0009  00 8007           111           L     PSWL,NULL       CLEAR LOW PSW, SELECTING            73201120
                       112  *                                 REGISTER SET 0.                     73201130
000A  80 E00C           113  COMIN1  LI    YSI,14                                              73201140
000B  0D 701C           114           L     YSH,PSWH,MRD2   START MEMORY READ, NO MAC           73201150
000C  00 081D           115           L     YSL,MR1         REG,14 = OLD PSW                    73201160
000D  80 F00C           116           LI    YSI,15                                              73201170
000E  0D B00E           117           L     PSWH,MDR,MRD2   LOAD NEW PSW (0:15)                 73201180
000F  00 881C           118           L     YSH,LOCH                                            73201190
0010  00 A010           119           L     YSL,LOC         REG,15 = OLD LOC                    73201200
0011  0D B007           120           L     PSWL,MDR,MRD2   LOAD NEW PSW (16:27)                73201210
                       121  *                                 BITS 28:31 CAPTURED IN FLR          73201220
0012  7B 0098           122           C     JH+XR2+PRIV     UPDATE CONDITION CODE FROM FLR      73201230
                       123  *                                 START EXTENDED MEMORY READ          73201240
                       124  *                                 WITH MAC DISABLED.                  73201250
0013  00 B014           125           L     LOC,MDR         LOAD NEW LOC                        73201260
0014  FC 2017           126           BF    UT,TWAIT        GO TEST WAIT BIT OF PSW IF          73201270
                       127  *                                 UTILITY FLOP RESET, ELSE            73201280
0015  00 000F           128           L     FLR,MR0         COPY MR0 TO FLR THEN COPY           73201290
0016  70 0088           129           C     JH              FLR TO CONDITION CODE.              73201300
0017  E0 102F           130  TWAIT   BT    WAIT,WAIT       TO WAIT IF PSW16=1 (P.4)            73201310
0018  04 8010           131           L     NULL,NULL,TR    ELSE, FETCH NEXT INSTRUCTION        73201320
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                          133  *          MACHINE MALFUNCTION INTERRUPT                          73201340

019     70 0010           135  MMFINT   C     CUT                      CLEAR UTILITY               73201360
                          136  *                                                                 73201370
                          137  * ENTRY POINT FOR MACHINE MALFUNCTION DURING AUTO DRIVER CHANNEL   73201380
                          138  *                                                                 73201390
01A     82 0017           139  MMF1     LI    MAR,'20'                                           73201400
01B     00 7016           140           L     MDR,PSWH                                           73201410
01C     7F 0090           141           C     MW2+PRIV                 (X'00020')=PSW(0:15)        73201420
01D     00 3816           142           L     MDR,PSWL                                           73201430
01E     7F 0090           143           C     MW2+PRIV                 (X'00022')=PSW(16:31)       73201440
01F     00 8816           144           L     MDR,LOCH                                           73201450
020     7F 0090           145           C     MW2+PRIV                 (X'00024')=LOC(0:15)        73201460
021     00 A016           146           L     MDR,LOC                                            73201470
022     7F 0090           147           C     MW2+PRIV                 (X'00026')=LOC(16:31)       73201480
023     83 8017           148           LI    MAR,'38'                 ADRS NEW PSW FOR MALF       73201490
024     0D 8001           149           L     MR1,NULL,MRD2            MR1 GETS ZERO               73201500
025     0D B00E           150           L     PSWH,MDR,MRD2            LOAD PSW 0:15               73201510
026     0D B009           151           L     ARL,MDR,MRD2             ARL=NEW PSW BITS 16:31      73201520
027     FC 2029           152           BF    UT,*+2                                             73201530
028     80 8001           153           LI    MR1,8                    MR1=C FLAG QUEUE FOR AUTO DRIVER  73201540
029     70 0001           154           C     ALRM                     CONNECT ALARM REGISTER.  WHEN     73201550
                          155  *                                       LOAD PSWL, PSW16:27 GET ZERO      73201560
02A     00 0807           156           L     PSWL.MR1                 FLR GETS 0 OR 8 PLUS ALARM BITS   73201570
                          157  *                                       PSW21 IS DELIBERATELY RESET SO    73201580
                          158  *                                       THAT MALF ALARM BITS WILL CLEAR   73201590
02B     7B 0098           159           C     UH+XR2+PRIV              SET CC, START EXTENDED READ       73201600
02C     20 3A07           160           O     PSWL,PSWL,ARL            'OR' IN OTHER PSW BITS            73201610
02D     00 B014           161           L     LOC,MDR                  LOAD LOC WITH NEW VALUE           73201620
02E     F0 0017           162           B     TWAIT                    GO TEST WAIT BIT (P.3)            73201630

                          164  *          INTERRUPTABLE WAIT LOOP                                73201650

02F     70 0004           166  WAIT     C     SWA                      SET WAIT INDICATOR          73201670
030     EA 0074           167           BT    SNGL.CONSER              (P.8)                       73201680
031     00 8010           168  WAIT1    L     NULL,NULL                NOP                         73201690
032     E4 2034           169           BT    ATN,WAIT2                TO WAIT2 IF ATN             73201700
033     F9 3031           170           BF    MALF+PPF+CATN,WAIT1 LEAVE WAIT LOOP IF MALF.PPF OR CATN 73201710
034     70 0000           171  WAIT2    C     CWA                      CLEAR WAIT INDICATOR        73201720
035     EA 0087           172           BT    SNGL,CLRWT               DO ONE INSTR IF SNGL (P.8)  73201730
036     F0 0045           173           B     HELP                     DETERMINE CAUSE OF INT. (P.5)     73201740
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INTERRUPT SUPPORT ROUTINES. 73200

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037  E8 10B6   175 HELP1   BT   PPF,PWRDWN     PRIMARY POWER FAIL (P.11)          73201760
038  E9 0074   176          BT   CATN,CONSER    CONSOLE ATTENTION (P.9)            73201770
039  89 0017   177          LI   MAR,'90'       (MAR)=ADRS OF MAC INT. NEW PSW     73201780
03A  E4 1007   178          BT   MAC,COMIN2     MEMORY ACCESS CONTROLLER (P.3)     73201790
03B  E8 2019   179          BT   MALF,MMFINT    MACHINE MALFUNCTION (P.8)          73201800
03C  F0 0074   180          B    CONSER         CONSOLE SINGLE STEP (P.9)          73201810
               181 *                                                              73201820
03D  E0 102F   182 TWAIT1   BT   WAIT,WAIT      TO WAIT IF PSW 16=1 (P.4)          73201830
03E  70 0000   183          C    CWA            RESET WAIT INDICATOR               73201840
03F  F0 02CC   184          B    ABR            LOC TO MAR & FETCH NEXT (P.30)     73201850
               185 *                                                              73201860

               187 *          ABORT CURRENT INSTRUCTION                           73201880
               188 * LOC IS POINTING TO NEXT INSTRUCTION TO BE PERFORMED          73201890

040                 190          ORG  '040'                                        73201910
040  50 A314   191 ABORT    S    LOC,LOC,TWO    DECREMENT LOC BY TWO               73201920
041  E4 4045   192          BT   RR,HELP        TO HELP IF RR                      73201930
042  50 A314   193          S    LOC,LOC,TWO    DECREMENT AGAIN BY TWO             73201940
043  EC 1045   194          BT   SHORT,HELP     TO HELP IF RI1,RX1 OR RX2          73201950
044  50 A314   195          S    LOC,LOC,TWO    DECREMENT AGAIN IF RX2 OR RX3      73201960

               197 * COMMON INTERRUPT SUPPORT ENTRY POINT                         73201980
               198 *                                                              73201990
               199 * DETERMINE CAUSE OF INTERRUPT                                 73202000
               200 *                                                              73202010
045  F6 0037   201 HELP     BF   ATNX,HELP1    TO HELP1 IF NO I/O INTERRUPT       73202020
               202 *                           OR IF PPF, MALF, OR MAC INT.       73202030
               203 *                                                              73202040
               204 * I/O ATTENTION AND NO HIGHER PRIORITY INTERRUPTS               73202050
               205 *                                                              73202060
               206 *                                                              73202070
046  00 A881   207 AUTOIO   L    MR1,IO,ACK     ACKNOWLEDGE INTERRUPT              73202080
               208 *                           DEVICE NUMBER TO MR1               73202090
               209 *                                                              73202100
047  00 0A0B   210 AUTOIO1  L    AR,MR1,SL      2X DEVICE NUMBER                   73202110
048  CD 0617   211          AI   MAR,'D0',AR    PLUS X'000D0'                      73202120
049  0A 3802   212          L    MR2,PSWL,MRD   FETCH SERVICE POINTER TABLE        73202130
               213 *                           ENTRY. SAVE PSW(16:31) IN MR2      73202140
04A  82 8607   214          LI   PSWL,'28',CS   SET PSWL = '2800'                 73202150
04B  00 0835   215          L    IO,MR1,ADRS    ADDRESS THE DEVICE                 73202160
04C  70 0081   216          C    CYD            REGISTER SET 0 IS SELECTED         73202170
04D  00 7018   217          L    YDH,PSWH                                          73202180
04E  00 101A   218          L    YDLP1,MR2      REG. 0 = PSW                       73202190
04F  00 8818   219          L    YDH,LOCH                                          73202200
050  00 A01A   220          L    YDLP1,LOC      REG. 1 = LOC                       73202210
051  00 800E   221          L    PSWH,NULL                                         73202220
052  00 8443   222          L    MR3,MDR,SR+CO  TEST LSB OF TABLE ENTRY            73202230
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INTERRUPT SUPPORT ROUTINES. 73200

```
053  00 1A14   223          L   LOC,MR3,SL     (LOC)=(MAR)=SERVICE POINTER TABLE   73202240
               224  *                          ENTRY - FORCED EVEN                 73202250
054  00 8018   225          L   YDH,NULL                                            73202260
055  00 061A   226          L   YDLP1,MR1      REG, 2 = DEVICE NUMBER              73202270
056  E2 0122   227          BT  C,CHANEL       CHANNEL I/O IF ODD (P.15)           73202280
057  05 A8D9   228          L   YDL,IO,STAT+IRJH REG, 3 = DEVICE STATUS            73202290
058  00 8018   229          L   YDH,NULL                                           73202300

               231  *      FLOATING POINT ARITHMETIC FAULT      *                  73202320

059  80 8000   233  FFAULT  LI  MR0,8          (MR0)=8 TO SET C FLAG IN NEW PSW    73202340

               235  *        FIXED POINT ARITHMETIC FAULT       *                  73202360

05A  00 800F   237  IFAULT  L   FLR,NULL       CLEAR FLAG REGISTER                 73202380
05B  81 0609   238          LI  ARL,'10',CS    (ARL)='1000'                        73202390
05C  10 3A30   239          N   NULL,PSWL,ARL,F TEST PSW BIT 19                     73202400
05D  F0 82CC   240          BF  G,NBR          IGNORE IF NOT ENABLED (P.30)        73202410
05E  64 8017   241          LI  MAR,'48'       (MAR)=ADRS OF ARITHMETIC            73202420
05F  70 0020   242          C   SUT            FAULT NEW PSW                       73202430
060  F0 0006   243          B   COMINT         TO COMMON INTERRUPT HANDLER (P.3)   73202440
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                                245  *                ADDRESS                 *                73202460
                                246  *                                                        73202470
                                247  ADRS    L       MDR,MDR,SR      LS 16 SWITCH REGISTER BITS      73202480
061   00 B416                   248          L       ARL,MDR,SL      FORCED EVEN                     73202490
062   00 8209                   249          L       ARH,YSI         MS 4 ADRS BITS FROM STATUS      73202500
063   00 600A                   250          A       LOC,NULL,AR     LOAD LOC                        73202510
064   40 8614

                                252  *           DISPLAY LOCATION COUNTER     *                73202530
                                253  *                                                        73202540
                                254  LOCDIS  LI      IO,1,ADRS       ADDRESS THE CONSOLE             73202550
065   80 1035                   255          L       MR0,LOCH        (MR0)=D2,D1=LOC(0:15)           73202560
066   00 8800                   256          L       MR1,LOC         (MR1)=D4,D3=LOC(16:31)          73202570
067   00 A001                   257          LI      MR2,'45'        (MR2)=D5=FUNCTION 5             73202580
068   84 5002

                                259  *           OUTPUT DATA BYTES TO THE CONSOLE     *           73202600
                                260  *                                                        73202610
                                261  OUTDIS  L       IO,MR1,DA       OUTPUT D1                       73202620
069   C0 0855                   262          L       IO,MR1,DA+CS    OUTPUT D2                       73202630
06A   00 0E55                   263          L       IO,MR0,DA       OUTPUT D3                       73202640
06B   C0 0055                   264          L       IO,MR0,DA+CS    OUTPUT D4                       73202650
06C   00 0655                   265          L       IO,MR2,DA       OUTPUT D5                       73202660
06D   00 1055                   266  *                                                        73202670
                                267  * FALL THROUGH TO IDLE                                  73202680

                                269  *           UN-INTERRUPTABLE IDLE LOOP   *                73202700
                                270  *                                                        73202710
06E   70 0004                   271  IDLE    C       SWA             SET WAIT INDICATOR              73202720
06F   F9 106E                   272  IDLE1   BF      PPF+CATN,IDLE   WAIT FOR PPF OR CATN          73202730
070   70 0000                   273          C       CWA             CLEAR WAIT INDICATOR            73202740
071   E8 10B6                   274          BT      PPF,PWRDWN      POWER FAIL (P.11)               73202750
072   80 1035                   275          LI      IO,1,ADRS       ADDRESS THE CONSOLE             73202760
073   EA 0067                   276          BT      SNGL,CLRWT      LEAVE IF SINGLE STEP (P.8)      73202770
                                277  *                               ADDRESSING THE DISPLAY          73202780
                                278  *                               MAKES CATN GO INACTIVE          73202790
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074  80 1035   280  CONSER  LI   IO,1,ADRS        ADDRESS THE CONSOLE                    73202810
075  00 A8C0   281          L    MR0,IO,STAT      (MR0)=CONSOLE STATUS                   73202820
076  00 0413   282          L    SRH,MR0,SR                                              73202830
077  70 0C00   283          C    SR2                                                     73202840
078  00 9C01   284          L    MR1,SRH,SR       MR1(12:15)=STATUS(0:3)                 73202850
079  88 0075   285          LI   IO,'80',OC       OUTPUT COMMAND NORMAL MODE             73202860
07A  82 9017   286          LI   MAR,'29'                                                73202870
07B  0A 080F   287          L    FLR,MR1,MRD      FETCH LAST STATUS BYTE                 73202880
07C  00 B004   288          L    MR4,MDR          SET ASIDE IN MR4                       73202890
07D  CC 0E16   289          L    MDR,MR1,MWD+CS   SAVE SHIFTED STATUS AT X'00029'        73202900
07E  80 1035   290          LI   IO,1,ADRS        RE-ADDRESS TO CLEAR BYTE COUNTERS      73202910
07F  00 028C   291          L    YSI,MR0,SL+CI    YSI=STATUS BITS 5,6,7,0                73202920
080  E1 0093   292          BT   V,DISPLY         FUNCTION OR REGISTER DISPLAY (P.9)     73202930
081  EA 006E   293          BT   SNGL,IDLE        GO TO IDLE IF SINGLE STEP (P.7)        73202940
082  00 A017   294          L    MAR,LOC                                                 73202950
083  E0 408A   295          BT   L,ADRMW          ADDRESS OR MEMORY WRITE                73202960
084  08 8010   296          L    NULL,NULL,MR     RUN MODE OR MEMORY READ                73202970
085  00 B001   297          L    MR1,MDR          MR1=MEMORY DATA                        73202980
086  E0 808E   298          BT   G,DISMEM         SHOW ADDRESS AND DATA                  73202990

                300  *                RUN MODE                *                          73203010
                301  *                                                                    73203020
087  00 3A06   302  CLRWT   L    MR6,PSWL,SL                                             73203030
088  00 3407   303          L    PSWL,MR6,SR      CLEAR WAIT BIT (PSW14)                 73203040
089  F0 02CC   304          B    MBR              FETCH NEXT USER INSTRUCTION (P.30)     73203050

                306  *          ADDRESS OR MEMORY WRITE       *                          73203070
                307  *                                                                    73203080
08A  00 A8B6   308  ADRMW   L    MDR,IO,DR        INPUT LS SWITCH REGISTER BYTE          73203090
08B  00 AEB6   309          L    MDR,IO,DR+CS     INPUT MS SWITCH REGISTER BYTE          73203100
08C  E0 8061   310          BT   G,ADRS           ADDRESS (P.7)                          73203110

                312  *                MEMORY WRITE            *                          73203130
                313  *                                                                    73203140
08D  0E B001   314          L    MR1,MDR,MW       (MR1)=D4,D3=MEMORY DATA                73203150
08E  40 A314   315  DISMEM  A    LOC,LOC,TWO      INCREMENT LOC                          73203160
08F  00 A000   316          L    MR0,LOC          (MR0)=D2,D1=MEMORY ADDRESS             73203170
090  88 0009   317          LI   ARL,'80'         (MR2)=D5=MEMORY ADRS/MEMORY DATA       73203180
091  20 8A02   318          O    MR2,LOCH,ARL     AND MS 4 BITS OF THE ADDRESS           73203190
092  F0 0069   319          B    OUTDIS           SHOW D5,D4,D3,D2,& D1 (P.7)            73203200
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093  00 000F  321  DISPLY  L    FLR,MR0                                        73203220
094  F2 009E  322           BF   C,FN          FUNCTION IF STATUS BIT 4 RESET  73203230

                  324  *      GENERAL REGISTER OR FLOATING REGISTER      *    73203250
                  325  *                                                      73203260
095  00 080F      326  REGDIS L    FLR,MR1                                    73203270
096  F0 4099      327           BF   C,GENREG      DISPLAY GENERAL REGISTER    73203280
097  E5 050D      328           BT   HW,FLTREGC    IF HARDWARE FLOATING POINT (P,58)  73203290
098  F0 04F5      329           B    FLTREG        ELSE (P,49)                 73203300
                  330  *                                                      73203310
099  00 E000      331  GENREG  L    MR0,YSH        (MR0)=D2,D1=GEN,REG. (0:15) 73203320
09A  00 E801      332           L    MR1,YSL        (MR1)=D4,D3=GEN,REG.(16:31) 73203330
09B  82 0009      333           LI   ARL,'20'       (MR2)=D5=GEN,REG. N         73203340
09C  20 6202      334           O    MR2,YSI,ARL                                73203350
09D  F0 0069      335           B    OUTDIS        (P,7)                       73203360

                  337  *                    FUNCTION                      *    73203380
                  338  *                                                      73203390
09E  00 600F      339  FN       L    FLR,YSI                                    73203400
09F  E2 006E      340           BT   C,IDLE        IDLE IF UNDEFINED FUNCTION (P,7)  73203410
0A0  F1 00A6      341           BF   V,FN0123      FUNCTION 0,1,2 OR 3 (P,10)  73203420

                  343  *                  FUNCTION 4 OR 5                 *    73203440
                  344  *                                                      73203450
0A1  E0 4065      345           BT   L,LOCDIS      FN 5 = LOCATION COUNTER (P,7)  73203460

                  347  *              DISPLAY PROGRAM STATUS WORD          *    73203480
                  348  *                                                      73203490
0A2  00 7000      349  PSWDIS  L    MR0,PSWH       (MR0)=D2,D1=PSW(0:15)       73203500
0A3  00 3801      350           L    MR1,PSWL       (MR1)=D4,D3=PSW(16:31)      73203510
0A4  84 4002      351           LI   MR2,'44'       (MR2)=D5=FUNCTION 4         73203520
0A5  F0 0069      352           B    OUTDIS        (P,7)                       73203530
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0A6     EA 0065     354  FN0123  BT   SNGL,LOCDIS      LEAVE IF SINGLE STEP          73203550
0A7     F0 80AB     355          BF   G,FN01           FUNCTION 0 OR 1               73203560
0A8     82 8017     356          LI   MAR,'28'                                       73203570
0A9     0C 6616     357          L    MDR,YSI,CS+MWD   SAVE FUNCTION # IF 2 OR 3     73203580
0AA     F0 0065     358          B    LOCDIS           THEN EXIT                     73203590
                    359  *                                                          73203600
                    360  *            FUNCTION 0 OR 1              *                73203610
                    361  *                                                          73203620
0AB     F0 4061     362  FN01    BF   L,FN0            FUNCTION 0                    73203630

                    364  *            FUNCTION 1                   *                73203650
                    365  *                                                          73203660
0AC     00 A8A0     366          L    MR0,IO,DR        INPUT LS SWITCH REGISTER BYTE 73203670
0AD     00 AEA9     367          L    ARL,IO,DR+CS     INPUT MS SWITCH REGISTER BYTE 73203680
0AE     20 0207     368          O    PSWL,MR0,ARL     COMBINE AND LOAD PSW          73203690
0AF     70 0088     369          C    JH               COPY FLR TO CONDITION CODE    73203700
0B0     F0 00A2     370          B    PSWDIS           SHOW NEW PSW (P.9)            73203710

                    372  *            FUNCTION 0                   *                73203730
                    373  *                                                          73203740
0B1     00 3A06     374  FN0     L    MR6,PSWL,SL                                   73203750
0B2     00 3250     375          L    NULL,MR6,SL+C0   TEST PSW BIT 17               73203760
0B3     F2 0087     376          BF   C,CLRWT          (P.8) RUN MODE IF INTERRUPTS  73203770
                    377  *                            ARE NOT ENABLED.  ELSE.       73203780
0B4     80 1001     378          LI   MR1,1            SIMULATE INTERRUPT FROM DEVICE 73203790
0B5     F0 0047     379          B    AUTOI01          NUMBER '001' (P.5)            73203800
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POWER DOWN SEQUENCE 73203

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0B6   88 4017   381  PWRDWN  LI   MAR,'84'        ADDRESS PSW SAVE POINTER                    73203820
0B7   0D 8010   382          L    NULL,NULL,MRD2  FETCH PSW SAVE POINTER                       73203830
0B8   0A B017   383          L    MAR,MDR,MRD     (MAR)=ADDRESS OF CURRENT PSW                73203840
                384  *                           SAVE AREA, FETCH ADDRESS OF                 73203850
0B9   00 B000   385          L    MR0,MDR         REGISTER SAVE AREA, SAVE IN MR0             73203860
0BA   00 7016   386          L    MDR,PSWH                                                    73203870
0BB   7F 0090   387          C    MW2+PRIV        SAVE HIGH PSW                               73203880
0BC   00 3816   388          L    MDR,PSWL                                                    73203890
0BD   7F 0090   389          C    MW2+PRIV        SAVE LOW PSW                                73203900
0BE   00 8007   390          L    PSWL,NULL       CLEAR LOW PSW (DISABLES MAC)                73203910
0BF   0F 8816   391          L    MDR,LOCH,MW2    SAVE HIGH LOC                               73203920
0C0   0F A016   392          L    MDR,LOC,MW2     SAVE LOW LOC                                73203930
0C1   00 0017   393          L    MAR,MR0         (MAR)=REGISTER SAVE AREA ADRS.              73203940
0C2   70 0010   394          C    CUT             CLEAR UTILITY FLOP                          73203950
                395  *                           REGISTER SET 0 IS SELECTED                  73203960
0C3   70 0081   396  SAVREG  C    CYD             SELECT GENERAL REGISTER 0                   73203970
0C4   80 F008   397          LI   CTR,15                                                      73203980
0C5   0F C016   398  SLOOP1  L    MDR,YDH,MW2     STORE MS 16 BITS                            73203990
0C6   0F D016   399          L    MDR,YDLP1,MW2   STORE LS 16 BITS AND INCREMENT              73204000
0C7   FC 80C5   400          BF   CNTR,SLOOP1     YD FIELD BY ONE,  LOOP UNTIL               73204010
                401  *                           16 REGISTERS HAVE BEEN SAVED.               73204020
0C8   70 0030   402          C    TUT             TOGGLE UTILITY                              73204030
0C9   8F 0007   403          LI   PSWL,'F0'       SELECT REGISTER SET 'F'                     73204040
0CA   EC 20C3   404          BT   UT,SAVREG       LOOP BACK TO SAVE REG.SET 'F'               73204050
0CB   E5 05EA   405          BT   HW,SAVEFLPT     BRANCH IF HARDWARE FLPT (P.59)              73204060
0CC   70 0002   406          C    POW             SYSTEM INITIALIZE                           73204070
                407  *                           ON POWER RESTORE, MICROCODE                 73204080
                408  *                           EXECUTION BEGINS AT '100'                   73204090
                409  *                                                                       73204100
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LOADER STORAGE UNIT SUPPORT 73204

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0CD  00 800E  411  LSU    L  PSWH,NULL              CLEAR PSW(0:15)          73204120
0CE  00 AEA9  412         L  ARL,IO,DR+CS                                    73204130
0CF  00 A8A0  413         L  MR0,IO,DR                                       73204140
0D0  20 0207  414         O  PSWL,MR0,ARL           LOAD PSW <16:27>         73204150
0D1  70 0088  415         C  JH                     LOAD PSW (28:31)         73204160
0D2  00 AEAA  416         L  ARH,IO,DR+CS                                    73204170
0D3  00 A8A0  417         L  MR0,IO,DR                                       73204180
0D4  20 0714  418         O  LOC,MR0,ARH            LOAD LOC (0:31)          73204190
0D5  00 AEAA  419         L  ARH,IO,DR+CS                                    73204200
0D6  00 A8A0  420         L  MR0,IO,DR                                       73204210
0D7  20 0717  421         O  MAR,MR0,ARH            (MAR)=16 BIT START ADDRESS 73204220
0D8  00 AEA9  422         L  ARL,IO,DR+CS                                    73204230
0D9  00 A8A0  423         L  MR0,IO,DR                                       73204240
0DA  20 0201  424         O  MR1,MR0,ARL            (MR1)=16 BIT END ADDRESS 73204250
0DB  00 B80B  425         L  AR,MAR                                          73204260
0DC  50 0A41  426         S  MR1,MR1,ARL,CO         (MR1)=END ADRS-START ADDRESS 73204270
0DD  E2 006E  427         BT C,IDLE                 IDLE IF START > END (P,7) 73204280
              428  *                                                         73204290
0DE  08 8010  429  LSLOOP L  NULL,NULL,MR                                   73204300
0DF  0E AE86  430         L  MDR,IO,DR+CS+MW        INPUT & STORE A BYTE     73204310
0E0  50 0941  431         S  MR1,MR1,ONE,CO         DECREMENT BYTE COUNT     73204320
0E1  E2 003D  432         BT C,TWAIT1               BRANCH IF DONE (P,5)     73204330
0E2  40 B917  433         A  MAR,MAR,ONE            INCREMENT BYTE ADDRESS   73204340
0E3  F0 00DE  434         B  LSLOOP                 AND LOOP                 73204350
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                                436  * SYSTEM QUEUE INTERRUPT IS ENABLED, TEST THE QUEUE                    73204370
                                437  * MR3 CONTAINS BIT 0:15 OF THE PSW                                     73204380
                                438  *                                                                      73204390
0E4   88 0017                   439  QUFINT   LI    MAR,'80'     (MAR)=ADDRESS OF POINTER TO THE          73204400
0E5   0D 800E                   440           L     PSWH,NULL,MRD2 SYSTEM QUEUE.  CLEAR HIGH PSW          73204410
                                441  *                            AND FETCH QUEUE POINTER                  73204420
                                                                                                            73204430
0E6   80 D00C                   442           LI    YSI,13                                                   73204440
0E7   7B 0090                   443           C     YR2+PRIV     START EXTENDED READ, NO MAC                 73204450
0E8   00 3601                   444           L     MR1,PSWL     SAVE LOW PSW IN MR1                         73204460
0E9   40 B317                   445           A     MAR,MDR,TWO  (MAR)=QUEUE ADDRESS + 2                     73204470
0EA   0A B008                   446           L     AR,MDR,MRD   (AR)=ADDRESS OF QUEUE. FETCH                73204480
                                                                 NUMBER USED TALLY                          73204490
                                447  *                                                                      73204500
0EB   00 B030                   448           L     NULL,MDR,F   CHECK THE SYSTEM QUEUE                     73204510
0EC   F0 83FA                   449           BF    G,TWAIT2     TEST WAIT IF QUEUE EMPTY (P.40)            73204520
                                450  *                                                                      73204530
                                451  * SYSTEM QUEUE IS NOT EMPTY                                           73204540
                                452  *                                                                      73204550
0ED   00 180E                   453           L     PSWH,MR3     LOAD PSWH FROM MR3                         73204560
0EE   88 8017                   454           LI    MAR,'88'     (MAR)=ADDRESS OF QUEUE SERVICE             73204570
0EF   00 8007                   455           L     PSWL,NULL    INTERRUPT NEW PSW.  CLEAR PSWL,            73204580
                                456  *                            SELECTING REGISTER SET 1                 73204590
0F0   40 821D                   457           A     YSL,NULL,ARL                                             73204600
0F1   40 871C                   458           A     YSH,NULL,ARH REG. 13 = ADDRESS OF SYSTEM QUEUE           73204610
0F2   70 0010                   459           C     CUT          CLEAR UTILITY                               73204620
0F3   F0 000A                   460           B     COMIN1       TO COMMON INTERRUPT ROUTINE (P.3)           73204630
                                461  *                                                                      73204640
0F4   5E 8116                   462  TS1      S     MDR,NULL,ONE,MW WRITE A HALFWORD OF ALL ONES            73204650
0F5   F0 044B                   463           B     FETCHJ       EXIT (P.43)                                 73204660
                                464  *                                                                      73204670
0F6   07 8010                   465  LRERR    L     NULL,NULL,IRJ LIMIT VIOLATION                           73204680
0F7   80 800F                   466           LI    FLR,8                                                    73204690
0F8   07 8010                   467  SETG     L     NULL,NULL,IRJ WRITE PROTECT                             73204700
0F9   80 200F                   468           LI    FLR,2                                                    73204710
0FA   07 8010                   469  SETL     L     NULL,NULL,IRJ EXECUTE PROTECT                           73204720
0FB   80 100F                   470           LI    FLR,1                                                    73204730
                                471  *                                                                      73204740
0FC   00 B214                   472  NTRANS   L     LOC,MDR,SL   (LOC)=(MAR)=SUBROUTINE ADRS              73204750
0FD   F0 02D0                   473           B     FETCH        GO TO SUBROUTINE (P.30)                     73204760
0FE   00 8010                   474           L     NULL,NULL    FILLER (NOT USED)
0FF   00 8010                   475           L     NULL,NULL    FILLER (NOT USED)
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100                     477         ORG   '100'                                          73204780
100      88 4077        478 PWRUP   LI    MAR,'84',C0+F     (MAR)=ADRS OF PSW SAVE POINTER 73204790
                        479 *                                 CLEAR C AND V FLAGS        73204800
101      80 5035        480         LI    IO,'05',ADRS      ADDRESS THE LOADER STORAGE UNIT 73204810
102      F1 00CD        481         BF    V,LSU             LSU PRESENT IF NO FALSE SYNC (P,12) 73204820
                        482 *                                                              73204830
                        483 * LSU NOT PRESENT, DO NORMAL POWER UP                         73204840
                        484 *                                                              73204850
103      0D 8007        485         L     PSWL,NULL,MRD2    CLEAR LOW PSW, FETCH PSW     73204860
104      09 8000        486         L     MR0,MDR,MR2       SAVE POINTER.  SAVE IN MR0.  73204870
105      00 8017        487         L     MAR,MDR           (MAR)=REGISTER SAVE POINTER  73204880
106      7D 0081        488         C     MRD2+CYD          FETCH GENERAL REGISTER 0     73204890
107      80 F008        489 LLOOP2  LI    CTR,15            REGISTER SET 0 IS SELECTED FIRST 73204900
                        490 *                                                              73204910
                        491 * RESTORE REGISTER SET 0                                      73204920
                        492 *                                                              73204930
108      09 8018        493 LLOOP1  L     YDH,MDR,MR2       LOAD MS 16 BITS              73204940
109      09 801A        494         L     YDLP1,MDR,MR2     LOAD LS 16 BITS, INCREMENT   73204950
10A      FC 8108        495         BF    CNTR,LLOOP1       YD FIELD, LOOP FOR 16 REGISTERS 73204960
                        496 *                                                              73204970
10B      70 0030        497         C     TUT               TOGGLE UTILITY FLIP-FLOP     73204980
10C      8F 0007        498         LI    PSWL,'F0'         SELECT REGISTER SET 'F'      73204990
10D      EC 2107        499         BT    UT,LLOOP2         RESTORE REGISTER SET 'F'     73205000
                        500 *                                                              73205010
                        501 *                                                              73205020
10E      E5 05F6        502         BT    HW,RSTRFLPT       BRANCH IF HARDWARE FLOATING POINT 73205030
                        503 *                                                              73205040
10F      00 0017        504 PWRUP1  L     MAR,MR0           ADDRESS OF PSW SAVE AREA     73205050
110      09 8010        505         L     NULL,NULL,MR2                                  73205060
111      09 800E        506         L     PSWH,MDR,MR2      LOAD PSW(0:15)               73205070
112      00 8007        507         L     PSWL,MDR          LOAD PSW(16:27)              73205080
113      7D 0086        508         C     JH+MRD2           LOAD PSW(28:31),FETCH HIGH LOC 73205090
114      7B 0090        509         C     XR2+PRIV          START EXTENDED READ FOR LOW LOC 73205100
115      00 8014        510         L     LOC,MDR           LOAD ENTIRE LOC              73205105
116      82 8017        511         LI    MAR,'28'                                       73205110
117      0A 3A13        512         L     SRH,PSWL,SL+MRD   FETCH SAVED                  73205120
118      00 800F        513         L     FLR,MDR           CONSOLE STATUS BYTE.         73205130
119      0C 8616        514         L     MDR,NULL,CS+MWD   CLEAR HIGH BYTE OF '000028' 73205140
11A      E1 C065        515         BT    V+6+L,LOCDIS      (P,7) BRANCH IF CONSOLE STATUS 73205150
                        516 *                               BEFORE POWER DOWN WAS NOT RUN 73205160
                        517 *                               GO DISPLAY LOC THEN ENTER "IDLE" 73205170
11B      FC 4065        518         BF    ARST,LOCDIS       IF CONSOLE WAS IN RUN MODE, BUT 73205180
                        519 *                               THE AUTOMATIC RESTART OPTION IS 73205190
                        520 *                               NOT EQUIPPED, ALSO DISPLAY LOC 73205200
                        521 *                               AND ENTER "IDLE".  IF ARST OPTION 73205210
                        522 *                               IS EQUIPPED AND PSW BIT 16 IS 73205220
11C      70 1440        523         C     SL2+C0            SET(MACHINE MALFUNCTION INT. 73205230
11D      E2 0019        524         BT    C+MMFINT          ENABLE) TAKE THE INTERRUPT (P,4) 73205240
11E      F0 003D        525         B     TWAIT1            ELSE, WAIT OR RUN (P,4)      73205250
11F      00 8010        526         L     NULL,NULL         FILLER (NOT USED)            73205260
120      00 8010        527         L     NULL,NULL         FILLER (NOT USED)            73205270
121      00 8010        528         L     NULL,NULL         FILLER (NOT USED)            73205280
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                                                                                                    73205300
122  79 0010   530 CHANEL  C   CUT+MR2          FETCH CCW                                          73205310
123  00 A006   531          L   MR6,LOC          (MR6)=ADRS OF CCB                                  73205320
124  00 A8D9   532          L   YDL,IO,STAT      R2(16:31)=DEVICE ADDRESS                           73205330
               533  *                            R3(16:31)=DEVICE STATUS                            73205340
125  00 0009   534          L   ARL,YDLP1        (ARL)=DEVICE STATUS                                73205350
               535  *                            YD FIELD POINTS TO GR 4                            73205360
126  00 B601   536          L   MR1,MDR,CS       STATUS MASK DOWN                                   73205370
127  00 0A50   537          L   NULL,MR1,SL+CO    TEST "E" BIT OF CCW                                73205380
128  F2 017D   538          BF  C,EXSUB1         EXIT TO SUBROUTINE IF E=0 (P.18)                   73205390
129  10 0A30   539          N   NULL,MR1,ARL,F    TEST STATUS                                        73205400
12A  E0 818B   540          BT  G,EXSUB2         EXIT TO SUBROUTINE IF BAD (P.18)                   73205410
12B  00 B00F   541          L   FLR,MDR          FLR=CCW BITS 12:15                                 73205420
12C  F0 4151   542          BF  L,NFAST          BRANCH IF NORMAL MODE (P.17)
                                                                                                    73205440
               544  *                F A S T   M O D E                                             73205450
               545  *                                                                              73205460
12D  09 B803   546  FRONT  L   MR3,MAR,MR2      (MAR)=ADRS OF BYTE COUNT                           73205470
               547  *                            (MR3)=ADRS OF BYTE COUNT                           73205480
12E  00 800F   548          L   FLR,NULL                                                          73205490
12F  40 850A   549          A   ARH,NULL,SIGN     (ARH,ARL)=BUFFER BYTE COUNT                    73205500
130  09 B029   550          L   ARL,MDR,F+MR2     START FETCH FOR END ADDRESS                    73205510
131  E0 8140   551          BT  G,EXAUTO         TO EXAUTO IF COUNT POSITIVE                    73205520
132  40 8204   552          A   MR4,NULL,ARL      (MR4)=BUFFER BYTE COUNT                        73205530
133  0B 0E01   553          L   MR1,MR1,CS+XR2    (MR1)=CCW, EXTENDED READ                       73205540
134  40 B614   554          A   LOC,MDR,AR       (MAR)=(LOC)=BUFFER END ADDRESS                 73205550
               555  *                            PLUS BUFFER BYTE COUNT                         73205560
135  08 0C0F   556          L   FLR,MR1,SR+MR     (FLR)=CCW BITS 11:14                           73205570
136  EC 2156   557          BT  UT,NFAST1        BACK TO NORMAL MODE (P.17)                     73205580
137  EE 014B   558          BT  HWIO,HALFIO      BRANCH IF HW LINE ACTIVE (P.16)                73205590
138  E0 813B   559          BT  G,FWRITE         WRITE A BYTE IF R/W=1                          73205600
               560  *                            READ A BYTE IF R/W=0                           73205610
139  0E AEB6   561  FREAD  L   MDR,IO,DR+CS+MW   INPUT BYTE AND STORE IT                        73205620
13A  F0 013C   562          B   WRITE2                                                          73205630
               563  *                                                                          73205640
13B  00 B655   564  FWRITE L   IO,MDR,DA+CS      OUTPUT BYTE                                    73205650
13C  C0 1216   565  WRITE2 AI  MDR,'1',ARL       (MDR)=INCREMENTED BYTE COUNT                   73205660
               566  *                                                                          73205670
13D  40 3317   567  ADWTBH A   MAR,MR6,TWO       (MAR)=ADRS OF BUFFER0                          73205680
13E  5E 8430   568          S   NULL,NULL,MDR,F+MW BYTE COUNT, STORE UPDATED COUNT             73205690
               569  *                            SET L FLAG IF COUNT POSITIVE                   73205700
13F  E0 417C   570          BT  L,EXSUB3         EXIT IF COUNT POSITIVE NOW (P.18)

                                                                                                    73205720
140  80 100C   572  EXAUTO LI  YSI,'1'          POINT TO REGISTER 1                            73205730
141  00 E814   573          L   LOC,YSL          RESTORE LOC                                    73205740
142  50 610C   574          S   YSI,YSI,ONE                                                     73205750
143  00 E00E   575          L   PSWH,YSH         LOAD PSW                                       73205760
144  00 E807   576          L   PSWL,YSL                                                       73205770
145  70 0088   577          C   JH               PROPOGATE FLR TO CC                            73205780
146  E0 102F   578          BT  WAIT,WAIT        TO WAIT IF PSW 16 SET (P.4)                    73205790
147  E8 2149   579          BT  MALF,*+2         SKIP IF MACHINE MALFUNCTION
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148     04 8010     580           L     NULL,NULL,IR      FETCH INSTRUCTION                    73205800
149     70 0020     581           C     SUT                                                    73205810
14A     F0 001A     582           B     MMF1              DO MALFINTERRUPT (P.4)               73205820

14B     E0 814F     584  HALFIO   BT    G,HWRITE          OUTPUT A HALFWORD IF R/W=1           73205840
                    585  *                               READ A HALFWORD IF R/W=0             73205850
14C     0E A8B6     586           L     MDR,IO,DR+MW      INPUT & STORE                        73205860
14D     C0 2216     587  HRDWT    AI    MDR,'2',ARL       (MDR)=INCREMENTED BYTE COUNT         73205870
14E     F0 013D     588           B     RDWTBH            (P.15)                               73205880
                    589  *                                                                    73205890
14F     00 B055     590  HWRITE   L     IO,MDR,DA         OUTPUT A HAFLWORD                    73205900
150     F0 014D     591           B     HRDWT                                                  73205910
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                        593  *              N O R M A L   M O D E                                  73205930
                        594  *                                                                     73205940
151  70 0020            595  NFAST   C      SUT          UT=1 IF NORMAL MODE                       73205950
152  F2 012D            596          BF     C,FBCNT      GO SET UP FOR BUFFER 8 (P.15)             73205960
153  90 8403            597          NI     AR,'8',MDR                                             73205970
154  40 BE17            598          A      MAR,MAR,AR   (MAR)=ADRS OF BUFFER 1 COUNT              73205980
155  F0 012D            599          B      FBCNT        GO SET UP FOR BUFFER 1 (P.15)             73205990
                        600  *                                                                     73206000
                        601  * CONTROL RETURNS HERE      (FLR)=CCW BITS 11,12,13,14                73206010
                        602  *                                                                     73206020
156  E0 8170            603  NFAST1  BT     G,NFWRITE    WRITE IF R/W=1                            73206030
                        604  *                           READ IF R/W=0                             73206040
157  00 A8A2            605          L      MR2,IO,DR    (MR2)=INPUT DATA BYTE                     73206050
158  00 1013            606          L      SRH,MR2      (SRH)=INPUT DATA BYTE                     73206060
159  F0 4165            607          BF     L,RECHECK    NO TRANSLATE BRANCH                       73206070
                        608  *                                                                     73206080
                        609  *                                                                     73206090
15A  81 000B            610  TRANSL  LI     AR,'10'                                                73206100
15B  40 3617            611          A      MAR,MR6,AR   (MAR)=ADRS OF XLATION TABLE               73206110
15C  09 1208            612          L      AR,MR2,SL+MR2 2X CHARACTER, FETCH TABLE ADRS           73206120
15D  78 0000            613          C      XR2          START EXTENDED READ (20 BIT ADRS)         73206130
15E  40 B617            614          A      MAR,MDR,AR   2X CHAR, PLUS TABLE START                 73206140
15F  08 0C0F            615          L      FLR,MR1,SR+MR (FLR)=CCW BITS 11:14                     73206150
                        616  *                           FETCH TABLE ENTRY                         73206160
160  00 B250            617          L      NULL,MDR,SL+C0 TEST MSB OF ENTRY                       73206170
161  F2 0186            618          BF     C,EXTRAN     EXIT TO SUBROUTINE IF RESET (P.18)        73206180
162  9F F402            619          NI     MR2,'FF',MDR (MR2)=TRANSLATED CHARACTER                73206190
163  F0 8165            620          BF     G,RECHECK    SKIP IF R/W=0                             73206200
164  00 1013            621  RTRANW  L      SRH,MR2      SRH=TRANSLATED CHARACTER IF READ          73206210
                        622  *                           UNTRANSLATED CHARACTER IF WRITE           73206220
165  60 800B            623  RECHECK LI     AR,8         CCW ADDRESS PLUS 8 IS                     73206230
166  40 3617            624          A      MAR,MR6,AR   ADRS OF CHECK WORD                        73206240
167  08 0C0F            625          L      FLR,MR1,SR+MR (FLR)=CCW BITS 11:14                     73206250
168  E2 04C5            626          BT     C,CRCTEST    DO CYCLIC REDUNDANCY CHECK (P.47)         73206260
169  30 9C16            627  LRC     X      MDR,SRH,MDR  EXCLUSIVE-OR CHECKSUM                     73206270
16A  0E 0C0F            628  RETCRC  L      FLR,MR1,SR+MW STORE NEW CHECKWORD                      73206280
16B  E0 8174            629          BT     G,RCHKW      BRANCH IF R/W = 1                         73206290
16C  00 A017            630          L      MAR,LOC      ADRS OF HALFWORD                          73206300
16D  08 8010            631          L      NULL,NULL,MR FETCH EVEN/ODD BYTE PAIR                  73206310
16E  0E 1616            632          L      MDR,MR2,CS+MW STORE INPUT DATA BYTE                    73206320
16F  F0 0175            633          B      NFRW         BRANCH                                    73206330
                        634  *                                                                     73206340
                        635  *                                                                     73206350
170  00 B609            636  NFWRITE L      ARL,MDR,CS                                             73206360
171  9F F202            637          NI     MR2,'FF',ARL (MR2)=CHARACTER                           73206370
172  E0 415A            638          BT     L,TRANSL     GO TRANSLATE IF T = 1                     73206380
173  F0 0164            639          B      RTRANW       BACK TO COMMON CODE                       73206390
                        640  *                                                                     73206400
                        641  *                                                                     73206410
174  00 1055            642  RCHKW   L      IO,MR2,DA    OUTPUT THE DATA BYTE                      73206420
175  00 1617            643  NFRW    L      MAR,MR3      ADRS OF BUFFER BYTE COUNT                 73206430
176  4E 2116            644          A      MDR,MR4,ONE,MW STORE UPDATED COUNT                     73206440
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177  50 8430   645          S    NULL,NULL,MDR,F     TEST NEW COUNT                          73206450
178  F0 4140   646          BF   L,EXAUTO            BRANCH IF NOT POSITIVE (P,15)           73206460
179  00 3017   647          L    MAR,MR6             (MAR)=ADRS OF CCW                       73206470
17A  80 8009   648          LI   ARL,'8'                                                     73206480
17B  3E 0A16   649          X    MDR,MR1,ARL,MW      COMPLEMENT B BIT IN CCW                 73206490
               650  *                                                                       73206500
17C  80 200F   651  EXSUB3   LI   FLR,2              CC=2                                    73206510
17D  81 400B   652  EXSUB1   LI   AR,'14'                                                   73206520
17E  40 3617   653          A    MAR,MR6,AR                                                 73206530
17F  78 0088   654          C    MR+JH               FETCH SUBROUTINE ADDRESS                73206540
180  00 8018   655  EXIT     L    YDH,NULL            (R4)=CCB ADDRESS                        73206550
181  00 301B   656          L    YDLM1,MR6                                                  73206560
182  00 8018   657          L    YDH,NULL            (R3<0:15>)=0                            73206570
183  00 B014   658          L    LOC,MDR             (LOC)=(MAR)=SUBROUTINE ADRS             73206580
184  05 0810   659          L    NULL,YDLM1,IRJH     FETCH NEXT INSTRUCTION                  73206590
185  00 8018   660          L    YDH,NULL            (R2<0:15>)=0                            73206600

186  80 300C   662  EXTRAN   LI   YSI,3              POINT TO REGISTER 3                     73206620
187  00 101D   663          L    YSL,MR2             R3=UNTRANSLATED CHARACTER               73206630
188  00 B216   664          L    MDR,MDR,SL          (MDR)=SUBROUTINE ADDRESS                73206640
189  00 800F   665          L    FLR,NULL            CC=0                                    73206650
18A  F0 0180   666          B    EXIT                                                        73206660
               667  *                                                                       73206670
18B  30 100F   668  EXSUB2   LI   FLR,1              CC=1                                    73206680
18C  F0 0170   669          B    EXSUB1                                                      73206690
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                        671  * COMMON DROM1 ENTRY POINT FOR HALFWORD RX INSTRUCTIONS                    73206710
                        672  *                                                                          73206720
18D   60 A417           673  RXH     CA    MAR,LOC,MDR     CALCULATE EFFECT 2ND OP ADRS               73206730
18E   08 A017           674          L     MAR,LOC,MR      START MEMORY READ THEN SET                 73206740
                        675  *                               MAR EQUAL TO LOC                         73206750
18F   03 B009           676          L     ARL,MDR,D2      (ARH,ARL)=32 BIT VALUE                     73206760
190   40 850A           677          A     ARH,NULL,SIGN   EXTEND HALFWORD SIGN                       73206770
                        678  *                               THROUGH (ARH) THEN VECTOR                73206780
                        679  *                               THROUGH DROM2.                           73206790


                        681  * COMMON DROM1 ENTRY POINT FOR FULLWORD RX INSTRUCTIONS                    73206810
                        682  *                                                                          73206820
191   60 A417           683  RXF     CA    MAR,LOC,MDR     CALCULATE EFFECTIVE 2ND OP ADRS            73206830
192   09 8010           684          L     NULL,NULL,MR2   START READ, INCREMENT MAR BY 2              73206840
193   08 B00A           685          L     ARH,MDR,MR      (ARH)=MS 16 BITS OF 2ND OP                 73206850
194   03 A017           686          L     MAR,LOC,D2      (MAR)=(LOC)                                73206860
195   00 B009           687          L     ARL,MDR         (ARL)=LS 16 BITS OF 2ND OP                 73206870
                        688  *                               VECTOR THROUGH DROM 2                    73206880


                        690  * COMMON DROM 1 ENTRY POINT FOR HALFWORD RI INSTRUCTIONS                   73206900
                        691  *                                                                          73206910
196   43 F449           692  RI1     A     ARL,YSLX,MDR,CO+D2  (ARH,ARL)=EXTENDED IMM. FIELD          73206920
197   40 FD8A           693          A     ARH,YSHX,SIGN,CI    PLUS INDEX VALUE.                      73206930
                        694  *                               VECTOR THROUGH DROM2                     73206940


                        696  * COMMON DROM1 ENTRY POINT FOR FULLWORD RI INSTRUCTIONS                    73206960
                        697  *                                                                          73206970
198   01 B00A           698  RI2     L     ARH,MDR,MRI     (ARH)=MS 16 BITS OF 2ND OP                 73206980
                        699  *                               INCREMENT LOC & MAR BY 2                 73206990
199   43 F449           700          A     ARL,YSLX,MDR,CO+D2  ADD INDEX VALUE                        73207000
19A   40 FF8A           701          A     ARH,YSHX,ARH,CI     (ARH,ARL)=2ND OPERAND;                 73207010
                        702  *                               VECTOR THROUGH DROM2                     73207020


                        704  * COMMON DROM 1 ENTRY POINT FOR SRLS,SLLS                                  73207040
                        705  *                                                                          73207050
19B   00 6448           706  SRLLS   L     CTR,YSI,SR+CO   SHIFT COUNT/2                              73207060
                        707  *                               CARRY=1 IF COUNT ODD                     73207070
19C   03 C013           708          L     SRH,YDH,D2      SRH=HIGH 1ST OPERAND                       73207080
                        709  *                               VECTOR THROUGH DROM2                     73207090
19D   00 C812           710          L     SRL,YDL         SRL=LOW 1ST OPERAND                        73207100
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                                712  * COMMON DROM 1 ENTRY POINT FOR SRL,SLL                                  73207120
                                713  *                                                                        73207130
19E     00 C013                 714  SRLL    L       SRH,YDH         (SRH)=HIGH 1ST OPERAND                   73207140
19F     40 F409                 715          A       ARL,YSLX,MDR    (ARL)=A(X2) FIELD                        73207150
1A0     91 F200                 716          NI      MR0,'1F',ARL    MASK 5 BIT SHIFT COUNT                   73207160
1A1     03 0448                 717          L       CTR,MR0,SR+C0+D2 COUNT/2 TO COUNTER, IF                  73207170
                                718  *                               COUNT ODD, SET CARRY                     73207180
                                719  *                               VECTOR THROUGH DROM2                     73207190
1A2     00 C812                 720          L       SRL,YDL         (SRL)=LOW 1ST OPERAND                    73207200


                                722  * COMMON DROM 1 ENTRY POINT FOR RLL,RRL                                  73207220
                                723  *                                                                        73207230
1A3     00 C013                 724  RLRR    L       SRH,YDH         (SRH,SRL)=FIRST OPERAND                  73207240
1A4     03 C812                 725          L       SRL,YDL,D2      VECTOR THROUGH DROM 2                    73207250
1A5     40 F408                 726          A       CTR,YSLX,MDR    COUNTER GETS A+(X2)                      73207260


                                728  * COMMON DROM 1 ENTRY POINT FOR SLHL,SRHL,SLHA,SRHA                      73207280
                                729  *                                                                        73207290
1A6     43 F409                 730  SLRH    A       ARL,YSLX,MDR,D2 (ARL)=SHIFT COUNT                        73207300
1A7     90 F208                 731          NI      CTR,X'F',ARL    COPY TO COUNTER; VECTOR                  73207310
                                732  *                                    THROUGH DROM 2                      73207320


                                734  * COMMON DROM 1 ENTRY FOR SBT,CBT,RBT,TBT                                73207340
                                735  *                                                                        73207350
1A8     60 A417                 736  XBIT    CA      MAR,LOC,MDR     (MAR)=2ND OP ADDRESS                     73207360
1A9     00 C013                 737          L       SRH,YDH                                                  73207370
1AA     00 C812                 738          L       SRL,YDL         (SRH,SRL)=BIT DISPLACEMENT               73207380
1AB     70 0C00                 739          C       SR2                                                      73207390
1AC     00 9C4A                 740          L       ARH,SRH,SR+C0   (ARH,ARL)=BYTE DISPLACEMENT              73207400
1AD     00 9489                 741          L       ARL,SRL,SR+C1                                            73207410
1AE     40 BE17                 742          A       MAR,MAR,AR      ADDRESS ONE PARTICULAR BYTE              73207420
1AF     88 0016                 743          LI      MDR,'80'        (MDR)='0080'                             73207430
1B0     08 B600                 744          L       MR0,MDR,CS+MR   (MR0)='8000' OR '00A0'                  73207440
1B1     80 7009                 745          LI      ARL,7                                                    73207450
1B2     10 CA08                 746          N       CTR,YDL,ARL     GENERATE SHIFT COUNT                     73207460
1B3     70 0008                 747          C       RPT                                                      73207470
1B4     00 0400                 748          L       MR0,MR0,SR      SHIFT MASK RIGHT N TIMES                 73207480
1B5     13 0429                 749          N       ARL,MR0,MDR,F+D2 TEST MASK AGAINST TARGET BIT            73207490
1B6     00 8070                 750          L       NULL,NULL,C0+F  VECTOR THROUGH DROM 2                    73207500
                                751  *                               CLEAR C FLAG, G FLAG=1 IF                73207510
                                752  *                               SELECTED BIT WAS SET                     73207520
                                753  *                                                                        73207530
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                01B7          755  LR      EQU   *                                LOAD REGISTER                  * 08 *  73207550
                01B7          756  LH      EQU   *                                LOAD HALFWORD                  * 48 *  73207560
                01B7          757  L       EQU   *                                LOAD                           * 58 *  73207570
                01B7          758  LHI     EQU   *                                LOAD HALFWORD IMMEDIATE        * C8 *  73207580
                01B7          759  LI      EQU   *                                LOAD IMMEDIATE                 * F8 *  73207590
                              760  *                                                                                     73207600
1B7       47 8279             761       A       YDL,NULL,ARL,C0+F+IRJ SECOND OPERAND TO R1                           73207610
1B8       40 8778             762       A       YDH,NULL,ARH,C0+F                                                    73207620
                              763  *                                                                                     73207630
                01B9          764  LIS     EQU   *                                LOAD IMMEDIATE SHORT           * 24 *  73207640
                              765  *                                                                                     73207650
1B9       07 6079             766       L       YDL,YSI,C0+F+IRJ       R2 FIELD TO R1                                73207660
1BA       00 8078             767       L       YDH,NULL,C0+F                                                        73207670
                              768  *                                                                                     73207680
                01BB          769  LCS     EQU   *                                LOAD COMPLEMENT SHORT          * 25 *  73207690
                              770  *                                                                                     73207700
1BB       00 6009             771       L       ARL,YSI                2'S COMP OF R2 FIELD TO R1                    73207710
1BC       50 8279             772       S       YDL,NULL,ARL,C0+F                                                    73207720
1BD       47 80C9             773       A       ARL,NULL,NULL,CI+C0+IRJ CARRY =0                                     73207730
1BE       50 8238             774       S       YDH,NULL,ARL,F                                                       73207740
                              775  *                                                                                     73207750
                01BF          776  LA      EQU   *                                LOAD ADDRESS                   * E6 *  73207760
                              777  *                                                                                     73207770
1BF       60 A417             778       CA      MAR,LOC,MDR            (MAR)=2ND OP ADDRESS                          73207780
1C0       00 B808             779       L       AR,MAR                 ADDRESS TO (ARH,ARL)                          73207790
1C1       00 A017             780       L       MAR,LOC                (MAR)=(LOC)                                   73207800
1C2       44 8219             781       A       YDL,NULL,ARL,IR        EFFECTIVE ADDRESS TO R1                       73207810
1C3       40 8718             782       A       YDH,NULL,ARH                                                         73207820
                              783  *                                                                                     73207830
                01C4          784  LRA     EQU   *                                LOAD REAL ADDRESS              * 63 *  73207840
                              785  *                                                                                     73207850
1C4       60 A417             786       CA      MAR,LOC,MDR            (MAR)=2ND OP ADDRESS                          73207860
1C5       00 C200             787       L       MR0,YDH,SL             THE REGISTER SPECIFIED BY R1                  73207870
1C6       00 0209             788       L       ARL,MR0,SL             CONTAINS THE PROGRAM ADDRESS                  73207880
                              789  *                                   THAT IS TO BE CONVERTED TO A                  73207890
                              790  *                                   REAL ADDRESS.  THE CONVERSION                 73207900
                              791  *                                   IS ACCOMPLISHED BY STIMULATING                73207910
                              792  *                                   THE OPERATION OF THE MEMORY                   73207920
                              793  *                                   ACCESS CONTROLLER, USING AN                   73207930
                              794  *                                   IMAGE IN MEMORY OF THE                        73207940
                              795  *                                   SEGMENTATION REGISTERS.  BITS                 73207950
1C7       93 C20B             796       NI      AR,'3C',ARL            12 THROUGH 15 OF R1 SPECIFY                   73207960
1C8       40 BA17             797       A       MAR,MAR,ARL            THE SEGMENT NUMBER.  ADD 4X THE               73207970
                              798  *                                   SEGMENT NUMBER TO THE IMAGE                   73207980
1C9       09 C801             799       L       MR1,YDL,MR2            START ADDRESS.  COPY BITS 16:31               73207990
1CA       00 CE09             800       L       ARL,YDL,CS             OF R1 TO MR1 (BLOCK NUMBER AND                73208000
1CB       9F F209             801       NI      ARL,'FF',ARL           BYTE DISPLACEMENT) AND FETCH                  73208010
                              802  *                                   BITS 0:15 OF THE SEGMENTATION                 73208020
1CC       0B B012             803       L       SRL,MDR,XR2            REGISTER.  COPY TO SRL AND START              73208030
                              804  *                                   EXTENDED READ FOR BITS 12:31.                 73208040
1CD       70 0C00             805       C       SR2                    POSITION SEGMENT LIMIT FIELD                  73208050
1CE       70 0C00             806       C       SR2                                                                  73208060
1CF       00 A017             807       L       MAR,LOC                (MAR)=(LOC)                                   73208070
1D0       50 9250             808       S       NULL,SRL,ARL,C0        COMPARE PROG ADRS TO LIMIT                    73208080
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1D1     E2 00F6     809          BT    C,LR&ERR     IF PROG ADRS EXCEEDS THE                73208090
                    810  *                         SEGMENT LIMIT FIELD, DON'T CHANGE       73208100
                    811  *                         R1...EXIT WITH A C FLAG SET             73208110
                    812  *                         IN CC  LIMIT VIOLATION  (P,13)          73208120
                    813  *                         OR NOT MAPPED                           73208130
                    814  *                                                                 73208140
1D2     8F F609     815          LI    ARL,'FF',CS  (ARL)='FF00'                            73208150
1D3     00 B002     816          L     MR2,MDR      SAVE CONTROL BITS IN MR2                73208160
1D4     10 B216     817          N     MDR,MDR,ARL  CLEAR OUT LS 8 BITS OF MDR              73208170
1D5     40 0C0B     818          A     AR,MR1,MDR   ADD SEGMENT RELOCATION FIELD           73208180
                    819  *                         IN MDR 12:23 TO THE BLOCK               73208190
                    820  *                         NUMBER & BYTE DISPLACEMENT.             73208200
                    821  *                         RELOCATED ADDRESS TO ARH,ARL            73208210
1D6     00 1412     822          L     SRL,MR2,SR   SHIFT CONTROL FIELD DOWN                73208220
1D7     70 0C00     823          C     SR2          FOUR BIT POSITIONS                      73208230
1D8     00 940F     824          L     FLR,SRL,SR   TO FLR FOR TESTING                     73208240
1D9     F0 42B2     825          BF    L,LSTOUF     NOT PRESENT...CC=0100 (P,29)            73208250
1DA     40 8718     826          A     YDH,NULL,ARH REAL ADDRESS REPLACES THE               73208260
1DB     40 8219     827          A     YDL,NULL,ARL ORIGINAL PROGRAM ADDRESS                73208270
1DC     E1 80F8     828          BT    V+G,SETG     WRITE PROTECT...CC=0010 (P,13)          73208280
1DD     E2 00FA     829          BT    C,SETL       EXECUTE PROTECT...CC=0001 (P,13)        73208290
1DE     07 8010     830          L     NULL,NULL,TRJ NO RESTRICTIONS...CC = 0000            73208300
1DF     00 800F     831          L     FLR,NULL                                             73208310
                    832  *                                                                 73208320
        01E0        833  LHI     EQU   *            LOAD HALFWORD LOGICAL        * 73 *     73208330
                    834  *                                                                 73208340
1E0     47 8239     835          A     YDL,NULL,ARL,IRJ+F 2ND OP <16:31> TO R1              73208350
1E1     00 8018     836          L     YDH,NULL     R1 <0:15> GETS ZERO                     73208360
                    837  *                                                                 73208370
        01E2        838  LM      EQU   *            LOAD MULTIPLE                * 01 *     73208380
                    839  *                                                                 73208390
1E2     60 A417     840          CA    MAR,LOC,MDR  (MAR)=2ND OP ADDRESS                    73208400
1E3     00 6809     841          L     ARL,YDI                                              73208410
1E4     D0 F208     842          SI    CTR,'0F',ARL CTR=NUMBER OF REGS -1                   73208420
1E5     79 0000     843  LMLOOP  C     MR2          FETCH MS 16 BITS OF ONE REG.            73208430
1E6     09 B018     844          L     YDH,MDR,MR2  LOAD 0:15, FETCH LS 16 BITS             73208440
1E7     00 B01A     845          L     YDLP1,MDR    LOAD BITS 16:31                         73208450
1E8     FC 81E5     846          BF    CNTR,LMLOOP  LOOP IF COUNTER NOT ZERO                73208460
1E9     F0 02CC     847          B     NBR          EXIT (P,30)                             73208470
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                01EA                    849  LB      EQU   *                 LOAD BYTE                        * D3 *   73208490
                                        850  *                                                                       73208500
1EA       60 A417                       851           CA    MAR,LOC,MDR       (MAR)=2ND OP ADDRESS                   73208510
1EB       08 8010                       852           L     NULL,NULL,MR      FETCH EVEN/ODD BYTE PAIR               73208520
1EC       00 8609                       853           L     ARL,MDR,CS        PROPER BYTE TO ARL                     73208530
1ED       00 A017                       854           L     MAR,LOC                                                  73208540
                                        855  *                                                                       73208550
                01EE                    856  LBR     EQU   *                 LOAD BYTE REGISTER               * 93 *   73208560
                                        857  *                                                                       73208570
1EE       9F F219                       858           NI    YDL,X'FF',ARL     R1 <0:23> GETS ZERO                    73208580
                                        859  *                                R1 <24:31> = RESULT BYTE               73208590
1EF       04 8010                       860           L     NULL,NULL,IR      FETCH NEXT INSTRUCTION                 73208600
1F0       00 8018                       861           L     YDH,NULL          CLEAR R1 <0:15>                        73208610
                                        862  *                                                                       73208620
                01F1                    863  EXHR    EQU   *                 EXCHANGE HALFWORD REGISTER       * 34 *   73208630
                                        864  *                                                                       73208640
1F1       44 8218                       865           A     YDH,NULL,ARL,IR   R1 <0:15> = R2 <16:31>                 73208650
1F2       40 8719                       866           A     YDL,NULL,ARH      R1 <16:31> = R2 <0:15>                 73208660
                                        867  *                                                                       73208670
                01F3                    868  EXBR    EQU   *                 EXCHANGE BYTE REGISTER           * 94 *   73208680
                                        869  *                                                                       73208690
1F3       04 EE19                       870           L     YDL,YSL,CS+IR     R1 <16:23> = R2 <24:31>                73208700
                                        871  *                                R1 <24:31> = R2 <16:23>                73208710
1F4       00 8010                       872           L     NULL,NULL         NOP                                    73208720
                                        873  *                                                                       73208730
                01F5                    874  ST      EQU   *                 STORE                            * 50 *   73208740
                                        875  *                                                                       73208750
1F5       60 A417                       876           CA    MAR,LOC,MDR       (MAR)=2ND OP ADDRESS                   73208760
1F6       0F C016                       877           L     MDR,YDH,MW2       STORE R1(0:15)                         73208770
1F7       0E C816                       878           L     MDR,YDL,MW        STORE R1(16:31)                        73208780
1F8       F0 02CC                       879           B     NBR               EXIT (P,30)                            73208790
                                        880  *                                                                       73208800
                01F9                    881  STH     EQU   *                 STORE HALFWORD                   * 40 *   73208810
                                        882  *                                                                       73208820
1F9       60 A417                       883           CA    MAR,LOC,MDR       (MAR)=2ND OP ADDRESS                   73208830
1FA       0E C816                       884           L     MDR,YDL,MW        STORE R1(16:31)                        73208840
1FB       F0 02CC                       885           B     NBR               EXIT (P,30)                            73208850
1FC       00 8010                       886           L     NULL,NULL         FILLER (NOT USED)                      73208860
1FD       00 8010                       887           L     NULL,NULL         FILLER (NOT USED)                      73208870
1FE       00 8010                       888           L     NULL,NULL         FILLER (NOT USED)                      73208880
                                        889  *                                IF PRIVILEGED INSTR & PROTECT          73208890
1FF       F0 0003                       890           B     ILLEG             MODE, GO TO ILLEGAL (P,3)              73208900
                                        891  *                                                                       73208910
                0200                    892  STM     EQU   *                 STORE MULTIPLE                   * D0 *   73208920
                                        893  *                                                                       73208930
200       60 A417                       894           CA    MAR,LOC,MDR       (MAR)=2ND OP ADDRESS                   73208940
201       00 6809                       895           L     ARL,YDI                                                  73208950
202       D0 F208                       896           SI    CTR,X'0F',ARL     CTR=NUMBER OF REGS -1                  73208960
203       0F C016                       897  STMLOOP  L     MDR,YDH,MW2       STORE BITS 0:15                        73208970
204       0F D016                       898           L     MDR,YDLP1,MW2     STORE BITS 16:31                       73208980
205       FC 8203                       899           BF    CNTR,STMLOOP      LOOP IF COUNTER NOT ZERO               73208990
206       F0 02CC                       900           B     NBR               EXIT (P,30)                            73209000
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                0207                902  STR     EQU   *                    STORE BYTE                  * 02 *  73209020
                                    903  *                                                                     73209030
207       60 A417                   904          CA    MAR,LOC,MDR          (MAR)=2ND OP ADDRESS                73209040
208       08 8010                   905          L     NULL,NULL,MR         FETCH EVEN/ODD BYTE PAIR            73209050
209       0E CE16                   906          L     MDR,YDL,CS+MW        MODIFY ONE OF THEM                  73209060
20A       00 A017                   907          L     MAR,LOC              ADRS NEXT INSTRUCTION               73209070
20B       04 8010                   908          L     NULL,NULL,IR         AND FETCH                           73209080
                                    909  *                                                                     73209090
                020C                910  STBR    EQU   *                    STORE BYTE REGISTER         * 92 *  73209100
                                    911  *                                                                     73209110
20C       8F F609                   912          LI    ARL,'FF',CS          (ARL)='FF00'                        73209120
20D       10 EA01                   913          N     MR1,YSL,ARL          MR1(0:7)=R2(16:23)                  73209130
20E       8F F009                   914          LI    ARL,'FF'             (ARL)='00FF'                        73209140
20F       10 CA09                   915          N     ARL,YDL,ARL          (ARL)=R2 <24:31>                    73209150
210       24 0A10                   916          O     YSL,MR1,ARL,IR       COMBINE & LOAD R2 <16:31>           73209160
                                    917  *                                                                     73209170
211       80 000F                   918  CRI     LI    FLR,'0'              FROM CR:CLEAR FLR                   73209180
                                    919  *                                                                     73209190
                0212                920  CLR     EQU   *                    COMPARE LOGICAL REGISTER    * 05 *  73209200
                0212                921  CLH     EQU   *                    COMPARE LOGICAL HALFWORD    * 45 *  73209210
                0212                922  CL      EQU   *                    COMPARE LOGICAL             * 55 *  73209220
                0212                923  CLHI    EQU   *                    COMPARE LOGICAL HW IMMED.   * C5 *  73209230
                0212                924  CLI     EQU   *                    COMPARE LOGICAL IMMEDIATE   * F5 *  73209240
                                    925  *                                                                     73209250
212       57 CA70                   926          S     NULL,YDL,ARL,CO+F+IRJ SUBTRACT TO SET FLAGS               73209260
213       50 C7F0                   927          S     NULL,YDH,ARH,CI+CO+F                                      73209270
                                    928  *                                                                     73209280
                0214                929  CLR     EQU   *                    COMPARE LOGICAL BYTE        * D4 *  73209290
                                    930  *                                                                     73209300
214       60 A417                   931          CA    MAR,LOC,MDR          (MAR)=2ND OP ADDRESS                73209310
215       08 C809                   932          L     ARL,YDL,MR           ARL=1ST OPERAND; FETCH              73209320
                                    933  *                                 EVEN/ODD BYTE PAIR                  73209330
216       9F F200                   934          NI    MR0,'FF',ARL         ISOLATE 1ST OP BYTE                 73209340
217       00 B609                   935          L     ARL,MDR,CS           GET PROPER BYTE INTO POSITION       73209350
218       9F F209                   936          NI    ARL,'FF',ARL         ISOLATE IT                          73209360
219       00 A017                   937          L     MAR,LOC              (MAR)=(LOC)                         73209370
21A       57 0270                   938          S     NULL,MR0,ARL,CO+F+IRJ SUBTRACT TO COMPARE                 73209380
21B       00 8010                   939          L     NULL,NULL            NOP                                 73209390
                                    940  *                                                                     73209400
                021C                941  NR      EQU   *                    AND REGISTER                * 04 *  73209410
                021C                942  NH      EQU   *                    AND HALFWORD                * 44 *  73209420
                021C                943  N       EQU   *                    AND                         * 54 *  73209430
                021C                944  NHI     EQU   *                    AND HALFWORD IMMEDIATE      * C4 *  73209440
                021C                945  NI      EQU   *                    AND IMMEDIATE               * F4 *  73209450
                                    946  *                                                                     73209460
21C       17 CA79                   947          N     YDL,YDL,ARL,CO+F+IRJ R1 'AND' 2ND OP TO R1            73209470
21D       10 C778                   948          N     YDH,YDH,ARH,CO+F                                      73209480
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                                                                                                                    73209500
021E                    950  OR      EQU   *          OR REGISTER                          * 06 *                73209510
021E                    951  OH      EQU   *          OR HALFWORD                          * 46 *                73209520
021E                    952  O       EQU   *          OR                                   * 56 *                73209530
021E                    953  OHT     EQU   *          OR HALFWORD IMMEDIATE                * C6 *                73209540
021E                    954  OI      EQU   *          OR IMMEDIATE                         * F6 *                73209550
                        955  *                                                                                    73209560
21F     27 CA79         956          O     YDL,YDL,ARL,CO+F+IRJ R1 'OR' 2ND OP TO R1                              73209570
21F     20 C778         957          O     YDH,YDH,ARH,CO+F                                                       73209580
                        958  *                                                                                    73209590
0220                    959  XR      EQU   *          EXCLUSIVE-OR REGISTER                * 07 *                73209600
0220                    960  XH      EQU   *          EXCLUSIVE-OR HALFWORD                * 47 *                73209610
0220                    961  X       EQU   *          EXCLUSIVE-OR                         * 57 *                73209620
0220                    962  XHT     EQU   *          EXCLUSIVE-OR HW IMMEDIATE            * C7 *                73209630
0220                    963  XI      EQU   *          EXCLUSIVE-OR IMMEDIATE               * F7 *                73209640
                        964  *                                                                                    73209650
220     37 CA79         965          X     YDL,YDL,ARL,CO+F+IRJ R1 'XOR' 2ND OP TO R1                             73209660
221     30 C778         966          X     YDH,YDH,ARH,CO+F                                                       73209670
                        967  *                                                                                    73209680
0222                    968  THT     EQU   *          TEST HALFWORD IMMEDIATE              * C3 *                73209690
0222                    969  TI      EQU   *          TEST IMMEDIATE                       * F3 *                73209700
                        970  *                                                                                    73209710
222     17 CA70         971          N     NULL,YDL,ARL,CO+F+IRJ 'AND' TO TEST BITS                               73209720
223     10 C770         972          N     NULL,YDH,ARH,CO+F                                                      73209730
                        973  *                                                                                    73209740
0224                    974  SLLS    EQU   *          SHIFT LEFT LOGICAL SHORT             * 11 *                73209750
0224                    975  SLI     EQU   *          SHIFT LEFT LOGICAL                   * ED *                73209760
                        976  *                                                                                    73209770
224     F2 0226         977          BF    C,*+2      SKIP IF EVEN SHIFT COUNT                                    73209780
225     70 1040         978          C     SL1+CO     DO ODD SHIFT                                                73209790
226     70 0008         979          C     RPT        REPEAT NEXT INSTRUCTION                                     73209800
227     70 1440         980          C     SL2+CO     SHIFT 2 PLACES, ADJUST C                                    73209810
228     07 9039         981          L     YDL,SRL,F+IRJ  LOAD RESULT, ADJUST G&L                                 73209820
229     00 9838         982          L     YDH,SRH,F                                                              73209830
                        983  *                                                                                    73209840
022A                    984  SRLS    EQU   *          SHIFT RIGHT LOGICAL SHORT            * 10 *                73209850
022A                    985  SRI     EQU   *          SHIFT RIGHT LOGICAL                  * EC *                73209860
                        986  *                                                                                    73209870
22A     F2 022C         987          BF    C,*+2      SKIP IF EVEN SHIFT COUNT                                    73209880
22B     70 0840         988          C     SR1+CO     DO ODD SHIFT                                                73209890
22C     70 0008         989          C     RPT        REPEAT NEXT INSTRUCTION                                     73209900
22D     70 0C40         990          C     SR2+CO     SHIFT 2 BITS AT A TIME                                      73209910
22E     07 9039         991          L     YDL,SRL,F+IRJ  LOAD RESULT, ADJUST G & L                               73209920
22F     00 9838         992          L     YDH,SRH,F
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                0230                994  SLHLS   EQU   *                 SHIFT LEFT HW LOGICAL SHORT   * 91 *  73209940
                                    995  *                                                                    73209950
230          00 6008                996          L     CTR,YSI           COUNTER GETS SHIFT COUNT              73209960
                                    997  *                                                                    73209970
                0231                998  SLHL    EQU   *                 SHIFT LEFT HW LOGICAL         * CD *  73209980
                                    999  *                                                                    73209990
231          70 0008               1000          C     RPT               REPEAT NEXT INSTRUCTION               73210000
232          00 CA59               1001          L     YDL,YDL,SL+CO     SHIFT LS 16 BITS, ADJUST C            73210010
233          05 C839               1002          L     YDL,YDL,F+IRJH    ADJUST G&L, FETCH NEXT                73210020
                                    1003 *                                                                    73210030
                0234                1004 SRHLS   EQU   *                 SHIFT RIGHT HW LOGICAL SHORT  * 90 *  73210040
                                    1005 *                                                                    73210050
234          00 6008               1006          L     CTR,YSI           COUNTER GETS SHIFT COUNT              73210060
                                    1007 *                                                                    73210070
                0235                1008 SRHL    EQU   *                 SHIFT RIGHT HW LOGICAL        * CC *  73210080
                                    1009 *                                                                    73210090
235          70 0008               1010          C     RPT               REPEAT NEXT INSTRUCTION               73210100
236          00 CC59               1011          L     YDL,YDL,SR+CO     SHIFT LS 16 BITS, ADJUST C            73210110
237          05 C839               1012          L     YDL,YDL,F+IRJH    ADJUST G&L, FETCH NEXT                73210120
238          00 8010               1013          L     NULL,NULL         NOP                                   73210130
                                    1014 *                                                                    73210140
                0239                1015 RLI     EQU   *                 ROTATE LEFT LOGICAL           * EB *  73210150
                                    1016 *                                                                    73210160
239          EC 823D               1017          BT    CNTR,RLX          EXIT IF COUNTER=0                     73210170
23A          00 9A50               1018 RLI1     L     NULL,SRH,SL+CO    MSB TO CARRY                          73210180
23B          70 1200               1019          C     SL1+CI            DO ROTATE                             73210190
23C          FC 823A               1020          BF    CNTR,RLL1         REPEAT IF NOT DONE                    73210200
23D          07 9079               1021 RLX      L     YDL,SRL,F+CO+IRJ  RESULT TO R1, CLEAR CARRY             73210210
23E          00 9838               1022          L     YDH,SRH,F         ADJUST G&L                            73210220
                                    1023 *                                                                    73210230
                023F                1024 RRI     EQU   *                 ROTATE RIGHT LOGICAL          * EA *  73210240
                                    1025 *                                                                    73210250
23F          EC 8243               1026          BT    CNTR,RRX          EXIT IF COUNTER=0                     73210260
240          00 9450               1027 RRI1     L     NULL,SRL,SR+CO    LSB TO CARRY                          73210270
241          70 0A00               1028          C     SR1+CI            DO ROTATE                             73210280
242          FC 8240               1029          BF    CNTR,RRL1         REPEAT IF NOT DONE                    73210290
243          07 9079               1030 RRX      L     YDL,SRL,F+CO+IRJ  RESULT TO R1, CLEAR CARRY             73210300
244          00 9838               1031          L     YDH,SRH,F         ADJUST G&L                            73210310
                                    1032 *                                                                    73210320
                0245                1033 TS      EQU   *                 TEST AND SET                  * E0 *  73210330
                                    1034 *                                                                    73210340
245          60 A417               1035          CA    MAR,LOC,MDR       (MAR)=2ND OP ADDRESS                  73210350
246          78 0082               1036          C     MR+TS             READ H.W. RE-WRITE WITH               73210360
                                    1037 *                               BIT ZERO SET IF SHARED MEMORY         73210370
247          00 B030               1038          L     NULL,MDR,F        TEST PREVIOUS STATE                   73210380
248          F0 40F4               1039          BF    L,TS1             RE-WRITE ALL ONES IF RESET (P,13)     73210390
249          F0 044B               1040          B     FETCHJ            EXIT (P,43)                           73210400
                                    1041 *                                                                    73210410
                024A                1042 TBT     EQU   *                 TEST BIT                      * 74 *  73210420
                                    1043 *                                                                    73210430
24A          F0 044B               1044          B     FETCHJ            EXIT TO SET CC (P,43)                 73210440
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                0248                1046  SBT       EQU   *                        SET BIT                          * 75 *  73210460
                                    1047  *                                                                               73210470
248     2E 0416                     1048              O     MDR,MR0,MDR,MW           SET THE BIT                             73210480
24C     F0 0448                     1049              B     FETCHJ                   EXIT TO SET CC (P.43)                   73210490
                                    1050  *                                                                               73210500
                0249                1051  CBT       EQU   *                        COMPLEMENT BIT                   * 77 *  73210510
                                    1052  *                                                                               73210520
249     3E 0416                     1053              X     MDR,MR0,MDR,MW           COMPLEMENT THE BIT                      73210530
24E     F0 044B                     1054              B     FETCHJ                   EXIT TO SET CC (P.43)                   73210540
                                    1055  *                                                                               73210550
                024F                1056  RBT       EQU   *                        RESET BIT                        * 76 *  73210560
                                    1057  *                                                                               73210570
24F     3E B216                     1058              X     MDR,MDR,ARL,MW           XOR WITH SELF TO RESET                  73210580
250     F0 044B                     1059              B     FETCHJ                   EXIT TO SET CC (P.43)                   73210590
                                    1060  *                                                                               73210600
                0251                1061  CRC12     EQU   *                        CYCLIC REDUNDANCY CHECK 12       * 5E *  73210610
                                    1062  *                                                                               73210620
251     60 A417                     1063              CA    MAR,LOC,MDR              (MAR)=2ND OP ADDRESS                    73210630
252     08 C813                     1064              L     SRH,YDL,MR               R1 CONTAINS CHARACTER TO                 73210640
253     70 0010                     1065              C     CUT                      INCLUDE, FETCH CHECKWORD                73210650
254     80 5008                     1066              LI    CTR,5                    FOR 6-BIT CHARACTER, COUNTER            73210660
255     80 F012                     1067              LI    SRL,'F'                  GETS BIT COUNT-1=5                      73210670
256     83 F009                     1068              LI    ARL,'3F'                 (SRL) SET UP TO GENERATE                73210680
                                    1069  *                                        FEED-BACK PATTERN '0F01'                73210690
                                    1070  *                                        (ARL)=6-BIT CHARACTER MASK              73210700
257     F0 025E                     1071              B     COMCRC                   GO TO COMMON ROUTINE                    73210710
                                    1072  *                                                                               73210720
                0258                1073  CRC16     EQU   *                        CYCLIC REDUNDANCY CHECK 16       * 5F *  73210730
                                    1074  *                                                                               73210740
258     60 A417                     1075              CA    MAR,LOC,MDR              (MAR)=2ND OP ADDRESS                    73210750
259     08 C813                     1076              L     SRH,YDL,MR               R1 CONTAINS CHARACTER TO                73210760
25A     70 0010                     1077              C     CUT                      INCLUDE, FETCH CHECK WORD               73210770
                                    1078  *                                                                               73210780
                                    1079  * COMMON ROUTINE FOR CRC16 INSTRUCTION AND FOR                                 73210790
                                    1080  * CYCLIC REDUNDANCY CHECK IN AUTO DRIVER CHANNEL                               73210800
                                    1081  * (SRH=I15)=CHARACTER TO INCLUDE                                               73210810
                                    1082  * (MDR)=ACCUMULATED CHECKSUM                                                   73210820
                                    1083  * UTILITY=1 IF AUTO DRIVER CHANNEL                                            73210830
                                    1084  *                                                                               73210840
25B     80 7008                     1085  CRCAUTO   LI    CTR,7                    COUNT FOR 8-BIT CHARACTER               73210850
25C     8A 0012                     1086              LI    SRL,'A0'                 FOR 'A001' FEED BACK VALUE              73210860
25D     8F F009                     1087              LI    ARL,'FF'                 8-BIT CHARACTER MASK                    73210870
                                    1088  *                                                                               73210880
25E     10 9A09                     1089  COMCRC    N     ARL,SRH,ARL              (ARL)=CHARACTER                         73210890
25F     30 B213                     1090              X     SRH,MDR,ARL              EXCLUSIVE OR RESIDUAL                   73210900
260     00 9609                     1091              L     ARL,SRL,CS                                                       73210910
261     A0 1209                     1092              OI    ARL,'01',ARL             (ARL)=FEED-BACK VALUE                   73210920
                                    1093  *                                        FOR CRC POLYNOMIAL                      73210930
                                    1094  *                                                                               73210940
262     00 9C53                     1095  CRCLOOP   L     SRH,SRH,SR+CO            DATA & RESIDUAL EQUATE                  73210950
263     E2 0269                     1096              BT    C,XOR1                   BRANCH IF NOT                           73210960
264     FC 8262                     1097              BF    CNTR,CRCLOOP             ELSE CONTINUE SHIFTS                    73210970
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266  00 9816   1099  DONECRC  L    MDR,SRH          NEW RESIDUAL TO MDR                    73210990
266  EC 216A   1100           BT   UT,RETCRC        GO BACK TO AUTO DRIVER                 73211000
               1101  *                              CHANNEL IF UT SET (P.17)               73211010
267  0E A017   1102           L    MAR,LOC,MW       STORE ACCUMULATED CRC                  73211020
268  F0 02D0   1103           B    FETCH            FETCH NEXT USER INSTRUCTION (P.30)     73211030
269  30 9A13   1104  XOR1     X    SRH,SRH,ARL      EXCLUSIVE-OR FEEDBACK                  73211040
26A  FC 8262   1105           BF   CNTR,CRCLOOP     LOOP ON COUNTER (P.27)                 73211050
26B  F0 0265   1106           B    DONECRC                                                 73211060
               1107  *                                                                     73211070
     026C      1108  TLATE    EQU  *                TRANSLATE                  * E7 *      73211080
               1109  *                                                                     73211090
26C  60 A417   1110           CA   MAR,LOC,MDR      (MAR)=2ND OP ADDRESS                   73211100
26D  09 C809   1111           L    ARL,YDL,MR2      (ARL)=R1<16:31>                        73211110
26E  9F F206   1112           NI   MR6,'FF',ARL     (MR6)=ARGUMENT CHARACTER               73211120
26F  30 3205   1113           X    MR5,MR6,ARL      (MR5)=R1<16:23> WITH ZEROS             73211130
270  0B 320B   1114           L    AR,MR6,SL+XR2    (AR)=2X CHARACTER                      73211140
               1115  *                              EXTENDED READ FOR TABLE ADRS           73211150
271  BF F601   1116           LI   MR1,'FF',CS      (MR1)='FF00'                           73211160
272  40 B617   1117           A    MAR,MDR,AR       ADDRESS TABLE ENTRY                    73211170
273  08 A017   1118           L    MAR,LOC,MR       FETCH HALFWORD ENTRY                   73211180
274  10 0C2A   1119           N    ARH,MR1,MDR,F    TEST BIT 0 OF HALFWORD                 73211190
275  F0 40FC   1120           BF   L,NTRANS         NO TRNSLATE IF BIT0 = 0 (P.13)         73211200
276  34 B7C9   1121           X    ARL,MDR,ARH,IR   (ARL)=TRANSLATED CHARACTER             73211210
277  20 2A19   1122           O    YDL,MR5,ARL      INSERT IN R1                           73211220
               1123  *                                                                     73211230
     0278      1124  ATI      EQU  *                ADD TO TOP OF LIST         * 64 *      73211240
     0278      1125  ABI      EQU  *                ADD TO BOTTOM OF LIST      * 65 *      73211250
               1126  *                                                                     73211260
278  60 A417   1127           CA   MAR,LOC,MDR      (MAR)=LIST ADDRESS                     73211270
279  09 8010   1128           L    NULL,NULL,MR2    FETCH MAX SLOT NUMBER                  73211280
27A  08 B009   1129           L    ARL,MDR,MR       (ARL)=NO.OF SLOTS                      73211290
27B  50 B250   1130           S    NULL,MDR,ARL,CO  COMPARE TO NUMBER USED                 73211300
27C  F2 02B2   1131           BF   C,LSTOUF         LIST FULL IF NO CARRY (P.29)           73211310
27D  4F B116   1132           A    MDR,MDR,ONE,MW2  INC. NO.USED TALLY                     73211320
27E  43 8201   1133           A    MR1,NULL,ARL,D2  (MR1)=MAX SLOT NUMBER +1               73211330
27F  00 8010   1134           L    NULL,NULL        VECTOR THROUGH DROM 0                  73211340
               1135  *                                                                     73211350
280  08 8010   1136  ATI,D2   L    NULL,NULL,MR     FETCH CURRENT TOP                      73211360
281  50 B143   1137           S    MR3,MDR,ONE,CO   (MR3)= CURRENT TOP MINUS 1            73211370
282  F2 0284   1138           BF   C,*+2            SKIP IF NO WRAP                        73211380
283  50 0903   1139           S    MR3,MR1,ONE      (MR3)= MAX SLOT NUMBER                 73211390
284  0F 1816   1140           L    MDR,MR3,MW2      STORE NEW CURRENT TOP                  73211400
285  00 1A02   1141           L    MR2,MR3,SL       (MR2)= 2X SLOT NUMBER                  73211410
286  F0 028E   1142           B    ATBL2            GO TO COMMON ROUTINE (P.29)            73211420
               1143  *                                                                     73211430
               1144  *                                                                     73211440
               1145  *                                                                     73211450
287  40 BB17   1146  ABL,D2   A    MAR,MAR,TWO      POINT TO NEXT BOTTOM POINTER           73211460
288  08 8010   1147           L    NULL,NULL,MR     FETCH IT                               73211470
289  00 B202   1148           L    MR2,MDR,SL       (MR2)= 2X SLOT NUMBER                  73211480
28A  4E B116   1149           A    MDR,MDR,ONE,MW   INCREMENT NEXT BOTTOM                 73211490
28B  50 B250   1150           S    NULL,MDR,ARL,CO  COMPARE TO MAX SLOT                    73211500
28C  E2 028E   1151           BT   C,*+2            SKIP IF NO WRAP                        73211510
28D  0E 8016   1152           L    MDR,NULL,MW      LIST WRAP, NEXT BOTTOM=0               73211520
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                                1153  *                                                                          73211530
                                1154  *                                                                          73211540
28E      00 120B                1154  ATBL2    L     AR,MR2,SL      (AR)=4X SLOT NUMBER                        73211550
28F      40 BB17                1155           A     MAR,MAR,TWO    (MAR)=ADRS OF SLOT 0                       73211560
290      40 BE17                1156           A     MAR,MAR,AR     (MAR)=ADRS OF SLOT N                       73211570
291      0F C056                1157           L     MDR,YDH,CO+MW2 STORE ELEMENT 0:15                         73211580
292      0E C816                1158  ATBL3    L     MDR,YDL,MW     STORE ELEMENT 16:31                        73211590
293      F0 044B                1159           B     FETCHJ         EXIT (P,43)                                73211600
                                1160  *                                                                          73211610
          0294                  1161  RTI      EQU   *              REMOVE FROM TOP OF LIST      * 66 *        73211620
          0294                  1162  RBI      EQU   *              REMOVE FROM BOTTOM OF LIST   * 67 *        73211630
                                1163  *                                                                          73211640
294      60 A417                1164           CA    MAR,LOC,MDR    (MAR)=LIST ADDRESS                         73211650
295      09 8010                1165           L     NULL,NULL,MR2  FETCH MAX SLOT NUMBER                      73211660
296      08 B009                1166           L     ARL,MDR,MR     (ARL)=NO.OF SLOTS                          73211670
297      50 B150                1167           S     NULL,MDR,ONE,CO TEST NUMBER USED TALLY                    73211680
298      E2 0282                1168           BT    C,LSTOUF       LIST EMPTY, EXIT                           73211690
299      5F B136                1169           S     MDR,MDR,ONE,F+MW2 NEW TALLY, SET CC                       73211700
29A      43 8201                1170           A     MR1,NULL,ARL,D2 (MR1)=NO OF SLOTS IN LIST                 73211710
29B      00 8010                1171           L     NULL,NULL      VECTOR THROUGH DROM2                       73211720
                                1172  *                                                                          73211730
29C      08 8010                1173  RTI.D2   L     NULL,NULL,MR   FETCH CURRENT TOP                          73211740
29D      00 B202                1174           L     MR2,MDR,SL     (MR2)=2X CURRENT TOP                       73211750
29E      4E B116                1175           A     MDR,YDR,ONE,MW BUMP CURRENT TOP                           73211760
29F      50 B250                1176           S     NULL,MDR,ARL,CO COMPARE TO MAX SLOT                       73211770
2A0      E2 02A2                1177           BT    C,*+2          SKIP IF NO WRAP                            73211780
2A1      0E 8016                1178           L     MDR,NULL,MW    LIST WRAP, CURRENT TOP =0                  73211790
2A2      40 BB17                1179           A     MAR,MAR,TWO    POINT TO NEXT BOTTOM                       73211800
2A3      F0 02AB                1180           B     RTBL2          SKIP TO COMMON ROUTINE                     73211810
                                1181  *                                                                          73211820
                                1182  *                                                                          73211830
2A4      40 BB17                1183  RBI.D2   A     MAR,MAR,TWO    (MAR)=ADRS OF NEXT BOTTOM                  73211840
2A5      08 8010                1184           L     NULL,NULL,MR   FETCH IT                                   73211850
2A6      50 B143                1185           S     MR3,MDR,ONE,CO COMPARE TO ZERO                            73211860
2A7      F2 02A9                1186           BF    C,*+2          SKIP IF NO WRAP                            73211870
2A8      50 0903                1187           S     MR3,MR1,ONE    (MR3)=MAX SLOT                             73211880
2A9      0E 1816                1188           L     MDR,MR3,MW     NEW NEXT BOTTOM POINTER                    73211890
2AA      00 1A02                1189           L     MR2,MR3,SL     (MR2)=2X SLOT NUMBER                       73211900
                                1190  *                                                                          73211910
2AB      00 120B                1191  RTBL2    L     AR,MR2,SL      (AR)=4X SLOT NUMBER                        73211920
2AC      40 BB17                1192           A     MAR,MAR,TWO    (MAR)=ADRS OF SLOT 0                       73211930
2AD      40 BE17                1193           A     MAR,MAR,AR     (MAR)=ADRS OF SLOT N                       73211940
2AE      09 8050                1194           L     NULL,NULL,CO+MR2 FETCH ELEMENT 0:15                       73211950
2AF      08 B018                1195           L     YDH,MDR,MR     LOAD IT, FETCH ELEMENT 16:31               73211960
2B0      00 B019                1196  RTBL3    L     YDL,MDR        LOAD IT                                    73211970
2B1      F0 044B                1197           B     FETCHJ         EXIT (P,43)                                73211980
                                1198  *                                                                          73211990
2B2      80 400F                1199  LSTOUF   LI    FLR,4                                                     73212000
2B3      F0 044B                1200           B     FETCHJ         EXIT (P,43)
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                02B4                1202  BTC       EQU   *                 BRANCH ON TRUE CONDITION      * 42 *  73212020
                                    1203  *                                                                       73212030
2B4       F0 22CE                   1204            BF    MSK1,NOBR         NO BRANCH IF FALSE                    73212040
2B5       60 A417                   1205            CA    MAR,LOC,MDR       (MAR)=BRANCH ADDRESS                  73212050
2B6       04 B814                   1206            L     LOC,MAR,IR        (LOC)=(MAR); FETCH INSTR.             73212060
2B7       00 8010                   1207            L     NULL,NULL         NOP                                   73212070
                                    1208  *                                                                       73212080
                02B8                1209  BTCR      EQU   *                 BRANCH TRUE COND. REGISTER    * 02 *  73212090
                                    1210  *                                                                       73212100
2B8       F0 2200                   1211            BF    MSK1,FETCH        NO BRANCH IF FALSE                    73212110
2B9       40 8614                   1212            A     LOC,NULL,AR       (LOC)=(MAR)=BRANCH ADRS               73212120
2BA       04 8010                   1213            L     NULL,NULL,IR      FETCH INSTRUCTION                     73212130
2BB       00 8010                   1214            L     NULL,NULL         NOP                                   73212140
                                    1215  *                                                                       73212150
                02BC                1216  BTBS      EQU   *                 BRANCH TRUE BACKWARD SHORT    * 20 *  73212160
                02BC                1217  BTFS      EQU   *                 BRANCH TRUE FORWARD SHORT     * 21 *  73212170
                                    1218  *                                                                       73212180
2BC       F0 2200                   1219            BF    MSK1,FETCH        NO BRANCH IF FALSE                    73212190
2BD       53 A314                   1220            S     LOC,LOC,TWO,D2    DECREMENT LOC & MAR BY 2              73212200
2BE       00 620B                   1221            L     AR,YSI,SL         2X N-FIELD;GO TO BBS                  73212210
                                    1222  *                                                                       73212220
                02BF                1223  BFC       EQU   *                 BRANCH ON FALSE CONDITION     * 43 *  73212230
                                    1224  *                                                                       73212240
2BF       E0 22CE                   1225            BT    MSK1,NOBR         NO BRANCH IF TRUE                     73212250
2C0       60 A417                   1226            CA    MAR,LOC,MDR       (MAR)=BRANCH ADDRESS                  73212260
2C1       04 B814                   1227            L     LOC,MAR,IR        (LOC)=(MAR); FETCH INSTR.             73212270
2C2       00 8010                   1228            L     NULL,NULL         NOP                                   73212280
                                    1229  *                                                                       73212290
                02C3                1230  BFCR      EQU   *                 BRANCH FALSE COND. REGISTER   * 03 *  73212300
                                    1231  *                                                                       73212310
2C3       E0 2200                   1232            BT    MSK1,FETCH        NO BRANCH IF TRUE                     73212320
2C4       40 8614                   1233            A     LOC,NULL,AR       (LOC)=(MAR)=BRANCH ADRS               73212330
2C5       04 8010                   1234            L     NULL,NULL,IR      FETCH INSTRUCTION                     73212340
2C6       00 8010                   1235            L     NULL,NULL         NOP                                   73212350
                                    1236  *                                                                       73212360
                02C7                1237  BFBS      EQU   *                 BRANCH FALSE BACKWARD SHORT   * 22 *  73212370
                02C7                1238  BFFS      EQU   *                 BRANCH FALSE FORWARD SHORT    * 23 *  73212380
                                    1239  *                                                                       73212390
2C7       E0 2200                   1240            BT    MSK1,FETCH        NO BRANCH IF TRUE                     73212400
2C8       53 A314                   1241            S     LOC,LOC,TWO,D2    DECREMENT LOC & MAR BY 2              73212410
2C9       00 620B                   1242            L     AR,YSI,SL         2X N-FIELD; GO TO BBS                 73212420
                                    1243  *                                                                       73212430
2CA       50 A614                   1244  BBS       S     LOC,LOC,AR        (LOC)=(MAR)=BRANCH ADDRESS            73212440
2CB       04 8010                   1245            L     NULL,NULL,IR      FETCH NEXT INSTRUCTION                73212450
                                    1246  *                                                                       73212460
2CC       00 A017                   1247  NBR       L     MAR,LOC           (MAR)=(LOC)                           73212470
2CD       04 8010                   1248            L     NULL,NULL,IR      FETCH NEXT INSTR                      73212480
                                    1249  *                                                                       73212490
2CE       00 B10B                   1250  NOBR      L     AR,MDR,LEN        (AR)=2 IF RX3                         73212500
                                    1251  *                                 AR=0 IF RX1 OR RX2                    73212510
2CF       40 A614                   1252  BFS       A     LOC,LOC,AR        (LOC)=(MAR)=BRANCH ADDRESS            73212520
2D0       04 8010                   1253  FETCH     L     NULL,NULL,IR      FETCH NEXT INSTRUCTION                73212530
2D1       00 8010                   1254            L     NULL,NULL         NOP                                   73212540
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                02D2                1256  BAL     EQU   *                 BRANCH AND LINK                 * 41 *  73212560
                                    1257  *                                                                     73212570
2D2         60 A417                 1258        CA    MAR,LOC,MDR       (MAR)=BRANCH ADDRESS                  73212580
2D3         00 8818                 1259        L     YDH,LOCH                                                73212590
2D4         04 A019                 1260        L     YDL,LOC,IR        R1=LINK REGISTER=(LOC)                73212600
2D5         00 B814                 1261        L     LOC,MAR           (LOC)=(MAR)                           73212610
                                    1262  *                                                                     73212620
                02D6                1263  BALR    EQU   *                 BRANCH AND LINK REGISTER        * 01 *  73212630
                                    1264  *                                                                     73212640
2D6         40 8617                 1265        A     MAR,NULL,AR       (MAR)=BRANCH ADDRESS                  73212650
2D7         00 8818                 1266        L     YDH,LOCH                                                73212660
2D8         04 A019                 1267        L     YDL,LOC,IR        R1=LINK REGISTER=(LOC)                73212670
2D9         00 B814                 1268        L     LOC,MAR           (LOC)=(MAR)                           73212680
                                    1269  *                                                                     73212690
                02DA                1270  BXH     EQU   *                 BRANCH ON INDEX HIGH            * C0 *  73212700
                02DA                1271  BXLE    EQU   *                 BRANCH INDEX LOW OR EQUAL       * C1 *  73212710
                                    1272  *                                                                     73212720
2DA         60 A417                 1273        CA    MAR,LOC,MDR       (MAR)=BRANCH ADDRESS                  73212730
2DB         00 D009                 1274        L     ARL,YDLP1         (ARL)=R1(16:31)                       73212740
2DC         40 690C                 1275        A     YSI,YDI,ONE                                             73212750
2DD         00 C00A                 1276        L     ARH,YDH           (ARH)=R1)1(0:15)                      73212760
2DE         40 DA49                 1277        A     ARL,YDLM1,ARL,CO  (ARL)=SUM R1 & R1+1                   73212770
2DF         40 8219                 1278        A     YDL,NULL,ARL                                            73212780
2E0         40 C798                 1279        A     YDH,YDH,ARH,CI    (R1)=(R1)+(R1+1)                      73212790
2E1         00 C00A                 1280        L     ARH,YDH                                                 73212800
2E2         53 EA50                 1281        S     NULL,YSL,ARL,CO+D2  INDEX-INCREMENT                     73212810
2E3         50 E7D0                 1282        S     NULL,YSH,ARH,CI+C0  VECTOR THROUGH DROMO                73212820
                                    1283  *                                                                     73212830
2E4         F2 02CC                 1284  BXH.D2  BF    C,NBR             NO BRANCH IF NOT LESS (P.30)          73212840
2E5         04 B814                 1285        L     LOC,MAR,IR        (LOC)=(MAR); FETCH INSTR.             73212850
2E6         00 8010                 1286        L     NULL,NULL         NOP                                   73212860
                                    1287  *                                                                     73212870
2E7         E2 02CC                 1288  BXLE.D2 BT    C,NBR             NO BRANCH IF LESS (P.30)              73212880
2E8         04 B814                 1289        L     LOC,MAR,IR        (LOC)=(MAR);FETCH INSTR               73212890
2E9         00 8010                 1290        L     NULL,NULL         NOP                                   73212900
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                02EA          1292  AR      EQU   *                    ADD REGISTER                  * 0A *  73212920
                02EA          1293  AH      EQU   *                    ADD HALFWORD                  * 4A *  73212930
                02EA          1294  A       EQU   *                    ADD                           * 5A *  73212940
                02EA          1295  AHI     EQU   *                    ADD HALFWORD IMMEDIATE        * CA *  73212950
                02EA          1296  AI      EQU   *                    ADD IMMEDIATE                 * FA *  73212960
                              1297  *                                                                       73212970
2EA       47 CA79             1298        A     YDL,YDL,ARL,CO+F+IRJ R1 + 2ND OP TO R1                    73212980
2EB       40 C7F8             1299        A     YDH,YDH,ARH,CI+CO+F                                       73212990
                              1300  *                                                                       73213000
                02EC          1301  AIS     EQU   *                    ADD IMMEDIATE SHORT           * 26 *  73213010
                              1302  *                                                                       73213020
2EC       00 6009             1303        L     ARL,YSI              (ARL)=N FIELD OF INSTR.              73213030
2ED       47 CA79             1304        A     YDL,YDL,ARL,CO+F+IRJ R1 + N FIELD TO R1                   73213040
2EE       40 C0F8             1305        A     YDH,YDH,NULL,CI+CO+F                                      73213050
                              1306  *                                                                       73213060
                02EF          1307  AM      EQU   *                    ADD TO MEMORY                 * 51 *  73213070
                              1308  *                                                                       73213080
2EF       60 A417             1309        CA    MAR,LOC,MDR          (MAR)=2ND OP ADDRESS                 73213090
2F0       09 8010             1310        L     NULL,NULL,MR2        FETCH MS 16 BITS; BUMP MAR           73213100
2F1       08 B00A             1311        L     ARH,MDR,MR           (ARH)=MS 16 BITS                     73213110
2F2       4E CC76             1312        A     MDR,YDL,MDR,CO+F+MW  ADD LS 16 BITS & STORE               73213120
2F3       50 BB17             1313        S     MAR,MAR,TWO          POINT BACK AT MS 16 BITS             73213130
2F4       4E C7F6             1314        A     MDR,YDH,ARH,CI+CO+F+MW SUM AND STORE                      73213140
2F5       F0 044B             1315        B     FETCHJ               EXIT (P,43)                          73213150
                              1316  *                                                                       73213160
                02F6          1317  AHM     EQU   *                    ADD HALFWORD TO MEMORY        * 61 *  73213170
                              1318  *                                                                       73213180
2F6       60 A417             1319        CA    MAR,LOC,MDR          (MAR)=2ND OP ADDRESS                 73213190
2F7       08 8010             1320        L     NULL,NULL,MR         FETCH 2ND OPERAND                    73213200
2F8       4E CC76             1321        A     MDR,YDL,MDR,MW+CO+F  ADD 1ST OP & STORE RESULT            73213210
2F9       F0 044B             1322        B     FETCHJ               EXIT (P,43)                          73213220
                              1323  *                                                                       73213230
                02FA          1324  SR      EQU   *                    SUBTRACT REGISTER             * 0B *  73213240
                02FA          1325  SH      EQU   *                    SUBTRACT HALFWORD             * 4B *  73213250
                02FA          1326  S       EQU   *                    SUBTRACT                      * 5B *  73213260
                02FA          1327  SHI     EQU   *                    SUBTRACT HALFWORD IMMEDIATE   * CB *  73213270
                02FA          1328  SI      EQU   *                    SUBTRACT IMMEDIATE            * FB *  73213280
                              1329  *                                                                       73213290
2FA       57 CA79             1330        S     YDL,YDL,ARL,CO+F+IRJ R1 MINUS 2ND OP TO R1                73213300
2FB       50 C7F8             1331        S     YDH,YDH,ARH,CI+CO+F                                       73213310
                              1332  *                                                                       73213320
                02FC          1333  SIS     EQU   *                    SUBTRACT IMMEDIATE SHORT      * 27 *  73213330
                              1334  *                                                                       73213340
2FC       00 6009             1335        L     ARL,YSI              (ARL)=NFIELD OF INSTR.               73213350
2FD       57 CA79             1336        S     YDL,YDL,ARL,CO+F+IRJ R1 MINUS N FIELD TO R1               73213360
2FE       50 C0F8             1337        S     YDH,YDH,NULL,CI+CO+F                                      73213370
                              1338  *                                                                       73213380
2FF       00 8010             1339        L     NULL,NULL            FILLER (NOT USED)                    73213390
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                0300                1341  CR      EQU   *                        COMPARE REGISTER                * 09 *  73213410
                0300                1342  CH      EQU   *                        COMPARE HALFWORD                * 49 *  73213420
                0300                1343  C       EQU   *                        COMPARE                         * 59 *  73213430
                0300                1344  CHI     EQU   *                        COMPARE HALFWORD IMMEDIATE      * C9 *  73213440
                0300                1345  CI      EQU   *                        COMPARE IMMEDIATE               * F9 *  73213450
                                    1346  *                                                                             73213460
300       30 C730                   1347        X       NULL,YDH,ARH,F         COMPARE SIGNS                           73213470
301       F0 4211                   1348        BF      L,CR1                  BRANCH IF ALIKE (P.24)                  73213480
302       00 C250                   1349        L       NULL,YDH,SL+CO         SIGNS DIFFER. SET CARRY                 73213490
303       07 C830                   1350        L       NULL,YDL,F+IRJ         EQUAL TO SIGN OF FIRST                  73213500
304       00 C030                   1351        L       NULL,YDH,F             OPERAND THEN SET G&L                    73213510
                                    1352  *                                                                             73213520
                0305                1353  MR      EQU   *                        MULTIPLY REGISTER               * 1C *  73213530
                0305                1354  M       EQU   *                        MULTIPLY                        * 5C *  73213540
                                    1355  *                                                                             73213550
305       00 D010                   1356        L       NULL,YDLP1             INCREMENT R1 FIELD                      73213560
306       70 00A0                   1357        C       TABT                   ENABLE ABORT                            73213570
307       30 C700                   1358        X       MR0,YDH,ARH            FORM RESULT SIGN                        73213580
308       40 8224                   1359        A       MR4,NULL,ARL,F         (MR3,MR4)=SECOND OPERAND                73213590
309       40 8723                   1360        A       MR3,NULL,ARH,F                                                 73213600
30A       F0 430D                   1361        BF      L,M1                                                           73213610
30B       50 8244                   1362        S       MR4,NULL,ARL,CO        2'S COMP 2ND OP IF MINUS                73213620
30C       50 8783                   1363        S       MR3,NULL,ARH,CI                                                73213630
30D       00 C822                   1364  M1    L       MR2,YDL,F              (MR1,MR2)=FIRST OPERAND                 73213640
30E       00 C021                   1365        L       MR1,YDH,F                                                      73213650
30F       F0 4314                   1366        BF      L,M2                   BRANCH IF POSITIVE                      73213660
310       00 C809                   1367        L       ARL,YDL                                                        73213670
311       00 C00A                   1368        L       ARH,YDH                                                        73213680
312       50 8242                   1369        S       MR2,NULL,ARL,CO        2'S COMP 1ST OP IF MINUS                73213690
313       50 87C1                   1370        S       MR1,NULL,ARH,CI+CO                                             73213700
                                    1371  *                                    (MR1,MR2)=MULTIPLICAND: A               73213710
                                    1372  *                                    (MR3,MR4)=MULTIPLIER  : B               73213720
314       00 1012                   1373  M2    L       SRL,MR2                (SRL)=A 16:31                           73213730
315       00 2016                   1374        L       MDR,MR4                (MDR)=B 16:31                           73213740
316       00 B249                   1375        L       ARL,MDR,SL+CO          (ARL)=2X B 16:31                        73213750
317       70 C400                   1376        C       UMPY                   FORM FIRST PARTIAL PRODUCT              73213760
318       00 9006                   1377        L       MR6,SRL                SAVE IN (MR5,MR6)                       73213770
319       00 9805                   1378        L       MR5,SRH                                                        73213780
31A       00 0812                   1379        L       SRL,MR1                (SRL)=A 0:15                            73213790
31B       00 2016                   1380        L       MDR,MR4                (MDR)=B 16:31                           73213800
31C       00 B249                   1381        L       ARL,MDR,SL+CO          (ARL)=2X B 16:31                        73213810
31D       70 C400                   1382        C       UMPY                   FORM SECOND PARTIAL PRODUCT             73213820
31E       00 9009                   1383        L       ARL,SRL                                                        73213830
31F       40 2A45                   1384        A       MR5,MR5,ARL,CO         ACCUMULATE PARTIAL PRODUCTS             73213840
320       40 9884                   1385        A       MR4,SRH,NULL,CI        (MR4,MR5,MR6)=RESULT                    73213850
321       00 1012                   1386        L       SRL,MR2                (SRL)=A 16:31                           73213860
322       00 1816                   1387        L       MDR,MR3                (MDR)=B 0:15                            73213870
323       00 B249                   1388        L       ARL,MDR,SL+CO          (ARL)=2X B 0:15                         73213880
324       70 C400                   1389        C       UMPY                   FORM THIRD PARTIAL PRODUCT              73213890
325       00 9009                   1390        L       ARL,SRL                                                        73213900
326       00 980A                   1391        L       ARH,SRH                                                        73213910
327       00 0812                   1392        L       SRL,MR1                (SRL)=A 0:15                            73213920
328       00 1816                   1393        L       MDR,MR3                (MDR)=B 0:15                            73213930
329       40 2A45                   1394        A       MR5,MR5,ARL,CO         (MR3,MR4,MR5,MR6)=ACCUMULATED           73213940
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FIXED POINT ARITHMETIC INSTRUCTIONS 73212

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32A  40 27C4  1395        A   MR4,MR4,ARH,CI+CO   PARTIAL PRODUCTS                    73213950
32B  40 8083  1396        A   MR3,NULL,NULL,CI                                       73213960
32C  00 B249  1397        L   ARL,MDR,SL+CO       (MDR)=2X B 0:15                    73213970
32D  70 C400  1398        C   MPY                 FINAL PARTIAL PRODUCT              73213980
32E  00 9009  1399        L   ARL,SRL                                                73213990
32F  00 980A  1400        L   ARH,SRH                                                73214000
330  40 2244  1401        A   MR4,MR4,ARL,CO                                         73214010
331  40 1F83  1402        A   MR3,MR3,ARH,CI                                         73214020
                1403  *                                                            73214030
                1404  * (MR3,MR4,MR5,MR6)=UNSIGNED PRODUCT                        73214040
                1405  *                                                            73214050
332  00 0250  1406        L   NULL,MR0,SL+CO      TEST RESULT SIGN                   73214060
333  F2 033C  1407        BF  C,M3                SKIP IF POSITIVE                   73214070
334  00 3009  1408        L   ARL,MR6              ELSE, FORM 2'S COMPLEMENT          73214080
335  50 8246  1409        S   MR6,NULL,ARL,CO     OF 64-BIT RESULT                   73214090
336  00 2809  1410        L   ARL,MR5                                                73214100
337  50 82C5  1411        S   MR5,NULL,ARL,CI+CO                                     73214110
338  00 2009  1412        L   ARL,MR4                                                73214120
339  50 82C4  1413        S   MR4,NULL,ARL,CI+CO                                     73214130
33A  00 1809  1414        L   ARL,MR3                                                73214140
33B  50 8283  1415        S   MR3,NULL,ARL,CI                                        73214150
33C  70 00A0  1416  M3    C   TABT                DISABLE ABORT                      73214160
33D  00 2816  1417        L   YDH,MR5             SET RESULT UP IN R1 & R1+1         73214170
33E  00 3018  1418        L   YDL,MR6                                                73214180
33F  04 1818  1419        L   YDH,MR3,IR          FETCH NEXT INSTRUCTION             73214190
340  00 2019  1420        L   YDL,MR4                                                73214200
                1421  *                                                            73214210
     0341     1422  MHR   EQU *                 MULTIPLY HALFWORD REGISTER  * 0C *  73214220
     0341     1423  MH    EQU *                 MULTIPLY HALFWORD           * 4C *  73214230
                1424  *                                                            73214240
341  00 C812  1425        L   SRL,YDL             (SRL)=R1 16:31                     73214250
342  40 8216  1426        A   MDR,NULL,ARL        (MDR)=16 BIT 2ND OPERAND           73214260
343  00 B249  1427        L   ARL,MDR,SL+CO       (ARL)=2X SECOND OPERAND            73214270
344  70 8400  1428        C   MPY                 SIGNED MULTIPLY                    73214280
345  04 9818  1429        L   YDH,SRH,IR          (R1)=SIGNED PRODUCT                73214290
346  00 9019  1430        L   YDL,SRL                                                73214300
                1431  *                                                            73214310
347  00 8010  1432        L   NULL,NULL           FILLER (NOT USED)                  73214320
348  00 8010  1433        L   NULL,NULL           FILLER (NOT USED)                  73214330
349  00 8010  1434        L   NULL,NULL           FILLER (NOT USED)                  73214340
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                034A                1436  DR        EQU   *                 DIVIDE REIGSTER                 * 10 *  73214360
                034A                1437  D         EQU   *                 DIVIDE                          * 5D *  73214370
                                    1438  *                                                                       73214380
34A     70 00A0                     1439              C     TABT            ENABLE ABORT                            73214390
34A     30 C706                     1440              X     MR6,YDH,ARH     FORM RESULT SIGN                        73214400
34C     00 C250                     1441              L     NULL,YDH,SL+CO                                          73214410
34D     00 32C6                     1442              L     MR6,MR6,SL+CO+CI  MR6 BIT 14=DIVIDEND SIGN              73214420
34E     00 3266                     1443              L     MR6,MR6,SL+CI   MR6 BIT 15=RESULT SIGN                 73214430
34F     40 8230                     1444              A     NULL,NULL,ARL,F                                         73214440
350     40 8730                     1445              A     NULL,NULL,ARH,F TEST DIVISOR                            73214450
351     E0 4355                     1446              BT    L,OKDIV1        OK IF MINUS                             73214460
352     F0 8388                     1447              BF    G,OVDIV1        OVERFLOW IS ZERO (P.36)                 73214470
353     50 8249                     1448              S     ARL,NULL,ARL,CO 2'S COMP IF POSITIVE                    73214480
354     50 873A                     1449              S     ARH,NULL,ARH,CI                                         73214490
355     00 C021                     1450  OKDIV1      L     MR1,YDH,F       (MR1,MR2)=DIVIDEND (P.36)               73214500
356     00 D002                     1451              L     MR2,YDLP1                                               73214510
357     81 F008                     1452              LI    CTR,31          SET COUNTER                             73214520
358     00 C013                     1453              L     SRH,YDH         (SRH,SRL)= (R1+1)                       73214530
359     00 C812                     1454              L     SRL,YDL         BITS 32:63 OF DIVIDEND                  73214540
35A     E0 8363                     1455              BT    G,DF2           BRANCH IF NOT MINUS                     73214550
35B     00 9016                     1456              L     MDR,SRL                                                 73214560
35C     50 8452                     1457              S     SRL,NULL,MDR,CO 2'S COMP 64 BIT DIVIDEND                73214570
35D     00 9816                     1458              L     MDR,SRH                                                 73214580
35E     50 84C3                     1459              S     SRH,NULL,MDR,CI+CO                                      73214590
35F     00 1016                     1460              L     MDR,MR2                                                 73214600
360     50 84C2                     1461              S     MR2,NULL,MDR,CI+CO                                      73214610
361     00 0816                     1462              L     MDR,MR1                                                 73214620
362     50 8481                     1463              S     MR1,NULL,MDR,CI                                         73214630
                                    1464  *                                                                       73214640
                                    1465  * (MR1,MR2,SRH,SRL) = POSITIVE DIVIDEND                                  73214650
                                    1466  * (ARH,ARL) = NEGATIVE DIVISOR                                           73214660
                                    1467  *                                                                       73214670
363     40 1250                     1468  DF2         A     NULL,MR2,ARL,CO TRIAL SUBTRACT                          73214680
364     40 0FD0                     1469              A     NULL,MR1,ARH,CI+CO                                      73214690
365     E2 038A                     1470              BT    C,OVDIV1        OVERFLOW IF GOES FIRST TIME (P.36)      73214700
                                    1471  *                                                                       73214710
366     70 1240                     1472  DFLOOP      C     SL1+CI+CO       SHIFT REMAINDER & QUOTIENT              73214720
367     00 12C2                     1473              L     MR2,MR2,SL+CI+CO QUOTIENT SHIFTS FROM C FLAG            73214730
368     00 0AC1                     1474              L     MR1,MR1,SL+CI+CO INTO SRL BIT 15.                       73214740
369     40 1242                     1475              A     MR2,MR2,ARL,CO  TRIAL SUBTRACT                          73214750
36A     40 0FC1                     1476              A     MR1,MR1,ARH,CI+CO                                       73214760
36B     E2 036E                     1477              BT    C,NRESTO        NO RESTORE IF CARRY                     73214770
36C     50 1242                     1478              S     MR2,MR2,ARL,CO  RESTORE DIVIDEND                        73214780
36D     50 0FC1                     1479              S     MR1,MR1,ARH,CI+CO                                       73214790
36E     FC 8366                     1480  NRESTO      BF    CNTR,DFLOOP     REPEAT 32 TIMES                         73214800
                                    1481  *                                                                       73214810
36F     70 1240                     1482              C     SL1+CI+CO       ADJUST QUOTIENT                         73214820
370     00 9830                     1483              L     NULL,SRH,F      TEST SIGN OF QUOTIENT                   73214830
371     E0 4382                     1484              BT    L,STEST         TEST FOR OVERFLOW IF MINUS (P.36)       73214840
372     00 300F                     1485  DF4         L     FLR,MR6                                                 73214850
373     F0 4378                     1486              BF    L,DF4           QUOTIENT SHOULD BE PLUS (P.36)          73214860
374     00 9016                     1487              L     MDR,SRL                                                 73214870
375     50 8452                     1488              S     SRL,NULL,MDR,CO 2'S COMPLEMENT QUOTIENT                 73214880
376     00 9816                     1489              L     MDR,SRH                                                 73214890
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377  50 8493  1490          S   SRH,NULL,MDR,CI                          73214900
378  F0 837D  1491  DF4     BF  G,DF8      REMAINDER SHOULD BE PLUS      73214910
                 1492  *                  (SIGN OF REMAINDER EQUALS     73214920
                 1493  *                  SIGN OF DIVIDEND)             73214930
379  00 1016  1494          L   MDR,MR2                                   73214940
37A  50 8442  1495          S   MR2,NULL,MDR,CO  2'S COMPLEMENT REMAINDER 73214950
37B  00 0816  1496          L   MDR,MR1                                   73214960
37C  50 8481  1497          S   MR1,NULL,MDR,CI                          73214970
37D  70 00A0  1498  DF8     C   TABT          DISABLE ABORT               73214980
37E  00 9818  1499          L   YDH,SRH       STORE QUOTIENT IN R1        73214990
37F  00 901B  1500          L   YDL,SRL                                   73215000
380  04 0818  1501          L   YDH,MR1,IR    STORE REMAINDER IN R1       73215010
381  00 1019  1502          L   YDL,MR2       FETCH NEXT INSTRUCTION      73215020
                 1503  *                                                 73215030
382  00 300F  1504  STFST   L   FLR,MR6                                   73215040
383  F0 4386  1505          BF  L,OVDIV1      OVERFLOW IF                 73215050
384  88 0609  1506          LI  ARL,'80',CS   (ARL)='A000'                73215060
385  50 9150  1507          S   NULL,SRL,ONE,CO  DO QUOTIENT-'80000001'    73215070
386  50 9AC0  1508          S   NULL,SRH,ARL,CI+CO                        73215080
387  E2 0372  1509          BT  C,DF3         (P.35) OVERFLOW IF MAGNITUDE 73215090
                 1510  *                  OF QUOTIENT NOT LESS          73215100
                 1511  *                  THAN '80000001'               73215110
                 1512  * FIXED-POINT DIVIDE FAULT                       73215120
                 1513  *                                                 73215130
388  70 00A0  1514  OVDIV1  C   TABT          DISABLE ABORT               73215140
389  F0 038F  1515          B   OVDIV         TO COMMON FAULT ROUTINE (P.37) 73215150
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                    038A          1517  DHR     EQU   *                                DIVIDE HALFWORD REGISTER     * 00 *  73215170
                    038A          1518  DH      EQU   *                                DIVIDE HALFWORD              * 40 *  73215180
                                  1519  *                                                                                  73215190
38A       40 8222                 1520        A     MR2,NULL,ARL,F                   (MR2)=DIVISOR                       73215200
38B       70 0020                 1521        C     SUT                                                                  73215210
                                                                                                                         73215220
38C       81 0008                 1522        LI    CTR,16                                                               73215230
38D       E0 43A6                 1523        BT    L,OKDIVH                         NO CHANGE IF NEGATIVE               73215240
38E       E0 8391                 1524        BT    G,COMSOR                         TWO'S COMPLEMENT IF POSITIVE        73215250
                                                                                     FALL THROUGH IF ZERO                73215260
                                  1525  *                                                                                  73215270
                                  1526  *                                                                                  73215280
38F       00 8000                 1527  OVDIV   L     MR0,NULL                                                             73215290
390       F0 005A                 1528        B     AFAULT                           ARITHMETIC FAULT (P.A)              73215300
                                  1529  *                                                                                  73215310
391       50 8202                 1530  COMSOR  S     MR2,NULL,ARL                     2'S COMP DIVISOR                    73215320
392       70 0010                 1531        C     CUT                              UT=DIVISOR SIGN                     73215330
393       00 C812                 1532        L     SRL,YDL                                                              73215340
394       00 C033                 1533        L     SRH,YDH,F                        TEST DIVIDEND                       73215350
395       E0 83AD                 1534        BT    G,DIVOP                          QUOTIENT WILL BE PLUS               73215360
396       00 9009                 1535        L     ARL,SRL                                                              73215370
397       00 980A                 1536        L     ARH,SRH                                                              73215380
396       50 8252                 1537        S     SRL,NULL,ARL,CO                  2'S COMP DIVIDEND                   73215390
399       50 8793                 153A        S     SRH,NULL,ARH,CI                                                      73215400
39A       70 0030                 1539  DIVOM   C     TUT                              UT=RESULT SIGN                      73215410
39B       00 1009                 1540        L     ARL,MR2                                                              73215420
39C       40 9A42                 1541        A     MR2,SRH,ARL,CO                   TRIAL SUBTRACT                      73215430
39D       E2 038F                 1542        BT    C,OVDIV                          FAULT IF GOES FIRST TIME            73215440
39E       70 2200                 1543        C     DIV                              DO DIVIDE                           73215450
39F       00 9009                 1544        L     ARL,SRL                                                              73215460
3A0       50 8232                 1545        S     SRL,NULL,ARL,F                   2'S COMP QUOTIENT                   73215470
3A1       E0 43B3                 1546        BT    L,BCKDIV                         OK IF NEGATIVE                      73215480
3A2       80 000F                 1547  CHOVF   LI    FLR,0                            CLEAR FLAGS                         73215490
3A3       00 9032                 1548        L     SRL,SRL,F                        TEST QUOTIENT                       73215500
3A4       E0 838F                 1549        BT    G,OVDIV                          FAULT IF POSITIVE                   73215510
3A5       F0 03B3                 1550        B     BCKDIV                           OK IF '8000'                        73215520
3A6       00 C832                 1551  OKDIVH  L     SRL,YDL,F                                                            73215530
3A7       00 C033                 1552        L     SRH,YDH,F                        TEST DIVIDEND                       73215540
3A8       E0 839A                 1553        BT    G,DIVOM                          QUOTIENT WILL BE MINUS              73215550
3A9       00 9009                 1554        L     ARL,SRL                                                              73215560
3AA       00 980A                 1555        L     ARH,SRH                                                              73215570
3AB       50 8252                 1556        S     SRL,NULL,ARL,CO                  2'S COMP DIVIDEND                   73215580
3AC       50 87D3                 1557        S     SRH,NULL,ARH,CI+CO                                                   73215590
3AD       00 1009                 1558  DIVOP   L     ARL,MR2                                                              73215600
3AE       40 9A42                 1559        A     MR2,SRH,ARL,CO                   TRIAL SUBTRACT                      73215610
3AF       E2 038F                 1560        BT    C,OVDIV                          FAULT IF GOES FIRST TIME            73215620
3B0       70 2200                 1561        C     DIV                              DO DIVIDE                           73215630
3B1       00 9032                 1562        L     SRL,SRL,F                        TEST QUOTIENT SIGN                  73215640
3B2       E0 438F                 1563        BT    L,OVDIV                          FAULT IF NEGATIVE                   73215650
3B3       FC 23B6                 1564  BCKDIV  BF    UT,EXDIV                         REMAINDER SHOULD BE PLUS            73215660
3B4       00 9809                 1565        L     ARL,SRH                          IF UTILITY IS RESET                 73215670
3B5       50 8293                 1566        S     SRH,NULL,ARL,CI                  2'S COMP REMAINDER                  73215680
3B6       00 9816                 1567  FXDIV   L     MDR,SRH                                                              73215690
3B7       40 8518                 1568        A     YDH,NULL,SIGN                    R1 0:15=SIGN OF REMAINDER           73215700
3B8       00 981A                 1569        L     YDLP1,SRH                        R1 16:31=REMAINDER
3B9       00 9250                 1570        L     NULL,SRL,SL+CO                   CARRY=SIGN OF QUOTIENT
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3BA  04 9019  1571          L   YDL,SRL,IR          R1+1 16:31=QUOTIENT                    73215710
3BB  50 8098  1572          S   YDH,NULL,NULL,CI    R1+1 0:15=QUOTIENT SIGN                73215720
              1573  *                                                                       73215730
              1574  * COMMON DROM 1 ENTRY POINT FOR SLA,SRA                                 73215740
              1575  *                                                                       73215750
3BC  00 CA52  1576  SLRA    L   SRL,YDL,SL+CO       (SRH,SRL)=1ST OP SHIFTED               73215760
3BD  03 C2D3  1577          L   SRH,YDH,SL+CI+CO+D2 LEFT ONCE, CARRY = SIGN                73215770
3BE  40 F409  1578          A   ARL,YSLX,MDR        VECTOR THROUGH DROM2                   73215780
              1579  *                                                                       73215790
     03BF     1580  SLA     EQU *                  SHIFT LEFT ARITHMETIC        * EF *    73215800
              1581  *                                                                       73215810
3BF  00 848A  1582          L   ARH,NULL,SR+CI      SAVE SIGN BIT IN ARH                   73215820
3C0  91 F200  1583          NI  MR0,'1F',ARL        MASK COUNT                             73215830
3C1  00 0448  1584          L   CTR,MR0,SR+CO       COUNT/2, C=1 IF ODD                    73215840
3C2  F2 03C4  1585          BF  C,*+2               SKIP IF EVEN NO. OF SHIFTS             73215850
3C3  70 1040  1586          C   SL1+CO              DO ODD SHIFT AT START                  73215860
3C4  70 0008  1587          C   RPT                 REPEAT NEXT INSTRUCTION                73215870
3C5  70 1440  1588          C   SL2+CO              SHIFT 2 PLACES, ADJUST C               73215880
3C6  70 0800  1589          C   SR1                 COMPENSATE FOR PRE SHIFT               73215890
3C7  07 9039  1590          L   YDL,SRL,F+IRJ       LOAD RESULT, SET G&L                   73215900
3C8  20 9F38  1591          O   YDH,SRH,ARH,F       RESTORE SIGN BIT                       73215910
              1592  *                                                                       73215920
     03C9     1593  SLHA    EQU *                  SHIFT LEFT HW ARITHMETIC     * CF *    73215930
              1594  *                                                                       73215940
3C9  00 CA59  1595          L   YDL,YDL,SL+CO       CAPTURE SIGN BIT                       73215950
3CA  00 84C9  1596          L   ARL,NULL,SR+CI+CO   SAVE IN ARL <0>                        73215960
3CB  70 0008  1597          C   RPT                 REPEAT NEXT INSTRUCTION                73215970
3CC  00 CA59  1598          L   YDL,YDL,SL+CO       SHIFT LS 16 BITS, ADJUST C             73215980
3CD  05 CC19  1599          L   YDL,YDL,SR+IRJH     COMPENSATE PRE-SHIFT                   73215990
3CE  20 CA39  1600          O   YDL,YDL,ARL,F       ADJUST G&L RESTORE SIGN                73216000
              1601  *                                                                       73216010
     03CF     1602  SRA     EQU *                  SHIFT RIGHT ARITHMETIC       * EE *    73216020
              1603  *                                                                       73216030
3CF  91 F216  1604          NI  MDR,'1F',ARL        MASK COUNT                             73216040
3D0  00 B408  1605          L   CTR,MDR,SR          COUNT/2                                73216050
3D1  70 0008  1606          C   RPT                 REPEAT NEXT INSTRUCTION                73216060
3D2  70 0E00  1607          C   SR2+CI              SHIFT RIGHT, PROPOGATE SIGN            73216070
3D3  90 1408  1608          NI  CTR,1,MDR           SEE IF ODD SHIFT REQUIRED              73216080
3D4  70 0008  1609          C   RPT                                                        73216090
3D5  70 0A00  1610          C   SR1+CI              DO ODD SHIFT IF NECESSARY              73216100
3D6  70 0A40  1611          C   SR1+CI+CO           COMPENSATE FOR PRE SHIFT               73216110
3D7  07 9039  1612          L   YDL,SRL,F+IRJ       LOAD RESULT, SET G&L                   73216120
3D8  00 9838  1613          L   YDH,SRH,F                                                  73216130
              1614  *                                                                       73216140
     03D9     1615  SRHA    EQU *                  SHIFT RIGHT HW ARITHMETIC    * CE *    73216150
              1616  *                                                                       73216160
3D9  00 CA59  1617          L   YDL,YDL,SL+CO       MOVE SIGN TO CARRY FLAG                73216170
3DA  70 0008  1618          C   RPT                 REPEAT NEXT INSTRUCTION                73216180
3DB  00 CC99  1619          L   YDL,YDL,SR+CI       SHIFT LS 16 BITS;PROPOGATE SIGN        73216190
3DC  05 CCF9  1620          L   YDL,YDL,SR+CI+CO+F+IRJH  COMPENSATE PRESHIFT              73216200
              1621  *                               ADJUST G&L; SET C                      73216210
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                03DD                1623  CHVR    EQU   *                    CONVERT TO HW VALUE REGISTER * 12 *   73216230
                                    1624  *                                                                        73216240
03DD        00 3812                 1625          L     SRL,PSWL           GET PREVIOUS CONDITION CODE           73216250
03DE        00 E816                 1626          L     MDR,YSL            MDR=R2(16:31)                         73216260
03DF        70 0C00                 1627          C     SR2                                                      73216270
03E0        70 0C40                 1628          C     SR2+CO             CARRY=PREVIOUS CARRY                  73216280
03E1        50 E530                 1629          S     NULL,YSH,SIGN,F    TEST R2(0:15)                         73216290
03E2        40 8518                 1630          A     YDH,NULL,SIGN      R1(0:15)=SIGN OF R2                   73216300
03E3        E0 C3E5                 1631          BT    G+L,CHVR1          SET OVERFLOW IF BITS 0:15             73216310
                                    1632  *                                OF R2 NOT EQUAL TO R2 BIT 16          73216320
03E4        05 E839                 1633          L     YDL,YSL,F+IRJH     R1(16:31)=R2(16:31); FETCH             73216330
                                    1634  *                                NEXT INSTRUCTION & SET CC             73216340
03E5        80 4009                 1635  CHVR1   LI    ARL,4                                                    73216350
03E6        00 8281                 1636          L     MR1,NULL,SL+CI     MR1=PREVIOUS CARRY                    73216360
03E7        00 0C4F                 1637          L     FLR,MR1,SR+CO      CLEAR V,G,L...KEEP CARRY              73216370
03E8        00 E839                 1638          L     YDL,YSL,F          R1<16:31>=R2<16:31>                   73216380
03E9        75 0088                 1639          C     JH+IRJH            SET CONDITION CODE                    73216390
03EA        20 3A07                 1640          O     PSWL,PSWL,ARL      THEN SET V FLAG                       73216400
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STATUS SWITCHING INSTRUCTIONS 73216

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                03EB                1642  LPSW     EQU   *                 LOAD PROGRAM STATUS WORD      * C2 *  73216420
                                    1643  *                                                                     73216430
03EB        60 A417                 1644          CA    MAR,LOC,MDR       (MAR)=2ND OP ADDRESS                73216440
03EC        79 0000                 1645          C     MR2               FETCH HIGH NEW PSW                  73216450
03ED        09 B003                 1646          L     MR3,MDR,MR2       SET ASIDE IN MR3, FETCH LOW         73216460
03EE        09 B002                 1647          L     MR2,MDR,MR2       SET ASIDE IN MR2, FETCH LOC         73216470
03EF        0B 8010                 1648          L     NULL,NULL,XR2     EXTENDED READ FOR 2ND BITS          73216480
03F0        00 1007                 1649          L     PSWL,MR2          LOAD PSW 16:31                      73216490
03F1        00 B014                 1650          L     LOC,MDR           LOAD NEW LOC                        73216500
03F2        F0 03F8                 1651          B     TQWAIT            GO TEST QUEUE AND WAIT BITS         73216510
                                    1652  *                                                                     73216520
                03F3                1653  LPSWR    EQU   *                 LOAD PSW REGISTER             * 18 *  73216530
                                    1654  *                                                                     73216540
03F3        40 610C                 1655          A     YSI,YSI,ONE       POINT TO R2+1                       73216550
03F4        00 E814                 1656  LPSWR1  L     LOC,YSL           LOAD LOC                            73216560
03F5        50 610C                 1657          S     YSI,YSI,ONE       RESTORE R2 FIELD                    73216570
03F6        00 E003                 1658  EPSR1   L     MR3,YSH           (MR3)=NEW PSW 0:15                  73216580
03F7        00 E807                 1659          L     PSWL,YSL          LOAD PSW 16:31                      73216590
03F8        70 0088                 1660  TQWAIT  C     JH                PROPOGATE FLR TO CC                 73216600
03F9        E4 80E4                 1661          BT    QUE,QUEINT        CHECK SYSTEM QUEUE IF ENABLED (P.13)73216610
03FA        00 A017                 1662  TWAIT2  L     MAR,LOC           (MAR)=(LOC)                         73216620
03FB        00 180E                 1663          L     PSWH,MR3          LOAD PSW 0:15                       73216630
03FC        E0 102F                 1664          BT    WAIT,WAIT         WAIT IF PSW 16 SET (P.4)            73216640
03FD        04 8010                 1665          L     NULL,NULL,1R      ELSE, FETCH NEXT INSTR.             73216650
03FE        00 8010                 1666          L     NULL,NULL         NOP                                 73216660
                                    1667  *                                                                     73216670
                                    1668  *                                                                     73216680
                                    1669  *                               IF PRIVILEGED INSTR & PROTECT       73216690
03FF        F0 0003                 1670          B     ILLEG             MODE, GO TO ILLEGAL (P.3)           73216700
                                    1671  *                                                                     73216710
                0400                1672  EPSR     EQU   *                 EXCHANGE PSW REGISTER         * 95 *  73216720
                                    1673  *                                                                     73216730
400         00 7018                 1674          L     YDH,PSWH          (R1)=OLD PSW                        73216740
401         00 3819                 1675          L     YDL,PSWL                                              73216750
402         F0 03F6                 1676          B     EPSR1             GO TO COMMON ROUTINE                73216760
                                    1677  *                                                                     73216770
                0403                1678  SINT     EQU   *                 SIMULATE INTERRUPT            * E2 *  73216780
                                    1679  *                                                                     73216790
403         80 360A                 1680          LI    ARH,'03',CS       (ARH)='0300'                        73216800
404         AF F701                 1681          OI    MR1,'FF',ARH      (MR1)='03FF'                        73216810
405         10 0A01                 1682          N     MR1,MR1,ARL       MASK 10 BIT DEVICE NO.              73216820
406         F0 0047                 1683          B     AUTOIO1           AUTOMATIC I/O SERVICE (P.5)         73216830
                                    1684  *                                                                     73216840
                0407                1685  SVC      EQU   *                 SUPERVISOR CALL               * E1 *  73216850
                                    1686  *                                                                     73216860
407         60 A417                 1687          CA    MAR,LOC,MDR       (MAR)=2ND OP ADDRESS                73216870
408         03 B80B                 1688          L     AR,MAR,D2         (AR)=(MAR)+ VECTOR THROUGH          73216880
                                    1689  *                               DROM2 TO CLEAR MDR 12:15            73216890
409         89 8017                 1690  SVC.02  LI    MAR,'98'                                              73216900
40A         0D 3802                 1691          L     MR2,PSWL,MRD2     SAVE PSW 16:31                      73216910
40B         00 8007                 1692          L     PSWL,NULL                                             73216920
40C         80 E00C                 1693          LI    YSI,14                                                73216930
40D         00 701C                 1694          L     YSH,PSWH          REGISTER 14 = OLD PSW               73216940
40E         00 101D                 1695          L     YSL,MR2                                               73216950
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STATUS SWITCHING INSTRUCTIONS 73216

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40F  0D B00E  1696  L   PSWH,MDR,MRD2   LOAD NEW PSW 0:15          73216960
410  80 F00C  1697  LI  YSI,15                                    73216970
411  00 881C  1698  L   YSH,LOCH        REGISTER 15 = OLD LOC     73216980
412  00 A01D  1699  L   YSL,LOC                                   73216990
413  80 D00C  1700  LI  YSI,13                                    73217000
414  40 871C  1701  A   YSH,NULL,ARH    REGISTER 13=2ND OP ADDRESS 73217010
415  40 821D  1702  A   YSL,NULL,ARL                              73217020
416  00 B007  1703  L   PSWL,MDR        LOAD NEW PSW 16:31        73217030
417  00 6A16  1704  L   MDR,YDI,SL      2X R1 FIELD TO MDR        73217040
418  40 BC17  1705  A   MAR,MAR,MDR                              73217050
419  0A 8010  1706  L   NULL,NULL,MRD   FETCH ONE OF 16 LOC VALUES 73217060
41A  00 B014  1707  L   LOC,MDR        LOAD NEW LOC (16 BITS ONLY) 73217070
41B  05 8010  1708  L   NULL,NULL,IRJH  START INSTRUCTION READ    73217080
41C  00 8010  1709  L   NULL,NULL      NOP                       73217090
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                 041D                1711  SS      EQU   *                 SENSE STATUS                    * DD *   73217110
                                     1712  *                                                                      73217120
41D        60 A417                   1713          CA    MAR,LOC,MDR       (MAR)=2ND OP ADDRESS                 73217130
41E        08 C835                   1714          L     IO,YDL,ADRS+MR    ADDRESS THE DEVICE                   73217140
41F        00 AED6                   1715          L     MDR,IO,STAT+CS    INPUT STATUS                         73217150
420        0E B60F                   1716          L     FLR,MDR,CS+MW     LS 4 BITS TO FLR                     73217160
421        F0 044B                   1717          B     FETCHJ            EXIT (P,43)                          73217170
                                     1718  *                                                                      73217180
                 0422                1719  SSR     EQU   *                 SENSE STATUS REGISTER           * 9C *   73217190
                                     1720  *                                                                      73217200
422        00 C835                   1721          L     IO,YDL,ADRS       ADDRESS THE DEVICE                   73217210
423        00 A8DD                   1722          L     YSL,IO,STAT       INPUT STATUS                         73217220
424        00 E80F                   1723          L     FLR,YSL           LS 4 STATUS BITS TO FLR              73217230
425        F0 0434                   1724          B     RDR1                                                   73217240
                                     1725  *                                                                      73217250
                 0426                1726  OC      EQU   *                 OUTPUT COMMAND                  * DE *   73217260
                                     1727  *                                                                      73217270
426        60 A417                   1728          CA    MAR,LOC,MDR       (MAR)=2ND OP ADDRESS                 73217280
427        08 C835                   1729          L     IO,YDL,ADRS+MR    ADDRESS THE DEVICE                   73217290
428        00 B675                   1730          L     IO,MDR,CS+OC      OUTPUT COMMAND                       73217300
429        F0 044B                   1731          B     FETCHJ            EXIT (P,43)                          73217310
                                     1732  *                                                                      73217320
                 042A                1733  OCR     EQU   *                 OUTPUT COMMAND REGISTER         * 9E *   73217330
                                     1734  *                                                                      73217340
42A        00 C835                   1735          L     IO,YDL,ADRS       ADDRESS THE DEVICE                   73217350
42B        07 E875                   1736          L     IO,YSL,OC+IRJ     OUTPUT COMMAND                       73217360
42C        00 8010                   1737          L     NULL,NULL         NOP                                  73217370
                                     1738  *                                                                      73217380
                 042D                1739  RD      EQU   *                 READ DATA                       * D8 *   73217390
                                     1740  *                                                                      73217400
42D        60 A417                   1741          CA    MAR,LOC,MDR       (MAR)=2ND OP ADDRESS                 73217410
42E        08 8010                   1742          L     NULL,NULL,MR                                           73217420
42F        00 C835                   1743          L     IO,YDL,ADRS       ADDRESS THE DEVICE                   73217430
430        0E AEB6                   1744          L     MDR,IO,DR+CS+MW   INPUT A BYTE & STORE               73217440
431        F0 044B                   1745          B     FETCHJ            EXIT (P,43)                          73217450
                                     1746  *                                                                      73217460
                 0432                1747  RDR     EQU   *                 READ DATA REGISTER              * 98 *   73217470
                                     1748  *                                                                      73217480
432        00 C835                   1749          L     IO,YDL,ADRS       ADDRESS THE DEVICE                   73217490
433        00 A8BD                   1750          L     YSL,IO,DR         READ A BYTE                          73217500
434        07 801C                   1751  RDR1    L     YSH,NULL,IRJ      CLEAR R1 0:15                        73217510
435        00 8010                   1752          L     NULL,NULL         NOP                                  73217520
                                     1753  *                                                                      73217530
                 0436                1754  RH      EQU   *                 READ HALFWORD                   * D9 *   73217540
                                     1755  *                                                                      73217550
436        60 A417                   1756          CA    MAR,LOC,MDR       (MAR)=2ND OP ADDRESS                 73217560
437        03 C835                   1757          L     IO,YDL,ADRS+D2    ADDRESS THE DEVICE                   73217570
438        00 8010                   1758          L     NULL,NULL         GO TO RHH IF HW=1                    73217580
                                     1759  *                               GO TO RHB IF HW=0                    73217590
                                     1760  *                                                                      73217600
439        0E A8B6                   1761  RHH     L     MDR,IO,DR+MW      INPUT HALFWORD AND STORE             73217610
43A        F0 044B                   1762          B     FETCHJ            EXIT (P,43)                          73217620
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43B     00 AEA1         1764    RHR     L       MR1,IO,DR+CS    INPUT HIGH BYTE                                     73217650
43C     00 A8A9         1765            L       ARL,IO,DR       INPUT LOW BYTE
43D     2E 0A16         1766            O       MDR,MR1,ARL,MW  COMBINE AND STORE                                   73217660
43E     F0 044B         1767            B       FETCHJ                                                              73217670
                        1768    *                                                                                   73217680
        043F            1769    RHR     EQU     *               READ HALFWORD REGISTER          * 99 *              73217690
                        1770    *                                                                                   73217700
43F     03 C835         1771            L       IO,YDL,ADRS+D2  ADDRESS THE DEVICE                                  73217710
440     00 801C         1772            L       YSH,NULL        CLEAR HIGH R2.                                      73217720
                        1773    *               GO TO RHRH IF HW=1                                                  73217730
                        1774    *               GO TO RHRB IF HW=0                                                  73217740
                        1775    *                                                                                   73217750
441     07 A8BD         1776    RHRH    L       YSL,IO,DR+IRJ   INPUT HALFWORD                                     73217760
442     00 8010         1777            L       NULL,NULL       NOP                                                 73217770
                        1778    *                                                                                   73217780
443     00 AEBD         1779    RHRB    L       YSL,IO,DR+CS    INPUT HIGH BYTE                                     73217790
444     00 A8A9         1780            L       ARL,IO,DR       INPUT LOW BYTE                                      73217800
445     27 EA1D         1781            O       YSL,YSL,ARL,IRJ COMBINE                                             73217810
446     00 8010         1782            L       NULL,NULL       NOP                                                 73217820
                        1783    *                                                                                   73217830
        0447            1784    WD      EQU     *               WRITE DATA                      * DA *              73217840
                        1785    *                                                                                   73217850
447     60 A417         1786            CA      MAR,LOC,MDR     (MAR)=2ND OP ADDRESS                                73217860
448     08 8010         1787            L       NULL,NULL,MR                                                        73217870
449     00 C835         1788            L       IO,YDL,ADRS     ADDRESS THE DEVICE                                  73217880
44A     00 B655         1789            L       IO,MDR,DA+CS    OUTPUT DATA                                         73217890
                        1790    *                                                                                   73217900
44B     00 A017         1791    FETCHJ  L       MAR,LOC         (MAR)=(LOC)                                         73217910
44C     07 8010         1792    INSTRJ  L       NULL,NULL,IRJ   FETCH NEXT INSTRUCTION                              73217920
44D     00 8010         1793            L       NULL,NULL       NOP                                                 73217930
                        1794    *                                                                                   73217940
        044E            1795    WDR     EQU     *               WRITE DATA REGISTER             * 9A *              73217950
                        1796    *                                                                                   73217960
44E     00 C835         1797            L       IO,YDL,ADRS     ADDRESS THE DEVICE                                  73217970
44F     07 E855         1798            L       IO,YSL,DA+IRJ   OUTPUT DATA                                        73217980
450     00 8010         1799            L       NULL,NULL       NOP                                                 73217990
                        1800    *                                                                                   73218000
        0451            1801    WH      EQU     *               WRITE HALFWORD                  * D8 *              73218010
                        1802    *                                                                                   73218020
451     60 A417         1803            CA      MAR,LOC,MDR     (MAR)=2ND OP ADDRESS                                73218030
452     08 C835         1804            L       IO,YDL,ADRS+MR  ADDRESS THE DEVICE                                  73218040
453     03 8010         1805            L       NULL,NULL,D2    GO TO WHH IF HW=1                                   73218050
454     00 A017         1806            L       MAR,LOC         GO TO WHB IF HW=0                                   73218060
                        1807    *                                                                                   73218070
455     07 B055         1808    WHH     L       IO,MDR,DA+IRJ   OUTPUT HALFWORD                                    73218080
456     00 8010         1809            L       NULL,NULL       NOP                                                 73218090
                        1810    *                                                                                   73218100
457     00 B655         1811    WHB     L       IO,MDR,DA+CS    OUTPUT HIGH BYTE                                    73218110
458     F0 0455         1812            B       WHH             GO OUTPUT LOW BYTE                                  73218120
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                0459                1814  WHR     EQU   *                       WRITE HALFWORD REGISTER     * 98 *  73218140
                                    1815  *                                                                         73218150
459       03 C835                   1816        L     IO,YDL,ADRS+D2          ADDRESS THE DEVICE                  73218160
45A       00 E816                   1817        L     MDR,YSL                 GO TO WHH IF HW=1 (P.43)            73218170
                                    1818  *                                   GO TO WHB IF HW=0 (P.43)            73218180
                                    1819  *                                   (MDR)=HALFWORD                      73218190
                                    1820  *                                                                         73218200
                045B                1821  WB      EQU   *                       WRITE BLOCK                 * 06 *  73218210
                045B                1822  RB      EQU   *                       * D7 *                              73218220
                                    1823  *                                                                         73218230
45B       60 A417                   1824  WBRB    CA    MAR,LOC,MDR             (MAR)=2ND OP ADDRESS                73218240
45C       09 8010                   1825        L     NULL,NULL,MR2           FETCH START ADDRESS                 73218250
45D       0B C835                   1826        L     IO,YDL,ADRS+XR2         ADDRESS THE DEVICE                  73218260
45E       09 B00B                   1827        L     AR,MDR,MR2              (AR)=START ADDRESS                  73218270
45F       08 B000                   1828        L     MR0,MDR,MR              (MR0)=HIGH END ADDRESS              73218280
460       40 8617                   1829        A     MAR,NULL,AR             (MAR)=START ADDRESS                 73218290
461       53 B241                   1830        S     MR1,MDR,ARL,D2+CO       (MR0,MR1)=END MINUS START           73218300
462       50 07C0                   1831        S     MR0,MR0,ARH,CI+CO       VECTOR THROUGH DROM 2               73218310
                                    1832  *                                                                         73218320
                0463                1833  WBR     EQU   *                       WRITE BLOCK REGISTER        * 96 *  73218330
                0463                1834  RBR     EQU   *                       READ BLOCK REGISTER         * 97 *  73218340
                                    1835  *                                                                         73218350
463       00 C835                   1836  WBRRBR  L     IO,YDL,ADRS             ADDRESS THE DEVICE                  73218360
464       00 E80B                   1837        L     AR,YSL                  (AR)=START ADDRESS                  73218370
465       40 610C                   1838        A     YSI,YSI,ONE             POINT TO R2+1                       73218380
466       50 EA41                   1839        S     MR1,YSL,ARL,CO          (MR0,MR1)=END MINUS START           73218390
467       53 E7C0                   1840        S     MR0,YSH,ARH,CI+CO+D2    VECTOR THROUGH DROM 3               73218400
468       40 8617                   1841        A     MAR,NULL,AR             (MAR)=START ADDRESS                 73218410
                                    1842  *                                                                         73218420
                                    1843  * COMMON ROUTINE FOR WB,WBR         DROM 2 ENTRY POINT                  73218430
                                    1844  *                                                                         73218440
469       E2 0473                   1845  LOOPW   BT    C,FINIS                 EXIT WHEN DELTA GOES NEGATIVE       73218450
46A       08 8010                   1846        L     NULL,NULL,MR            FETCH EVEN/ODD BYTE PAIR            73218460
46B       00 A8CF                   1847  STATW   L     FLR,IO,STAT             SENSE DEVICE STATUS                 73218470
46C       E3 C471                   1848        BT    C+V+G+L,TESTW           TEST IF ANY BITS SET                73218480
46D       00 B655                   1849        L     IO,MDR,DA+CS            OUTPUT BYTE                         73218490
46E       50 0941                   1850        S     MR1,MR1,ONE,CO          DECREMENT BYTE COUNT                73218500
46F       53 00C0                   1851        S     MR0,MR0,NULL,CI+CO+D2                                       73218510
470       40 B917                   1852        A     MAR,MAR,ONE             BUMP MAR; LOOP THRU DROM 2          73218520
471       E1 C448                   1853  TESTW   BT    V+G+L,FETCHJ            EXIT ON BAD STATUS (P.43)           73218530
472       F0 046B                   1854        B     STATW                   LOOP ON BUSY                        73218540
                                    1855  *                                                                         73218550
473       00 800F                   1856  FINIS   L     FLR,NULL                CLEAR FLAGS                         73218560
474       F0 0448                   1857  FINIS1  B     FETCHJ                  (P.43)                              73218570
                                    1858  *                                                                         73218580
                                    1859  * COMMON ROUTINE FOR RB,RBR         DROM 2 ENTRY POINT                  73218590
                                    1860  *                                                                         73218600
475       E2 0473                   1861  LOOPR   BT    C,FINIS                 EXIT WHEN DELTA GOES NEGATIVE       73218610
476       08 8010                   1862        L     NULL,NULL,MR            FETCH EVEN/ODD BYTE PAIR            73218620
477       00 A8CF                   1863  STATR   L     FLR,IO,STAT             SENSE DEVICE STATUS                 73218630
478       E3 C47D                   1864        BT    C+V+G+L,TESTR           TEST IF ANY BITS SET                73218640
479       0E AEB6                   1865        L     MDR,IO,DR+CS+MW         INPUT BYTE AND STORE                73218650
47A       50 0941                   1866  LOOPR1  S     MR1,MR1,ONE,CO          DECREMENT BYTE COUNT                73218660
47B       53 00C0                   1867        S     MR0,MR0,NULL,CI+CO+D2                                       73218670
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47C     40 B917     1868          A     MAR,MAR,ONE      BUMP MAR1 LOOP THRU PROM2          73218680
47D     E1 C44B     1869  TESTR   BT    V+6+L,FETCHJ     EXIT ON BAD STATUS (P.43)          73218690
47E     F0 0477     1870          B     STATR            LOOP ON BUSY                       73218700

                    1872  *                                                                 73218720
        047F        1873  AL      EQU   *                AUTO-LOAD                  * D5 *  73218730
                    1874  *                                                                 73218740
47F     60 A417     1875          CA    MAR,LOC,MDR      (MAR)=FINAL ADDRESS                73218750
480     00 B808     1876          L     AR,MAR           ADDRESS TO (ARH,ARL)               73218760
481     87 8017     1877          LI    MAR,'78'         BINDV SPECIFICATION                73218770
482     4A 8700     1878          A     MR0,NULL,ARH,MR0 (MR0),MR1)=END ADDRESS             73218780
483     40 8201     1879          A     MR1,NULL,ARL                                        73218790
484     88 0017     1880          LI    MAR,'80'         (MAR)=START ADDRESS, '80'          73218800
485     00 B80B     1881          L     AR,MAR                                              73218810
486     50 0A41     1882          S     MR1,MR1,ARL,CO   (MR0,MR1)=END-START                73218820
487     50 07C0     1883          S     MR0,MR0,ARH+CI+CO                                   73218830
488     E2 0473     1884          BT    C,FINIS          NO LOAD IF END < START (P.44)      73218840
489     00 B609     1885          L     ARL,MDR,CS                                          73218850
48A     9F F206     1886          NI    MR6,'FF',ARL                                        73218860
48B     00 3035     1887          L     IO,MR6,ADRS      ADDRESS THE DEVICE                 73218870
48C     08 8075     1888          L     IO,MDR,OC+MR     OUTPUT COMMAND                     73218880
48D     00 A8CF     1889  INAL    L     FLR,IO,STAT      SENSE STATUS                       73218890
48E     E1 C44B     1890          BT    V+6+L,FETCHJ     EXIT ON BAD STATUS (P.43)          73218900
48F     E2 048D     1891          BT    C,INAL           LOOP ON BUSY                       73218910
490     00 A8A6     1892          L     MR6,IO,DR        READ DATA BYTE                     73218920
491     00 3616     1893          L     MDR,MR6,CS       INSERT IN MDR                      73218930
492     00 3030     1894          L     NULL,MR6,F       TEST IF ZERO                       73218940
493     F0 C48D     1895          BF    G+L,INAL         SKIP UNTIL READ NON-BLANK          73218950
494     7E 0000     1896          C     MW               STORE THIS BYTE                    73218960
495     F0 047A     1897          B     LOOPR1           GO TO READ BLOCK ROUTINE (P.44)    73218970
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                0496                1899  SCP       EQU   *                 SIMULATE CHANNEL PROGRAM      * E3 *   73218990
                                    1900  *                                                                        73219000
496     60 A417                     1901              CA    MAR,LOC,MDR       (MAR)=ADDRESS OF CCB                 73219010
497     09 B808                     1902              L     AR,MAR,MR2        SAVE ADRS, FETCH CCW                 73219020
498     40 8701                     1903              A     MR1,NULL,ARH                                           73219030
499     00 B00F                     1904              L     FLR,MDR           TEST CCW BITS 12:15                  73219040
49A     F2 049C                     1905              BF    C,*+2             BRANCH IF BUFFER 0                   73219050
49B     C0 A617                     1906              AI    MAR,10,AR         (MAR)=BUFFER 1 BYTE COUNT ADRS       73219060
49C     08 B000                     1907              L     MR0,MDR,MR        (MR0)=CCW                            73219070
49D     40 8202                     1908              A     MR2,NULL,ARL      (MR1,MR2)=CCW ADRS                   73219080
49E     00 800F                     1909              L     FLR,NULL                                               73219090
49F     00 B029                     1910              L     ARL,MDR,F         TEST BUFFER BYTE COUNT               73219100
4A0     E0 82B2                     1911              BT    G,LSTOUF          EXIT IF COUNT POSITIVE (P,29)        73219110
4A1     40 850A                     1912              A     ARH,NULL,SIGN     PROPOGATE SIGN THRU AR 0:15          73219120
4A2     4F B116                     1913              A     MDR,MDR,ONE,MW2   INCR, COUNT & RESTORE                73219130
4A3     80 000F                     1914              LI    FLR,0                                                  73219140
4A4     09 B023                     1915              L     MR3,MDR,MR2+F     SAVE INCREMENTED COUNT               73219150
4A5     7B 0088                     1916              C     JH+XR2            SET CC, FETCH END ADRS               73219160
4A6     00 000F                     1917              L     FLR,MR0                                                73219170
4A7     40 B617                     1918              A     MAR,MDR,AR        COUNT PLUS END ADRS                  73219180
4A8     08 080A                     1919              L     ARH,MR1,MR        FETCH EVEN/ODD BYTE PAIR             73219190
4A9     E1 04AC                     1920              BT    V,WRTSC           WRITE IF R/W =1                      73219200
                                    1921  *                                   READ IF R/W =0                       73219210
4AA     0E CE16                     1922              L     MDR,YDL,CS+MW     INSERT BYTE FROM R1                  73219220
4AB     F0 04AF                     1923              B     RWSC              SKIP TO COMMON ROUTINE               73219230
                                    1924  *                                                                        73219240
4AC     00 8018                     1925  WRTSC       L     YDH,NULL          CLEAR R1 0:15                        73219250
4AD     00 B609                     1926              L     ARL,MDR,CS        GET PROPER BYTE                      73219260
4AE     9F F219                     1927              NI    YDL,'FF',ARL      MASK AND LOAD R1 16:31               73219270
4AF     00 800F                     1928  RWSC        L     FLR,NULL                                               73219280
4B0     00 1830                     1929              L     NULL,MR3,F        TEST NEW BYTE COUNT                  73219290
4B1     F0 82CC                     1930              BF    G,NBR             EXIT IF NOT POSITIVE (P,30)          73219300
4B2     00 000F                     1931              L     FLR,MR0                                                73219310
4B3     E0 42CC                     1932              BT    L,NBR             EXIT IF NOT FAST MODE (P,30)         73219320
4B4     00 1009                     1933              L     ARL,MR2                                                73219330
4B5     40 8617                     1934              A     MAR,NULL,AR       (MAR)=CCW ADDRESS                    73219340
4B6     80 8009                     1935              LI    ARL,9                                                  73219350
4B7     3E 0216                     1936              X     MDR,MR0,ARL,MW    COMPLEMENT BUFFER SWITCH             73219360
4B8     F0 02CC                     1937              B     NBR               EXIT (P,30)                          73219370
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                000D                1939  CRC       EQU   X'0D'              DESTINATION ADRS FOR CRC BOX          73219390
                                    1940  *                                                                      73219400
                                    1941  *                                                                      73219410
                04B9                1942  PB        EQU   *                  PROCESS BYTE              * 62 *      73219420
                                    1943  *                                                                      73219430
4B9       60 A417                   1944            CA    MAR,LOC,MDR        (MAR)=2ND OP ADDRESS                  73219440
                                    1945  *                                  THE HALFWORD SECOND OPERAND           73219450
                                    1946  *                                  CONTAINS THE RESIDUAL CHECKSUM        73219460
4BA       08 C08D                   1947            L     CRC,YDH,MR+CI      BITS 8:15 OF THE REGISTER             73219470
                                    1948  *                                  SPECIFIED BY R1 CONTAIN CONTROL       73219480
                                    1949  *                                  CODE INDICATING THE TYPE OF ERROR     73219490
                                    1950  *                                  CHECKING TO BE PERFORMED. OUTPUT      73219500
                                    1951  *                                  CONTROL CODE TO CRC HARDWARE.         73219510
4BB       00 B08D                   1952            L     CRC,MDR,CI         OUTPUT RESIDUAL CHECKWORD             73219520
4BC       00 C88D                   1953            L     CRC,YDL,CI         OUTPUT DATA BYTE TO BE INCLUDED       73219530
                                    1954  *                                  IN THE ERROR CHECK                    73219540
4BD       00 A896                   1955            L     MDR,IO,ACK         INPUT THE RESULT                      73219550
4BE       0E A017                   1956            L     MAR,LOC,MW         AND STORE IT.... (MAR)=(LOC)          73219560
4BF       F0 02CC                   1957            B     NBR                EXIT (P,30)                           73219570
                                    1958  *                                                                      73219580
                04C0                1959  PBR       EQU   *                  PROCESS BYTE REGISTER     * 32 *      73219590
                                    1960  *                                                                      73219600
4C0       00 C06D                   1961            L     CRC,YDH,CI         BITS 8:15 OF THE REGISTER             73219610
                                    1962  *                                  SPECIFIED BY R1 CONTAIN A             73219620
                                    1963  *                                  CONTROL CODE INDICATING THE           73219630
                                    1964  *                                  TYPE OF ERROR CHECKING TO BE          73219640
                                    1965  *                                  PERFORMED.  OUTPUT CONTROL            73219650
                                    1966  *                                  CODE TO CRC HARDWARE                  73219660
4C1       00 E86D                   1967            L     CRC,YSL,CI         OUTPUT RESIDUAL CHECKWORD             73219670
4C2       00 C88D                   1968            L     CRC,YDL,CI         OUTPUT DATA BYTE TO BE INCLUDED       73219680
                                    1969  *                                  IN THE ERROR CHECK                    73219690
4C3       03 8010                   1970            L     NULL,NULL,D2       VECTOR THROUGH DROM 3                 73219700
4C4       00 A89D                   1971            L     YSL,IO,ACK         INPUT THE RESULT, GO TO NBR (P,30)    73219710
                                    1972  *                                                                      73219720
                                    1973  *                                                                      73219730
4C5       F8 4258                   1974  CRCTEST   BF    DRD,CRCAUTO        IF DRD LINE INACTIVE, HARDWARE        73219740
                                    1975  *                                  ASSIST OPTION NOT PRESENT             73219750
                                    1976  *                                  GO TO CRCAUTO (P,27)                  73219760
                                    1977  * (MR1) CONTAINS THE CHANNEL COMMAND WORD                              73219770
                                    1978  * (MDR) CONTAINS OLD RESIDUAL                                         73219780
                                    1979  * (SRH 8:15) CONTAINS BYTE TO INCLUDE                                 73219790
                                    1980  *                                                                      73219800
4C6       00 0C05                   1981            L     MR5,MR1,SR         SHIFT CRC TYPE BITS DOWN              73219810
4C7       00 2C0F                   1982            L     FLR,MR5,SR         C FLAG = CRC TYPE                     73219820
4C8       00 8285                   1983            L     MR5,NULL,SL+CI     MR5 = 0000 OR 0001                    73219830
4C9       00 288D                   1984            L     CRC,MR5,CI         CONTROL BITS TO CRC HARDWARE          73219840
4CA       00 B08D                   1985            L     CRC,MDR,CI         OUTPUT OLD RESIDUAL                   73219850
4CB       00 988D                   1986            L     CRC,SRH,CI         OUTPUT DATA BYTE                      73219860
4CC       00 A896                   1987            L     MDR,IO,ACK         INPUT NEW RESIDUAL                    73219870
4CD       F0 016A                   1988            B     RETCRC             (P,17)                                73219880
4CE       00 8010                   1989            L     NULL,NULL          FILLER (NOT USED)                     73219890
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                04CF                1991  NPRSR   EQU   *                 MOVE & PROCESS BYTE STRING   * 30 *   73219910
                                    1992  *                                                                    73219920
4CF             00 D017             1993        L     MAR,YDLP1         THE REGISTER SPECIFIED BY R1           73219930
                                    1994  *                             CONTAINS THE START ADDRESS OF          73219940
4D0             00 D010             1995        L     NULL,YDLP1        BYTE STRING A.  THE REGISTER           73219950
                                    1996  *                             SPECIFIED BY R1+1 CONTAINS THE         73219960
                                    1997  *                             TRANSLATION TABLE ADDRESS, THE         73219970
                                    1998  *                             REGISTER SPECIFIED BY R1+2             73219980
                                    1999  *                             CONTAINS A POSITIVE COUNT OF           73219990
                                    2000  *                             THE NUMBER OF BYTES TO THE             73220000
4D1             00 8010             2001        L     NULL,NULL         SOURCE STRING 'A'.  AFTER THE          73220010
4D2             00 C001             2002        L     MR1,YDH           NOP REQUIRED TO SETTLE THE YD          73220020
4D3             00 D020             2003        L     MR0,YDLP1,F       FIELD, COPY THE BYTE COUNT             73220030
4D4             E0 42B2             2004        BT    L,LSTOUF          TO MR0, EXIT IF MINUS (P.29)           73220040
                                    2005  *                                                                    73220050
                                    2006  *                             THE REGISTER SPECIFIED BY R1+2         73220060
                                    2007  *                             CONTAINS IN BITS 0:15, CONTROL         73220070
                                    2008  *                             CODES IDENTIFYING THE MANNER IN        73220080
                                    2009  *                             WHICH TRANSLATION AND ERROR            73220090
                                    2010  *                             CHECKING IS TO BE PERFORMED IN         73220100
4D5             00 0E0F             2011        L     FLR,MR1,CS        CONJUNCTION WITH THE BYTE MOVE         73220110
4D6             E1 0514             2012        BT    V,TRONLY          TRANSLATE ONLY (P.50)                  73220120
                                    2013  *                             BITS 8:15 SPECIFY THE TYPE OF          73220130
4D7             00 088D             2014        L     CRC,MR1,CI        ERROR CHECK, OUTPUT CODE TO            73220140
                                    2015  *                             THE CRC HARDWARE.  BITS 4:7            73220150
                                    2016  *                             CONTROL ERROR CHECKING AND             73220160
4D8             00 D88D             2017        L     CRC,YDLM1,CI      TRANSLATION, OUTPUT RESIDUAL           73220170
                                    2018  *                             CHECKWORD TO CRC HARDWARE              73220180
4D9             00 0810             2019        L     NULL,YDLM1        NOP...POINTING TO TRANSLATION          73220190
4DA             F2 052D             2020        BF    C,CKONLY          TABLE ADDRESS, CHECK ONLY (P.51)       73220200
4DB             F0 8500             2021        BF    G,CKTR            CHECK THEN TRANSLATE (P.50)            73220210

                                    2023  *       TRANSLATE THEN ERROR CHECK                                   73220230
                                    2024  *                                                                    73220240
                                    2025  * (MR0)=BYTE COUNT                                                   73220250
                                    2026  * YD FIELD POINTS TO R1+1 (ADRS OF TRANSLATION TABLE)               73220260
                                    2027  *                                                                    73220270
                                    2028  *                                                                    73220280
4DC             08 8010             2029  TRCK  L     NULL,NULL,MR      READ EVEN/ODD BYTE PAIR                73220290
4DD             EB 353E             2030        BT    CATN+SNGL+MALF+PPF,DONE0                                 73220300
4DE             E4 353E             2031        BT    ATN+MAC,DONE0     EXIT IF INTERRUPT PENDING (P.51)       73220310
4DF             00 B609             2032        L     ARL,MDR,CS        PICK OUT APPROPRIATE BYTE              73220320
4E0             9F F204             2033        NI    MR4,'FF',ARL      (MR4)=SOURCE BYTE                      73220330
4E1             00 2216             2034        L     MDR,MR4,SL        2X SOURCE BYTE PLUS TRANSLATION        73220340
4E2             40 DC17             2035        A     MAR,YDLM1,MDR     TABLE ADDRESS: POINT TO R1             73220350
4E3             08 E817             2036        L     MAR,YSL,MR        FETCH TABLE ENTRY THEN SET             73220360
4E4             40 E95D             2037        A     YSL,YSL,ONE,CO    MAR EQUAL DESTINATION ADDRESS          73220370
4E5             40 E09C             2038        A     YSH,YSH,NULL,CI   INCREMENT DESTINATION ADDRESS          73220380
4E6             08 B025             2039        L     MR5,MDR,MR+F      TEST MSB OF TABLE ENTRY                73220390
                                    2040  *                             FETCH DESTINATION HALFWORD             73220400
4E7             F0 4544             2041        BF    L,SUBR            EXIT TO SUBROUTINE IF PLUS (P.52)      73220410
                                    2042  *                                                                    73220420
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                        2043  * (MR5)=TRANSLATED CHARACTER, PERFORM ERROR CHECKING                    73220430
                        2044  *                                                                       73220440
4E8   00 288D           2045          L     CRC,MR5,CI      SEND BYTE TO ERROR CHECK                  73220450
                        2046  *                             HARDWARE.  THE CRC HARDWARE               73220460
                        2047  *                             MAINTAINS RESIDUAL CHECKWORD              73220470
4E9   0E 2E16           2048          L     MDR,MR5,CS+MW   INSERT TRANSLATED BYTE & STORE            73220480
4EA   40 C959           2049          A     YDL,YDL,ONE,CO  INCREMENT SOURCE ADDRESS                  73220490
4EB   40 C098           2050          A     YDH,YDH,NULL,CI                                           73220500
4EC   00 D017           2051          L     MAR,YDLP1       (MAR)=NEW SOURCE ADDRESS                  73220510
4ED   50 0140           2052          S     MR0,MR0,ONE,CO  DECREMENT BYTE COUNT                      73220520
4EE   F2 04DC           2053          BF    C,TRCK          LOOP IF NOT NEGATIVE (P.48)               73220530

                        2055  * NORMAL EXIT.  NEED TO UPDATE ACCUMULATED CHECKSUM                     73220550
                        2056  * AND THE BUFFER BYTE COUNT.  YD FIELD =R1+1                            73220560
                        2057  *                                                                       73220570
4EF   00 D010           2058  DONE    L     NULL,YDLP1      POINT TO R1+2                             73220580
4F0   50 6118           2059          S     YDH,NULL,ONE    SET MS COUNT TO ALL ONES                  73220590
4F1   00 A017           2060          L     MAR,LOC         (MAR)=(LOC)                               73220600
4F2   00 001A           2061  DONEOA  L     YDLP1,MR0       UPDATE LS COUNT; POINT TO R1+3            73220610
4F3   07 A899           2062          L     YDL,IO,ACK+IRJ  UPDATE CHECKWORD                          73220620
4F4   80 000F           2063          LI    FLR,0           FETCH NEXT INSTR, CC=0000                 73220630

                        2065  * FLOATING POINT REGISTER DISPLAY                                       73220650
                        2066  *                                                                       73220660
4F5   80 E009           2067  FLTREG  LI    ARL,'E'                                                   73220670
4F6   10 6202           2068          N     MR2,YSI,ARL     FORCE EVEN FLOATING REGISTER              73220680
4F7   00 1217           2069          L     MAR,MR2,SL      REGISTER ADDRESS TO MAR                   73220690
4F8   0D 8010           2070          L     NULL,NULL,MRD2  START MEMORY READ, NO MAC                  73220700
4F9   0A B000           2071          L     MR0,MDR,MRD     (MR0)=D2,D1=FLT.REG.(0:15)                73220710
4FA   00 B001           2072          L     MR1,MDR         (MR1)=D4,D3=FLT.REG.(16:31)               73220720
4FB   81 0009           2073          LI    ARL,'10'        (MR2)=D5,=FLT.REG. #                      73220730
4FC   20 1202           2074          O     MR2,MR2,ARL                                               73220740
4FD   F0 0069           2075          B     OUTDIS          (P.7)                                     73220750
4FE   00 8010           2076          L     NULL,NULL       FILLER (NOT USED)                         73220760
                        2077  *                             IF PRIVILEGED INSTR & PROTECT             73220770
4FF   F0 0003           2078          B     ILLEG           MODE, GO TO ILLEGAL (P.3)                 73220780
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                        2080  *          ERROR CHECK THEN TRANSLATE                                    73220800
                        2081  *                                                                        73220810
500  08 8010            2082  CKTR   L    NULL,NULL,MR          READ EVEN/ODD BYTE PATR                 73220820
501  EB 353E            2083         BT   CATN+SNGL+MALF+PPF,DONE0                                      73220830
502  E4 353E            2084         BT   ATN+MAC,DONE0         EXIT IF INTERRUPT PENDING (P.51)        73220840
503  00 B609            2085         L    ARL,MDR,CS            PICK OUT APPROPRIATE BYTE               73220850
504  9F F204            2086         NI   MR4,'FF',ARL          (MR4)=SOURCE BYTE                       73220860
505  00 2216            2087         L    MDR,MR4,SL            2XARGUMENT BYTE PLUS                    73220870
506  40 DC17            2088         A    MAR,YDLM1,MDR         TRANSLATION TABLE ADDRESS               73220880
507  08 E817            2089         L    MAR,YSL,MR            FETCH TABLE ENTRY, MAR EQUALS           73220890
508  40 E95D            2090         A    YSL,YSL,ONE,CO        DESTINATION ADDRESS                     73220900
509  40 E09C            2091         A    YSH,YSH,NULL,CI       INCREMENT DESTINATION ADDRESS           73220910
50A  08 B025            2092         L    MR5,MDR,MR+F          TEST MSB OF TABLE ENTRY AND             73220920
                        2093  *                                FETCH DESTINATION HALFWORD              73220930
50B  F0 4544            2094         BF   L,SUBR                EXIT TO SUBROUTINE IF MSB (P.52)        73220940
                        2095  *                                OF TABLE ENTRY IS NOT SET               73220950
                        2096  *                                OUTPUT ORIGINAL BYTE TO THE             73220960
50C  00 208D            2097         L    CRC,MR4,CI            CRC HARDWARE.  THE HARDWARE             73220970
                        2098  *                                MAINTAINS THE RESIDUAL CHECKWORD        73220980
50D  0E 2E16            2099         L    MDR,MR5,CS+MW         INSERT TRANSLATED BYTE                  73220990
50E  40 C959            2100         A    YDL,YDL,ONE,CO        INCREMENT SOURCE ADDRESS                73221000
50F  40 C098            2101         A    YDH,YDH,NULL,CI                                               73221010
510  00 D017            2102         L    MAR,YDLP1             (MAR)=NEW SOURCE ADDRESS                73221020
511  50 0140            2103         S    MR0,MR0,ONE,CO        DECREMENT BYTE COUNT                    73221030
512  F2 0500            2104         BF   C,CNTR                LOOP IF NOT NEGATIVE                    73221040
513  F0 04EF            2105         B    DONE                  (P.49)                                  73221050


                        2107  *          PERFORM TRANSLATION ONLY                                      73221070
                        2108  *                                                                        73221080
514  00 D810            2109  TRONLY L    NULL,YDLM1            POINT TO R1+2                           73221090
515  00 D810            2110         L    NULL,YDLM1            POINT TO R1+1                           73221100
                        2111  *                                                                        73221110
516  08 8010            2112  TRA    L    NULL,NULL,MR          READ SOURCE BYTE                        73221120
517  EB 3541            2113         BT   CAT,+SNGL+MALF+PPF,DONE2                                      73221130
518  E4 3541            2114         BT   ATN+MAC,DONE2         EXIT IF INTERRUPT PENDING (P.51)        73221140
519  00 B609            2115         L    ARL,MDR,CS            PICK OUT APPROPRIATE BYTE               73221150
51A  9F F204            2116         NI   MR4,'FF',ARL          (MR4)=SOURCE BYTE                       73221160
51B  00 2216            2117         L    MDR,MR4,SL            2X SOURCE BYTE PLUS TRANSLATION         73221170
51C  40 DC17            2118         A    MAR,YDLM1,MDR         TABLE ADDRESS                           73221180
51D  08 E817            2119         L    MAR,YSL,MR            FETCH TABLE ENTRY                       73221190
51E  40 E95D            2120         A    YSL,YSL,ONE,CO        INCREMENT DESTINATION ADDRESS           73221200
51F  40 E09C            2121         A    YSH,YSH,NULL,CI                                               73221210
520  08 B025            2122         L    MR5,MDR,MR+F          TEST TABLE ENTRY                        73221220
521  F0 4549            2123         BF   L,SUBR1               EXIT TO SUBROUTINE IF BIT 0=0 (P.52)    73221230
522  40 C959            2124         A    YDL,YDL,ONE,CO        INCREMENT SOURCE ADDRESS                73221240
523  40 C098            2125         A    YDH,YDH,NULL,CI                                               73221250
524  0E 2E16            2126         L    MDR,MR5,CS+MW         INSERT TRANSLATED BYTE                  73221260
525  00 D017            2127         L    MAR,YDLP1             (MAR)=NEW SOURCE ADDRESS                73221270
526  50 0140            2128         S    MR0,MR0,ONE,CO        DECREMENT BYTE COUNT                    73221280
527  F2 0516            2129         BF   C,TRA                 LOOP IF NOT NEGATIVE                    73221290
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                        2131  *                                                                  73221310
                        2132  * NORMAL EXIT, NEED TO UPDATE BUFFER BYTE COUNT                    73221320
                        2133  *                                                                  73221330
528  00 D010            2134  DONE1     L     NULL,YDLP1          POINT TO R1+2                 73221340
529  50 8118            2135            S     YDH,NULL,ONE        SET MS COUNT TO ALL ONES      73221350
52A  00 A017            2136            L     MAR,LOC             (MAR)=(LOC)                   73221360
52B  07 0019            2137            L     YDL,MR0,IRJ         UPDATE BYTE COUNT             73221370
52C  80 000F            2138            LI    FLR,0               FETCH NEXT INSTR. CC=0000     73221380

                        2140  *              PERFORM ERROR CHECK ONLY                            73221400
                        2141  *                                                                  73221410
52D  08 D810            2142  CKONLY    L     NULL,YDLM1,MR       READ SOURCE BYTE, POINT TO R1 73221420
52E  EB 353D            2143            BT    CATN+SNGL+MALF+PPF,DONE0B                        73221430
52F  E4 353D            2144            BT    ATN+MAC,DONE0B      EXIT IF INTERRUPT PENDING     73221440
530  40 C959            2145            A     YDL,YDL,ONE,CO      INCREMENT SOURCE ADDRESS      73221450
531  40 C098            2146            A     YDH,YDH,NULL,CI                                   73221460
532  00 B609            2147            L     ARL,MDR,CS          PICK OUT APPROPRIATE BYTE     73221470
533  00 E817            2148            L     MAR,YSL             (MAR)=DESTINATION ADDRESS     73221480
534  9F F204            2149            NI    MR4,'FF',ARL        (MR4)=SOURCE BYTE             73221490
535  48 E95D            2150            A     YSL,YSL,ONE,CO+MR   INCREMENT DESTINATION ADDRESS 73221500
536  40 E09C            2151            A     YSH,YSH,NULL,CI                                   73221510
                        2152  *                                   SEND BYTE TO CRC HARDWARE     73221520
537  00 208D            2153            L     CRC,MR4,CI          HARDWARE MAINTAINS RESIDUAL   73221530
538  0E 2616            2154            L     MDR,MR4,CS+MW       INSERT ARGUMENT BYTE & STORE  73221540
539  50 0140            2155            S     MR0,MR0,ONE,CO      DECREMENT BYTE COUNT          73221550
53A  00 D017            2156            L     MAR,YDLP1           (MAR)=NEW SOURCE ADDRESS      73221560
53B  F2 052D            2157            BF    C,CKONLY            LOOP IF COUNT NOT NEGATIVE    73221570
53C  F0 04EF            2158            B     DONE                (P,49)                        73221580
                        2159  *                                                                  73221590
                        2160  *                                                                  73221600
53D  00 D010            2161  DONE0B    L     NULL,YDLP1          POINT TO R1+1                 73221610
53E  50 A314            2162  DONE0     S     LOC,LOC,TWO         DECREMENT LOCATION COUNTER    73221620
53F  00 D010            2163            L     NULL,YDLP1          POINT TO R1+2                 73221630
540  F0 04F2            2164            B     DONE0A              (P,49)                        73221640
                        2165  *                                                                  73221650
                        2166  *                                                                  73221660
541  50 A314            2167  DONE2     S     LOC,LOC,TWO         DECREMENT LOCATION COUNT      73221670
542  04 D010            2168            L     NULL,YDLP1,IR       POINT TO R1+2                 73221680
543  00 0019            2169            L     YDL,MR0             FETCH NEXT INSTRUCTION        73221690
                        2170  *                                   AND UPDATE BYTE COUNT         73221700
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                        2172  *                    EXIT TO SUBROUTINE                                                  73221720
                        2173  *                                                                                        73221730
                        2174  * NEED TO UPDATE ACCUMULATED CHECKSUM & BYTE COUNT                                      73221740
                        2175  *                                                                                        73221750
544     00 D010         2176  SUBR    L     NULL,YDLP1       POINT TO R1+1                                            73221760
545     00 D010         2177          L     NULL,YDLP1       POINT TO R1+2                                            73221770
546     00 D010         2178          L     NULL,YDLP1       POINT TO R1+3                                            73221780
547     00 A89B         2179          L     YDLM1,IO,ACK     UPDATE CHECKWORD, POINT TO R1+2                          73221790
548     F0 054B         2180          B     SUBR2                                                                     73221800
                        2181  *                                                                                        73221810
549     00 D010         2182  SUBR1   L     NULL,YDLP1       POINT TO R1+1                                            73221820
54A     00 D010         2183          L     NULL,YDLP1       POINT TO R1+2                                            73221830
54B     00 001A         2184  SUBR2   L     YDLP1,MR0        UPDATE BYTE COUNT                                        73221840
54C     00 D010         2185          L     NULL,YDLP1       POINT TO R1+4                                            73221850
54D     50 A359         2186          S     YDL,LOC,TWO,CO   SAVE LOC-2                                               73221860
54E     50 8898         2187          S     YDH,LOCH,NULL,CI                                                          73221870
54F     00 2A14         2188          L     LOC,MR5,SL       (LOC)=(MAR)=SUBR. ADDRESS                                73221880
550     50 E95D         2189          S     YSL,YSL,ONE,CO   DECREMENT DESTINATION ADRS                              73221890
551     54 E09C         2190          S     YSH,YSH,NULL,CI+IR FETCH NEXT INSTRUCTION                                 73221900
552     00 8010         2191          L     NULL,NULL        NOP                                                      73221910
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                                2453            ELSE                                                                    73224530
                                2455    FLTREG0 EQU     '5DD'                                                           73224550
05DD                                                                                                                    73224560
05EA                            2456    SAVEFLPT EQU    '5EA'                                                           73224570
05F6                            2457    RSTRFLPT EQU    '5F6'                                                           73224580
                                2458    *
0553                            2459    LER     EQU     *       LOAD FLOATING POINT REGISTER * 28 *                     73224590
                                2460    *                                                                               73224600
553     00 6217                 2461            L       MAR,YSI,SL      (MAR)=2ND OP ADDRESS                            73224610
554     7D 00A0                 2462            C       MRD2+TABT       ENABLE ABORT, FETCH 1ST HW                      73224620
                                2463    *               NO MAC INTERFERENCE ON READ                                     73224630
555     00 6A00                 2464            L       MR0,YDI,SL      (MR0)=1ST OP ADDRESS                            73224640
556     9F F433                 2465            NI      SRH,'FF',MDR,F  (SRH)=HIGH FRACTION                             73224650
557     30 9C04                 2466            X       MR4,SRH,MDR     (MR4)=SIGN & EXPONENT                           73224660
558     4A 0317                 2467            A       MAR,MR0,TWO,MRD (MAR)=1ST OP ADRS+2                             73224670
559     F0 0560                 2468            B       LE,LER          GO TO COMMON SEQUENCE                           73224680
                                2469    *                                                                               73224690
055A                            2470    LE      EQU     *       LOAD FLOATING POINT             * 68 *                  73224700
                                2471    *                                                                               73224710
55A     60 A417                 2472            CA      MAR,LOC,MDR     (MAR)=2ND OP ADDRESS                            73224720
55B     79 00A0                 2473            C       MR2+TABT        ENABLE ABORT, FETCH 1ST HW                      73224730
55C     00 6A00                 2474            L       MR0,YDI,SL      (MR0)=1ST OP ADDRESS                            73224740
55D     9F F433                 2475            NI      SRH,'FF',MDR,F  (SRH)=HIGH FRACTION, SET G                      73224750
55E     30 9C04                 2476            X       MR4,SRH,MDR     (MR4)=SIGN & EXPONENT                           73224760
55F     48 0317                 2477            A       MAR,MR0,TWO,MR  FETCH 2ND HW                                    73224770
                                2478    *               (MAR)=1ST OP ADDRESS+2                                          73224780
560     03 B032                 2479    LE,LER  L       SRL,MDR,F+D2    (SRH,SRL)=FRACTION                              73224790
                                2480    *               VECTOR THROUGH DROM 2                                           73224800
                                2481    *               TO LE,LERX, SET G&L (P.60)                                      73224810
561     00 2206                 2482            L       MR6,MR4,SL      (MR6)=EXPONENT LEFT ONCE                        73224820
562     00 8010                 2483            L       NULL,NULL       FILLER (NOT USED)                               73224830
563     00 8010                 2484            L       NULL,NULL       FILLER (NOT USED)                               73224840
564     00 8010                 2485            L       NULL,NULL       FILLER (NOT USED)                               73224850
                                2486    *                                                                               73224860
0565                            2487    LME     EQU     *       LOAD MULTIPLE FLOATING  * 72 *                          73224870
0565                            2488    STME    EQU     *       STORE MULTIPLE FLOATING * 71 *                          73224880
                                2489    *                                                                               73224890
565     60 A417                 2490            CA      MAR,LOC,MDR     (MAR)=2ND OP ADDRESS                            73224900
566     00 B80B                 2491            L       AR,MAR                                                          73224910
567     00 6A00                 2492            L       MR0,YDI,SL      (MR0)=1ST OP ADDRESS                            73224920
568     03 6816                 2493            L       MDR,YDI,D2      SET COUNTER EQUAL TO NUMBER                     73224930
569     D0 F408                 2494            SI      CTR,15,MDR      OF HALFWORDS TO TRANSFER                        73224940
                                2495    *               MINUS 1, VECTOR THROUGH DROM2                                   73224950
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56A  08 0017  2497  LME.D2   L    MAR,MR0,MR      FETCH A HALFWORD,                    73224970
56B  C0 260B  2498           AI   AR,2,AR         INCREMENT (ARH,ARL)                  73224980
56C  40 0300  2499           A    MR0,MR0,TWO     INCREMENT (MR0)                      73224990
56D  4C 8617  2500           A    MAR,NULL,AR,MWD STORE HALFWORD                       73225000
56E  FC 856A  2501           BF   CNTR,LME,D2     LOOP FOR ALL REGISTERS               73225010
56F  F0 02CC  2502           B    NBR             FETCH NEXT INSTRUCTION (P,30)        73225020
              2503  *                                                                  73225030
              2504  *                                                                  73225040
570  00 0017  2505  STME.D2  L    MAR,MR0         ADRS OF FIRST REGISTER               73225050
571  4A 8617  2506  STMELOOP A    MAR,NULL,AR,MRD FETCH A HALFWORD                     73225060
572  40 0300  2507           A    MR0,MR0,TWO     INCREMENT (MR0)                      73225070
              2508  *                                                                  73225080
573  C0 260B  2509  STE.D2   AI   AR,2,AR         INCREMENT (ARH,ARL)                  73225090
574  0E 0017  2510           L    MAR,MR0,MW      STORE HALFWORD                       73225100
575  FC 8571  2511           BF   CNTR,STMELOOP   LOOP FOR ALL REGISTERS               73225110
576  F0 02CC  2512           B    NBR             FETCH NEXT INSTRUCTION (P,30)        73225120
577  00 8010  2513           L    NULL,NULL       FILLER (NOT USED)                    73225130
578  00 8010  2514           L    NULL,NULL       FILLER (NOT USED)                    73225140
579  00 8010  2515           L    NULL,NULL       FILLER (NOT USED)                    73225150
57A  00 8010  2516           L    NULL,NULL       FILLER (NOT USED)                    73225160
              2517  *                                                                  73225170
     057B     2518  STF      EQU  *               STORE FLOATING POINT      * 6B *     73225180
              2519  *                                                                  73225190
57B  60 A417  2520           CA   MAR,LOC,MDR     (MAR)=2ND OP ADDRESS                 73225200
57C  00 B80B  2521           L    AR,MAR          COPY ADDRESS TO (ARH,ARL)            73225210
57D  00 6A17  2522           L    MAR,YDI,SL      (MAR)=1ST OP ADDRESS                 73225220
57E  4A BB00  2523           A    MR0,MAR,TWO,MRD FETCH HALFWORD                       73225230
57F  43 8617  2524           A    MAR,NULL,AR,D2  VECTOR THROUGH DROM 2                73225240
580  80 1006  2525           LI   CTR,1           TO STE.D2, (CTR)=1                   73225250
              2526  *                                                                  73225260
     0581     2527  CER      EQU  *               COMPARE FLOATING REGISTER * 29 *     73225270
     0581     2528  AER      EQU  *               ADD FLOATING POINT REGISTER * 2A *   73225280
     0581     2529  SER      EQU  *               SUBTRACT FLOATING REGISTER * 2B *    73225290
     0581     2530  MER      EQU  *               MULTIPLY FLOATING REGISTER * 2C *    73225300
     0581     2531  DER      EQU  *               DIVIDE FLOATING REGISTER * 2D *      73225310
              2532  *                                                                  73225320
581  00 6217  2533  FLPTRR   L    MAR,YSI,SL      (MAR)=2ND OP ADDRESS                 73225330
582  7D 00A0  2534           C    MRD2+TABT       ENABLE ABORT, FETCH 1ST HW           73225340
              2535  *                            NO MAC ON THIS READ                  73225350
583  8F F609  2536  FLPTRR1  LI   ARL,'FF',CS      (ARL)='FF00'                         73225360
584  9F F400  2537           NI   MR0,'FF',MDR    (MR0)=HIGH 2ND OP FRACTION           73225370
585  1A B208  2538           N    MR3,MDR,ARL,MRD (MR3)=2ND OP SIGN & EXPONENT         73225380
586  00 1A04  2539  FLPTRRRX L    MR4,MR3,SL      (MR4)=2ND OP EXPONENT                73225390
587  00 6A17  2540           L    MAR,YDI,SL      (MAR)=1ST OP ADDRESS                 73225400
588  0D B001  2541           L    MR1,MDR,MRD2    (MR0,MR1)=2ND OP FRACTION            73225410
589  9F F402  2542           NI   MR2,'FF',MDR    (MR2)=HIGH 1ST OP FRACTION           73225420
58A  13 B205  2543           N    MR5,MDR,ARL,D2  (MR5)=1ST OP SIGN & EXPONENT         73225430
58B  0A 2A06  2544           L    MR6,MR5,SL,MRD  (MR6)=1ST OP EXPONENT, FETCH         73225440
              2545  *                            REST OF 1ST OP FRACTION              73225450
              2546  *                            VECTOR THROUGH DROM 2                73225460
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                058C                2548  CE      EQU   *                 COMPARE FLOATING POINT      * 69 *  73225480
                058C                2549  AE      EQU   *                 ADD FLOATING POINT          * 6A *  73225490
                058C                2550  SE      EQU   *                 SUBTRACT FLOATING POINT     * 6B *  73225500
                058C                2551  ME      EQU   *                 MULTIPLY FLOATING POINT     * 6C *  73225510
                058C                2552  DE      EQU   *                 DIVIDE FLOATING POINT       * 6D *  73225520
                                    2553  *                                                                   73225530
58C      60 A417                    2554  FLPTRX  CA    MAR,LOC,MDR       (MAR)=2ND OP ADDRESS              73225540
58D      79 00A0                    2555          C     MR2+TABT          ENABLE ABORT, FETCH 1ST HW        73225550
58E      8F F609                    2556          LI    ARL,'FF','CS      (ARL)='FF00'                      73225560
58F      9F F400                    2557          NI    MR0,'FF',MDR      (MR0)=HIGH 2ND OP FRACTION        73225570
590      18 B203                    2558          N     MR3,MDR,ARL,MR    (MR3)=2ND OP SIGN & EXPONENT      73225580
591      F0 0586                    2559          B     FLPTRRRX          TO COMMON CODE (P.541             73225590
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                0592                2561  FXR     EQU   *                       FIX REGISTER                    * 2F *   73225610
                                    2562  *                                                                              73225620
592     00 6217                     2563          L     MAR,YSI,SL              (MAR)=2ND OP ADDRESS                     73225630
593     4D 8301                     2564          A     MR1,NULL,TWO,MRD2       FETCH 1ST HW. NO MAC                     73225640
594     00 0A08                     2565          L     CTR,MR1,SL              (CTR)=4                                  73225650
595     00 B000                     2566          L     MR0,MDR                 (MR0)=HI 2ND OPERAND                     73225660
596     0A B013                     2567          L     SRH,MDR,MRD             (SRH)=(MR0),FETCH LO 2ND OP              73225670
597     00 060A                     2568          L     ARH,MR0,CS                                                       73225680
598     00 B012                     2569          L     SRL,MDR                 (SRH,SRL)=SECOND OP                      73225690
599     70 0010                     2570          C     CUT                                                              73225700
59A     00 A017                     2571          L     MAR,LOC                 (MAR)=(LOC)                              73225710
59B     70 0008                     2572          C     RPT                                                              73225720
59C     70 1400                     2573          C     SL2                     SHIFT FRACTION LEFT 8                    73225730
59D     97 F70A                     2574          NI    ARH,'7F',ARH            (ARH)=2ND OP EXPONENT                    73225740
59E     D4 8756                     2575          SI    MDR,'48',ARH,CO         COMPARE TO UPPER LIMIT                   73225750
59F     E2 05A8                     2576          BT    C,OVF1                  OVERFLOW IF CARRY SET                    73225760
5A0     D0 7450                     2577          SI    NULL,'07',MDR,CO        COMPARE TO LOWER LIMIT                   73225770
5A1     F2 05A3                     2578          BF    C,*+2                   SKIP IF NO CARRY                         73225780
5A2     80 8016                     2579          LI    MDR,8                   FORCE VALUE TO 8                         73225790
5A3     00 B208                     2580          L     CTR,MDR,SL              2X VALUE                                 73225800
5A4     70 0008                     2581          C     RPT                                                              73225810
5A5     70 0C00                     2582          C     SR2                     SHIFT BACK RIGHT                         73225820
5A6     00 9A50                     2583          L     NULL,SRH,SL+CO          TEST MS BIT                              73225830
5A7     F2 05AB                     2584          BF    C,NOVF                  NO OVERFLOW                              73225840
5A8     70 0020                     2585  OVF1    C     SUT                                                              73225850
5A9     50 8112                     2586          S     SRL,NULL,ONE                                                     73225860
5AA     00 9413                     2587          L     SRH,SRL,SR              (SRH,SRL)='7FFFFFFF'                     73225870
5AB     00 0250                     2588  NOVF    L     NULL,MR0,SL+CO          PICK UP RESULT SIGN                      73225880
5AC     F2 05B1                     2589          BF    C,PLUS1                                                          73225890
5AD     00 9009                     2590          L     ARL,SRL                                                          73225900
5AE     00 980A                     2591          L     ARH,SRH                                                          73225910
5AF     50 8252                     2592          S     SRL,NULL,ARL,CO         2'S COMPLEMENT                           73225920
5B0     50 8793                     2593          S     SRH,NULL,ARH,CI                                                  73225930
5B1     FC 223D                     2594  PLUS1   BF    UT,RLX                  EXIT IF NO OVERFLOW (8,26)               73225940
5B2     00 0250                     2595          L     NULL,MR0,SL+CO                                                   73225950
5B3     D0 608F                     2596          SI    FLR,6,NULL,CI                                                    73225960
5B4     07 9019                     2597          L     YDL,SRL,IRJ             LOAD RESULT, FETCH NEXT                  73225970
5B5     00 9818                     2598          L     YDH,SRH                                                          73225980
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                05B6                    2600  FLR     EQU   *                 FLOAT REGISTER                  * 2F *  73226000
                                        2601  *                                                                     73226010
05B6        70 00A0                     2602          C     TABT              ENABLE ABORT                            73226020
05B7        00 E013                     2603          L     SRH,YSH           (SRH,SRL)=2ND OPERAND                   73226030
05B8        00 E812                     2604          L     SRL,YSL                                                   73226040
                                                                                                                      73226050
05B9        00 E250                     2605          L     NULL,YSH,SL+CO                                          73226060
05BA        00 8484                     2606          L     MR4,NULL,SR+CI    (MR4) HOLDS ARGUMENT SIGN              73226070
05BB        F2 05BE                     2607          BF    C,FLR3                                                  73226080
05BC        50 8252                     2608          S     SRL,NULL,ARL,CO   2'S COMP IF NEGATIVE                  73226090
05BD        50 8793                     2609          S     SRH,NULL,ARH,CI                                         73226100
05BE        00 9E0A                     2610  FLR3    L     ARH,SRH,CS                                              73226110
05BF        80 4008                     2611          LI    CTR,4                                                   73226120
05C0        89 0606                     2612          LI    MR6,'90',CS       PRESET EXPONENT='48'                  73226130
05C1        9F 0730                     2613          NI    NULL,'F0',ARH,F   TEST MS 4 ARGUMENT BITS               73226140
05C2        E0 85C9                     2614          BT    G,FLR1            TO FLR1 IF NON ZERO                   73226150
05C3        80 2008                     2615          LI    CTR,2                                                   73226160
05C4        88 E606                     2616          LI    MR6,'8E',CS       PRESENT EXPONENT='47'                 73226170
05C5        90 F730                     2617          NI    NULL,'0F',ARH,F   TEST MS 8 ARGUMENT BITS              73226180
05C6        E0 85C9                     2618          BT    G,FLR1            TO FLR1 IF NON ZERO                   73226190
05C7        80 0008                     2619          LI    CTR,0                                                   73226200
05C8        88 C606                     2620          LI    MR6,'8C',CS       PRESET EXPONENT='46'                  73226210
05C9        00 E830                     2621  FLR1    L     NULL,YSL,F        SET G&L                               73226220
05CA        00 E030                     2622          L     NULL,YSH,F                                              73226230
05CB        70 0008                     2623          C     RPT                                                     73226240
05CC        70 0C00                     2624          C     SR2               SHIFT (SRH,SRL) RIGHT                 73226250
                                        2625  *                               FOUR OR EIGHT PLACES                  73226260
05CD        00 6A17                     2626          L     MAR,YDI,SL        (MAR)=1ST OP ADDRESS                  73226270
05CE        40 BB17                     2627          A     MAR,MAR,TWO       1ST OP ADDRESS +2                     73226280
05CF        F0 061D                     2628          B     LE,LERX           GO TO LOAD SEQUENCE (P.60)            73226290
                                        2629  *                               TO NORMALIZE AND LOAD R1
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                        2631  * FLOATING POINT DIVISION BY ZERO                                    73226310
                        2632  *                                                                    73226320
5D0     70 00A0         2633  DIVZRO    C     TABT                DISABLE ABORT                  73226330
5D1     80 C00F         2634  DEZ       LI    FLR,'C'             SET C & V                      73226340
5D2     70 0088         2635            C     JH                  COPY FLR TO CONDITION CODE     73226350
5D3     F0 0059         2636            B     FFAULT              (P,6)                          73226360


                        2638  * EXPONENT OVERFLOW OR UNDERFLOW OR ZERO RESULT (MPY OR DIV)         73226380
                        2639  *                                                                    73226390
5D4     E0 45DD         2640  EXPOUF    BT    L,EXPOF             OVERFLOW IF L FLAG IS SET      73226400
                        2641  *                                                                    73226410
                        2642  * ZERO RESULT OR UNDERFLOW                                          73226420
                        2643  *                                                                    73226430
5D5     50 0150         2644  EXPUFZ    S     NULL,MR0,ONE,CO     SET CARRY IF 2ND OP IS ZERO    73226440
5D6     E2 0664         2645            BT    C,ZRESULT           (P,62)                         73226450
5D7     50 1150         2646            S     NULL,MR2,ONE,CO     SET CARRY IF 1ST OP IS ZERO    73226460
5D8     E2 0664         2647            BT    C,ZRESULT           (P,62)                         73226470
                        2648  *                                                                    73226480
                        2649  * EXPONENT UNDERFLOW                                               73226490
                        2650  *                                                                    73226500
5D9     00 8013         2651  EXPUF     L     SRH,NULL            (SRH,SRL)=RESULT               73226510
5DA     00 8012         2652            L     SRL,NULL                                           73226520
5DB     60 400F         2653            LI    FLR,4               CLEAR G&L, SET V               73226530
5DC     F0 05E5         2654            B     OUEXIT              TO COMMON EXIT                 73226540
                        2655  *                                                                    73226550
                        2656  * EXPONENT OVERFLOW                                                73226560
                        2657  * FORCE LARGEST MAGNITUDE                                          73226570
                        2658  *                                                                    73226580
5DD     50 8113         2659  EXPOF     S     SRH,NULL,ONE        (SRH,SRL)='FFFFFFFF'           73226590
5DE     00 9812         2660            L     SRL,SRH                                            73226600
5DF     60 500F         2661            LI    FLR,'5'             V&L FLAGS SET                  73226610
5E0     00 2250         2662            L     NULL,MR4,SL+CO      TEST RESULT SIGN               73226620
5E1     E2 05E4         2663            BT    C,EXPOF1            SKIP IF NEGATIVE               73226630
5E2     70 0800         2664            C     SR1                 (ARH,SRL)='7FFFFFFF'           73226640
5E3     60 600F         2665            LI    FLR,'6'             V&G FLAGS SET                  73226650
5E4     00 8050         2666  EXPOF1    L     NULL,NULL,CO        RESET CARRY                    73226660
5E5     00 9016         2667  OUFXIT    L     MDR,SRL                                            73226670
5E6     7E 0060         2668            C     MW+PRIV+TABT        STORE LOW RESULT               73226680
5E7     50 BB17         2669            S     MAR,MAR,TWO                                        73226690
5E8     00 9816         2670            L     MDR,SRH                                            73226700
5E9     7E 0098         2671            C     JH+MW+PRIV          (CC)=(FLR), STORE HIGH RESULT  73226710
5EA     F0 0059         2672            B     FFAULT              (P,6)                          73226720
                        2673  *                                                                    73226730
                        2674  *                                                                    73226740
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5EB                          2676          ORG   '600'                                          73226760
                             2677  * PROM 2 ENTRY POINT FOR SE,SER                              73226770
                             2678  *                                                            73226780
600     88 060A              2679  SE.SER  LI    ARH,'80',CS     (ARH)='8000'                   73226790
601     30 1F03              2680          X     MR3,MR3,ARH     COMPLEMENT THE 2ND OPERAND     73226800
                             2681  *               (SUBTRAHEND) SIGN AND ADD                    73226810
                             2682  *                                                            73226820
                             2683  * PROM 2 ENTRY POINT FOR AE,AER                              73226830
                             2684  *                                                            73226840
                             2685  AE.AER  L     ARL,MR2                                        73226850
602     00 1009              2686          S     NULL,MR1,MDR,CO COMPARE 1ST OP AND 2ND OP      73226860
603     50 0C50              2687          S     NULL,MR0,ARL,CI+CO FRACTIONS                   73226870
604     50 0200              2688          L     SRH,MR4,CS                                     73226880
605     00 2613              2689          L     ARL,MR6,CS                                     73226890
606     00 3609              2690          S     NULL,SRH,ARL,CI+CO INCLUDE EXPONENTS IN COMPARE 73226900
607     50 9AD0              2691          S     ARL,SRH,ARL     (ARL)=EXPONENT DELTA V2         73226910
608     50 9A09              2692          BT    C,AGB           BRANCH, A GREATER THAN B (P.61) 73226920
609     E2 063C              2693  *                                                            73226930
                             2694  * FIRST OPERAND LESS THAN OR EQUAL TO SECOND                 73226940
                             2695  *                                                            73226950
60A     D0 A250              2696          SI    NULL,10,ARL,CO  TEST EXPONENT DELTA            73226960
60B     E2 065F              2697          BT    C,BRESULT       1ST OPERAND WOULD LOSE         73226970
                             2698  *               SIGNIFICANCE; RESULT                         73226980
                             2699  *               EQUALS SECOND OPERAND (P.62)                 73226990
                             2700  *                                                            73227000
60C     C0 0208              2701          AI    CTR,0,ARL       EXPONENT DELTA TO COUNTER      73227010
60D     00 B012              2702          L     SRL,MDR         (SRH,SRL)=FIRST OP             73227020
60E     00 1013              2703          L     SRH,MR2                                        73227030
60F     00 0816              2704          L     MDR,MR1         (MR2,MDR)=SECOND OP            73227040
610     00 0002              2705          L     MR2,MR0                                        73227050
611     00 2006              2706          L     MR6,MR4         SWAP EXPONENTS                 73227060
612     00 1804              2707          L     MR4,MR3                                        73227070
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                                2709  *                                                                                  73227090
                                2710  * (CTR)=2X EXPONENT DELTA                                                        73227100
                                2711  * (SRH,SRL)=FRACTION OF SMALLER OPERAND                                         73227110
                                2712  * (MR2,MDR)=FRACTION OF LARGER OPERAND                                          73227120
                                2713  * (MR4)=SIGN & EXPONENT OF LARGER OPERAND                                       73227130
                                2714  * (MR6)=EXPONENT LEFT ONE OF LARGER OPERAND                                     73227140
                                2715  *                                                                               73227150
                                2716  * (MR3)=SIGN & EXPONENT OF 2ND OPERAND                                          73227160
                                2717  * (MR5)=SIGN & EXPONENT OF 1ST OPERAND                                          73227170
                                2718  *                                                                               73227180
                                2719  *                                                                               73227190
613     70 0008                 2720  CONT1     C     RPT                 EQUALIZE THE FRACTION OF                    73227200
614     70 0C00                 2721            C     SR2                 THE SMALL ER OPERAND                        73227210
615     00 2809                 2722            L     ARL,MR5                                                         73227220
616     30 1A30                 2723            X     NULL,MR3,ARL,F      COMPARE SIGNS OF TWO OPERANDS               73227230
617     F0 4630                 2724            BF    L,SUM               GENERATE SUM IF SIGNS ALIKE (P.61)          73227240
                                2725  *                                   DIFFERENCE IF SIGNS DIFFER                  73227250
                                2726  *                                                                               73227260
618     80 000F                 2727            LI    FLR,0               CLEAR FLAGS                                 73227270
619     00 9009                 2728            L     ARL,SRL                                                         73227280
61A     50 B272                 2729            S     SRL,MDR,ARL,F+CO    SUBTRACT SMALLER FROM LARGER                73227290
61B     00 9809                 2730            L     ARL,SRH                                                         73227300
61C     50 12F3                 2731            S     SRH,MR2,ARL,CI+CO+F                                             73227310
                                2732  *                                                                               73227320
                                2733  *                                                                               73227330
61D     F0 C664                 2734  LE.LERX   BF    G+L,ZRESULT         BRANCH IF ZERO (P.62)                       73227340
                                2735  *                                                                               73227350
                                2736  *                                                                               73227360
61E     FD 0627                 2737  NORMAL    BF    NNORM,FEND          EXIT IF NORMALIZED                          73227370
61F     80 0000                 2738            LI    MR0,0               CLEAR COUNT REGISTER                        73227380
620     70 1400                 2739  NORMLOOP  C     SL2                 SHIFT FRACTION LEFT                         73227390
621     70 1400                 2740            C     SL2                 ONE HEX POSITION                            73227400
622     40 0300                 2741            A     MR0,MR0,TWO         COUNT NUMBER OF SHIFTS DONE                 73227410
623     ED 0620                 2742            BT    NNORM,NORMLOOP      LOOP TIL NORMALIZED                         73227420
624     00 0609                 2743            L     ARL,MR0,CS          POSITION COUNT                              73227430
625     50 3246                 2744            S     MR6,MR6,ARL,CO      DECREMENT EXPONENT                          73227440
626     E2 05D9                 2745            BT    C,EXPUF             UNDERFLOW (P.58)                            73227450
                                2746  *                                                                               73227460
                                2747  * COMMON FLOATING POINT EXIT ROUTINE                                           73227470
                                2748  *                                                                               73227480
627     80 000F                 2749  FEND      LI    FLR,0               CLEAR FLAG REGISTER                         73227490
628     00 9036                 2750            L     MDR,SRL,F           LOW RESULT TO MDR                           73227500
629     7E 00B0                 2751            C     MW+PRIV+TABT        PRIVILEGED WRITE,KILL ABORT                 73227510
62A     50 BB17                 2752            S     MAR,MAR,TWO                                                     73227520
62B     00 2250                 2753            L     NULL,MR4,SL+CO      RESULT SIGN TO CARRY                        73227530
62C     00 3489                 2754            L     ARL,MR6,SR+CI       COMBINE WITH EXPONENT                       73227540
62D     20 9A76                 2755            O     MDR,SRH,ARL,F+CO    INSERT HIGH FRACTION                        73227550
62E     7E 0090                 2756            C     MW+PRIV             PRIVLEGED WRITE                             73227560
62F     F0 044B                 2757            B     FETCHJ              GO FETCH NEXT INSTRUCTION (P.43)            73227570
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630  00 1009   2759  SUM      L   ARL,MR2                                    73227590
631  40 9472   2760           A   SRL,SRL,MDR,CO+F      ADD FRACTIONS        73227600
632  40 9AF3   2761           A   SRH,SRH,ARL,CI+CO+F                        73227610
633  F0 8664   2762           BF  G,ZRESULT             BRANCH IF ZERO (P.62)73227620
                2763  *                                                     73227630
634  00 9E0F   2764  CARRYCK  L   FLR,SRH,CS            SEE IF CARRY INTO EXPONENT FIELD 73227640
635  F0 4627   2765           BF  L,FEND                NO CARRY, COMMON EXIT (P.60)     73227650
636  70 0C00   2766           C   SR2                   SHIFT RIGHT ONE HEX POSITION     73227660
637  70 0C00   2767           C   SR2                                        73227670
638  80 2609   2768           LI  ARL,2,CS              (ARL)='0200'         73227680
639  40 3246   2769           A   MR6,MR6,ARL,CO        INCREMENT EXPONENT   73227690
63A  F2 0627   2770           BF  C,FEND                OK IF NO CARRY (P.60)73227700
63B  F0 05DD   2771           B   EXPOF                 EXPONENT OVERFLOW (P.58)73227710
                2772  *                                                     73227720
                2773  *                                                     73227730
63C  D0 0209   2774  AGR      SI  ARL,0,ARL                                 73227740
63D  D0 A250   2775           SI  NULL,10,ARL,CO        TEST EXPONENT DELTA  73227750
63E  E2 065A   2776           BT  C,ARESULT             2ND OPERAND WOULD LOSE73227760
                2777  *                                 SIGNIFICANCE; RESULT 73227770
                2778  *                                 IS THE FIRST OPERAND (P.62)73227780
63F  C0 0208   2779           AI  CTR,0,ARL             2X DELTA TO COUNTER  73227790
640  00 0013   2780           L   SRH,MR0               (SRH,SRL)=SMALLER FRACTION73227800
641  00 0812   2781           L   SRL,MR1                                    73227810
642  00 2804   2782           L   MR4,MR5               (MR4)=SIGN & EXPONENT OF A73227820
643  F0 0613   2783           B   CONT1                 TO COMMON ROUTINE (P.60)73227830
644  00 8010   2784           L   NULL,NULL             FILLER               73227835
645  00 8010   2785           L   NULL,NULL             FILLER               73227836
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                                2787  * ROM 2 ENTRY POINT FOR CE,CER                                                    73227850
                                2788  *                                                                                 73227860
646     00 1809                 2789  CE.CER    L     ARL,MR3                                                           73227870
647     00 A017                 2790            L     MAR,LOC           (MAR)=(LOC)                                     73227880
648     30 2A30                 2791            X     NULL,MR5,ARL,F    COMPARE SIGNS OF OPERANDS                       73227890
649     E0 4658                 2792            BT    L,CE2             BRANCH IF DIFFERENT                             73227900
64A     80 000F                 2793            LI    FLR,0                                                             73227910
64B     00 0809                 2794            L     ARL,MR1                                                           73227920
64C     00 000A                 2795            L     ARH,MR0           (ARH,ARL)=2ND OP FRACTION                       73227930
64D     50 B270                 2796            S     NULL,MDR,ARL,CO+F SUBTRACT 1ST OP FRACTION                    73227940
64E     50 17F0                 2797            S     NULL,MR2,ARH,CI+CO+F                                            73227950
64F     00 200A                 2798            L     ARH,MR4                                                         73227960
650     50 37F0                 2799            S     NULL,MR6,ARH,CI+CO+F INCLUDE EXPONENTS IN COMPARE               73227970
651     F0 C65E                 2800            BF    G+L,CE4           BRANCH IF ZERO                                73227980
652     E2 0655                 2801            BT    C,CE3             TO CE3 IF A<B                                   73227990
653     00 2A50                 2802            L     NULL,MR5,SL+CO    C=SIGN OF 1ST OPERAND                         73228000
654     55 80B0                 2803            S     NULL,NULL,NULL,CI+F+IRJH SET CC, FETCH NEXT                     73228010
                                2804  *                                                                               73228020
655     88 0609                 2805  CE3       LI    ARL,'80',CS                                                     73228030
656     55 2A70                 2806            S     NULL,MR5,ARL,CO+F+IRJH SET CC, FETCH NEXT                       73228040
657     50 80F0                 2807            S     NULL,NULL,NULL,CI+CO+F NO V FLAG                                73228050
                                2808  *                                                                               73228060
658     00 2A50                 2809  CE2       L     NULL,MR5,SL+CO    CARRY=1ST OP SIGN                             73228070
659     07 2830                 2810            L     NULL,MR5,F+IRJ    ADJUST G,L                                    73228080
                                2811  *                                                                               73228090
                                2812  *                                                                               73228100
65A     00 1013                 2813  ARFSULT   L     SRH,MR2           (SRH,SRL)=1ST OP FRACTION                     73228110
65B     00 B012                 2814            L     SRL,MDR                                                         73228120
65C     C0 2804                 2815            L     MR4,MR5           COLLECT 1ST OP SIGN & FRACTION                73228130
65D     F0 0627                 2816            B     FEND              EXIT (P,60)                                   73228140
                                2817  *                                                                               73228150
65E     07 800F                 2818  CE4       L     FLR,NULL,IRJ      CLEAR CC & LEAVE                              73228160
                                2819  *                                                                               73228170
65F     00 0013                 2820  BRFSULT   L     SRH,MR0           (SRH,SRL)=2ND OP FRACTION                     73228180
660     00 0812                 2821            L     SRL,MR1                                                         73228190
661     00 2006                 2822            L     MR6,MR4           (MR6)=2ND OP EXPONENT                         73228200
662     00 1804                 2823            L     MR4,MR3           (MR4)=2ND OP SIGN & EXPONENT                  73228210
663     F0 0627                 2824            B     FEND              EXIT (P,60)                                   73228220
                                2825  *                                                                               73228230
664     80 0013                 2826  ZRFSULT   LI    SRH,0             CLEAR (SRH,SRL)                               73228240
665     80 0012                 2827            LI    SRL,0                                                           73228250
666     80 0006                 2828            LI    MR6,0             CLEAR RESULT SIGN & EXPONENT                  73228260
667     80 0004                 2829            LI    MR4,0                                                           73228270
668     F0 0627                 2830            B     FEND              EXIT (P,60)                                   73228280
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                        2832  * DROM 2 ENTRY POINT FOR ME,MER                                    73228300
                        2833  *                                                                  73228310
669     88 0609         2834  ME,MER  LI    ARL,'80',CS     (ARL = '8000'                       73228320
66A     30 220A         2835          X     ARH,MR4,ARL     2'S COMP 2ND OP EXPONENT            73228330
66B     30 3206         2836          X     MR6,MR6,ARL     2'S COMP 1ST OP EXPONENT            73228340
66C     40 3726         2837          A     MR6,MR6,ARH,F   ADD EXPONENTS                       73228350
66D     30 3206         2838          X     MR6,MR6,ARL     RESULT BACK TO EXCESS 64            73228360
66E     00 2809         2839          L     ARL,MR5                                             73228370
66F     30 1A04         2840          X     MR4,MR3,ARL     (MR4) HOLDS RESULT SIGN             73228380
670     E1 05D4         2841          BT    V,EXPOUF        OVERFLOW OR UNDERFLOW (P.58)        73228390
                        2842  *                                                                  73228400
671     00 B005         2843          L     MR5,MDR         SAVE LOW 1ST OPERAND                73228410
672     00 0612         2844          L     SRL,MR1                                             73228420
673     00 B249         2845          L     ARL,MDR,SL+CO                                       73228430
674     70 C400         2846          C     UMPY            A LOW * B LOW                       73228440
675     00 980A         2847          L     ARH,SRH         SAVE MS 16 BITS OF RESULT           73228450
676     00 0012         2848          L     SRL,MR0                                             73228460
677     00 2816         2849          L     MDR,MR5                                             73228470
678     00 B249         2850          L     ARL,MDR,SL+CO                                       73228480
679     70 C400         2851          C     UMPY            A LOW * B HIGH                      73228490
67A     40 9743         2852          A     MR3,SRL,ARH,CO  KEEP RUNNING SUM OF                 73228500
67B     40 988A         2853          A     ARH,SRH,NULL,CI PARTIAL PRODUCTS                    73228510
67C     00 1012         2854          L     SRL,MR2         (ARH,MR3)=PARTIAL RESULT            73228520
67D     00 0816         2855          L     MDR,MR1                                             73228530
67E     00 B249         2856          L     ARL,MDR,SL+CO                                       73228540
67F     70 C400         2857          C     UMPY            A HIGH * BLOW                       73228550
680     00 1809         2858          L     ARL,MR3                                             73228560
681     40 9243         2859          A     MR3,SRL,ARL,CO                                      73228570
682     40 9F8A         2860          A     ARH,SRH,ARH,CI  (ARH,MR3)=PARITAL RESULT            73228580
683     00 0012         2861          L     SRL,MR0                                             73228590
684     00 1016         2862          L     MDR,MR2                                             73228600
685     00 B249         2863          L     ARL,MDR,SL+CO                                       73228610
686     70 C400         2864          C     UMPY            A HIGH * B HIGH                     73228620
687     40 9713         2865          A     SRH,SRL,ARH                                         73228630
688     00 1812         2866          L     SRL,MR3                                             73228640
                        2867  *                                                                  73228650
                        2868  *                                                                  73228660
                        2869  * RESULTANT FRACTION IS IN SRH & SRL                              73228670
                        2870  * IF THE MOST SIGNIFICANT HEX DIGIT OF THE PRODUCT                 73228680
                        2871  * IS NON-ZERO, EXPONENT NEEDS NO CORRECTION, SHIFT                 73228690
                        2872  * PRODUCT RIGHT 8 PLACES THEN ROUND.                              73228700
                        2873  * IF THE MOST SIGNIFICANT HEX DIGIT IS ZERO DECREMENT              73228710
                        2874  * EXPONENT BY ONE, SHIFT PRODUCT RIGHT 4 PLACES, AND ROUND.       73228720
                        2875  *                                                                  73228730
                        2876  *                                                                  73228740
689     80 4008         2877          LI    CTR,4           PRESET CTR                          73228750
68A     80 000F         2878          LI    FLR,0                                               73228760
68B     8F 0609         2879          LI    ARL,'F0',CS     (ARL)='F000'                        73228770
68C     10 9A30         2880          N     NULL,SRH,ARL,F  TEST MS 4 PRODUCT BITS              73228780
68D     E0 C692         2881          BT    G+L,NOCOR       BRANCH IF NOT ZERO (P.64)           73228790
68E     80 2008         2882          LI    CTR,2                                               73228800
68F     80 2609         2883          LI    ARL,2,CS                                            73228810
690     50 3246         2884          S     MR6,MR6,ARL,CO  DECREMENT EXPONENT                  73228820
691     E2 0505         2885          BT    C,EXPUFZ        EXPONENT UNDERFLOW (P.58)           73228830
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                        2886  *
692     80 000F         2887  NOCOR     LI      FLR,0                                                   73228840
                        2888  *                                                                         73228850
693     70 0008         2889  CORRECT   C       RPT             SHIFT RIGHT 2(CTR) TIMES                73228860
694     70 0C40         2890            C       SR2+C0                                                  73228870
695     40 90F2         2891            A       SRL,SRL,NULL,CI+CO+F ROUND                              73228880
696     40 98F3         2892            A       SRH,SRH,NULL,CI+CO+F                                    73228890
697     E0 C634         2893            BT      G+L,CARRYCK     CHECK CARRY IF NOT ZERO (P.61)          73228900
698     80 0004         2894            LI      MR4,0           ELSE SET RESULT SIGN =0                 73228910
699     80 0006         2895            LI      MR6,0           RESULT EXPONENT = 0                     73228920
69A     F0 0627         2896            B       FEND            TAKE COMMON EXIT (P.60)                 73228930
                                                                                                        73228940
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                                2898  * DROM 2 ENTRY POINT FOR DE,DER                                          73228960
                                2899  *                                                                       73228970
69B  88 0609                    2900  DE.DER   LI    ARL,'80',CS     (ARL)='8000'                            73228980
69C  88 0609                    2901           LI    ARL,'80',CS     (ARL)='8000'                            73228990
69D  30 220A                    2902           X     ARH,MR4,ARL     2'S COMP 2ND OP EXPONENT                73229000
69E  30 3206                    2903           X     MR6,MR6,ARL     2'S COMP 1ST OP EXPONENT                73229010
69F  50 3726                    2904           S     MR6,MR6,ARH,F   SUBTRACT EXPONENTS                      73229020
6A0  00 280A                    2905           L     ARH,MR5                                                 73229030
6A1  30 1F04                    2906           X     MR4,MR3,ARH     (MR4)HOLDS RESULT SIGN                  73229040
6A2  00 000A                    2907           L     ARH,MR0                                                 73229050
6A3  50 8750                    2908           S     NULL,NULL,ARH,CO TEST FOR ZERO DIVISOR                  73229060
6A4  F2 0500                    2909           BF    C,DIVZRO        FAULT IF ZERO (P.58)                    73229070
6A5  E1 05D4                    2910           BT    V,EXPOUF        OVERFLOW OR UNDERFLOW (P.58)            73229080
6A6  30 3206                    2911           X     MR6,MR6,ARL     EXPONENT BACK TO EXCESS 64              73229090
6A7  00 0600                    2912           L     MR0,MR0,CS                                              73229100
6A8  00 0E09                    2913           L     ARL,MR1,CS                                              73229110
6A9  9F F20A                    2914           NI    ARH,'FF',ARL                                            73229120
6AA  20 0700                    2915           O     MR0,MR0,ARH                                             73229130
6AB  00 040A                    2916           L     ARH,MR0,SR      (ARH)=MS 1K BITS OF FRACTION B          73229140
6AC  80 1609                    2917           LI    ARL,'01',CS                                             73229150
6AD  AF F209                    2918           OI    ARL,'FF',ARL    (ARL)='01FF'                            73229160
6AE  10 0A01                    2919           N     MR1,MR1,ARL     (MR1)=LS * BITS OF FRACTION B           73229170
                                2920  *                                                                       73229180
                                2921  * THE SECOND OPERAND DIVISOR HAS BEEN SEPARATED                         73229190
                                2922  * INTO TWO PARTS: BHI (15 BITS) AND BLO (9 BITS)                        73229200
                                2923  * (ARH)=BHI    (WITH SCAL FACTOR=2**-15)                                 73229210
                                2924  * (MR1)=BLO    (WITH SCALE FACTOR=2**-24)                                73229220
                                2925  *                                                                       73229230
6AF  00 1013                    2926           L     SRH,MR2         (SRH,SRL)=DIVIDEND FRACTION             73229240
6B0  00 B012                    2927           L     SRL,MDR                                                 73229250
6B1  50 8709                    2928           S     ARL,NULL,ARH    NARL)=2'S COMP OF BHI                   73229260
6B2  81 0008                    2929           LI    CTR,16                                                  73229270
6B3  70 2200                    2930           C     DIV                                                     73229280
6B4  00 9003                    2931           L     MR3,SRL         (MR3)=QUOTIENT OF A/BHI                 73229290
                                2932  *                               SCALE FACTOR= 2**-9                     73229300
6B5  00 8012                    2933           L     SRL,NULL        (SRH,SRL)=(2**15)*REMAINDER             73229310
6B6  70 0800                    2934           C     SR1             SCALE RIGHT                             73229320
6B7  50 8709                    2935           S     ARL,NULL,ARH                                            73229330
6B8  81 0008                    2936           LI    CTR,16                                                  73229340
6B9  70 2200                    2937           C     DIV                                                     73229350
6BA  00 9005                    2938           L     MR5,SRL         (MR5)=LS QUOTIENT OF A/BHI              73229360
                                2939  *                               SCALE FACTOR=2**-24                     73229370
                                2940  *                               IGNORE THIS REMAINDER                   73229380
6BB  00 0813                    2941           L     SRH,MR1         (SRH,SRL) = BLO*2**15                   73229390
6BC  00 8012                    2942           L     SRL,NULL                                                73229400
6BD  50 8709                    2943           S     ARL,NULL,ARH                                            73229410
6BE  81 0008                    2944           LI    CTR,16                                                  73229420
6BF  70 2200                    2945           C     DIV             (SRL)=BLO/BHI                           73229430
6C0  00 9002                    2946           L     MR2,SRL         CORRECTION QUOTIENT HAS                 73229440
6C1  00 9016                    2947           L     MDR,SRL         SCALE FACTOR= 2**25                     73229450
6C2  00 B249                    2948           L     ARL,MDR,SL+CO                                           73229460
6C3  70 C400                    2949           C     UMPY            SQUARE CORRECTION QUOTIENT              73229470
                                2950  *                               (SRH,SRL)HAS SCALE FACTOR               73229480
                                2951  *                               EQUAL TO 2**-50, ADJUST BY              73229490
```

```
6C4  00 9E09  2952          L     ARL,SRH,CS        SHIFTING RIGHT 9 PLACES          73229500
6C5  9F F212  2953          NI    SRL,'FF',ARL      IGNORE LS 16 BITS IN SRL         73229510
6C6  00 9409  2954          L     ARL,SRL,SR        SCALE FACTOR= 2**-25             73229520
6C7  50 1202  2955          S     MR2,MR2,ARL       SUBTRACT FROM ORIGINAL           73229530
6C8  00 1012  2956          L     SRL,MR2           CORRECTION QUOTIENT = D          73229540
6C9  00 2816  2957          L     MDR,MR5           (MDR)=LS QUOTIENT                73229550
6CA  00 B249  2958          L     ARL,MDR,SL+CO                                      73229560
6CB  70 C400  2959          C     UMPY              (SRH,SRL)=D*LS QUOTIENT          73229570
6CC  00 9252  2960          L     SRL,SRL,SL+CO     SHIFT RIGHT 15 PLACES            73229580
6CD  00 9AC1  2961          L     MR1,SRH,SL+CI+CO                                   73229590
6CE  40 808A  2962          A     ARH,NULL,NULL,CI  RESULT TO (ARH,ARL)              73229600
6CF  00 1012  2963          L     SRL,MR2                                            73229610
6D0  00 1816  2964          L     MDR,MR3                                            73229620
6D1  00 B249  2965          L     ARL,MDR,SL+CO                                      73229630
6D2  70 C400  2966          C     UMPY              SCALE FACTOR NOW 2**-34          73229640
6D3  00 0809  2967          L     ARL,MR1                                            73229650
6D4  40 9252  2968          A     SRL,SRL,ARL,CO    ADD CORRECTION QUOTIENT          73229660
6D5  40 9F93  2969          A     SRH,SRH,ARH,CI                                     73229670
6D6  80 4008  2970          LI    CTR,4                                              73229680
6D7  70 0008  2971          C     RPT                                                73229690
6D8  70 0C00  2972          C     SR2               SHIFT RIGHT 9 PLACES             73229700
6D9  00 9C4A  2973          L     ARH,SRH,SR+CO     ADJUSTING THE SCALE FACTOR       73229710
6DA  00 9489  2974          L     ARL,SRL,SR+CI                                      73229720
6DB  00 2A05  2975          L     MR5,MR5,SL                                         73229730
6DC  50 2A52  2976          S     SRL,MR5,ARL,CO    FINAL RESULT FORMED              73229740
6DD  50 1F93  2977          S     SRH,MR3,ARH,CI    SCALE FACTOR = 2**-25            73229750
              2978  *                                                                73229760
              2979  * NEED TO CORRECT QUOTIENT TO 2**-24                            73229770
              2980  * SHIFT RIGHT 1 PLACE IF SRH 0:6=0                              73229780
              2981  * SHIFT RIGHT 5 PLACES IF SRH 0:6 NOT ZERO                      73229790
              2982  * THEN INCREMENT EXPONENT BY ONE                                73229800
              2983  *                                                                73229810
6DE  80 000F  2984          LI    FLR,0                                              73229820
6DF  8F E609  2985          LI    ARL,'FE',CS       (ARL)='FE00'                     73229830
6E0  80 0008  2986          LI    CTR,0                                              73229840
6E1  10 9A30  2987          N     NULL,SRH,ARL,F    TEST BITS 0 THROUGH 6            73229850
6E2  F0 C6E7  2988          BF    6+L,NOCOR1        NO CORRECTION IF ZERO            73229860
6E3  80 2008  2989          LI    CTR,2                                              73229870
6E4  80 2609  2990          LI    ARL,'02',CS       (ARL)='0200'                     73229880
6E5  40 3246  2991          A     MR6,MR6,ARL,CO    INCREMENT EXPONENT               73229890
6E6  E2 05DD  2992          BT    C,EXPOF           EXPONENT OVERFLOW (P'68)         73229900
6E7  80 000F  2993  NOCOR1  LI    FLR,0             CLEAR FLAGS                      73229910
6E8  70 0840  2994          C     SR1,CO            DO ONE SHIFT HERE                73229920
6E9  F0 0693  2995          B     CORRECT           FINISH CORRECTION (P'64)         73229930
              2996  *                               THEN ROUND RESULT                73229940
              2997          ENDC                                                     73229950
              2998  *                                                                73229960
              2999  *                                                                73229970
              3000  *                                                                73229980
```

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6EA                     3002          IFP   HWFLPT                                    73230000
6EA                     3003          ORG   '700'                                     73230010
                        3006          ENDC                                            73230040
                        3007  *                                                       73230050
                        3008  *                                                       73230060
                        3009  *                                                       73230070
                        3010  *                                                       73230080
                        3011  *                                                       73230090
                        3012          DCX   000000                                    73230100
700     00 0000         3013          DCX   2D6000                                    73230110
701     2D 6000         3014          DCX   2B8000                                    73230120
702     2B 8000         3015          DCX   2C3000                                    73230130
703     2C 3000         3016          DCX   21C000                                    73230140
704     21 C000         3017          DCX   212000                                    73230150
705     21 2000         3018          DCX   21E000                                    73230160
706     21 E000         3019          DCX   220000                                    73230170
707     22 0000         3020          DCX   1B7000                                    73230180
708     1B 7000         3021          DCX   300000                                    73230190
709     30 0000         3022          DCX   2EA000                                    73230200
70A     2E A000         3023          DCX   2FA000                                    73230210
70B     2F A000         3024          DCX   341000                                    73230220
70C     34 1000         3025          DCX   38A000                                    73230230
70D     38 A000         3026          DCX   000000                                    73230240
70E     00 0000         3027          DCX   000000                                    73230250
70F     00 0000         3028  *                                                       73230260
                        3029          DCX   19B22A                                    73230270
710     19 B22A         3030          DCX   19B224                                    73230280
711     19 B224         3031          DCX   3DD000                                    73230290
712     3D D000         3032          DCX   000000                                    73230300
713     00 0000         3033          DCX   000000                                    73230310
714     00 0000         3034          DCX   000000                                    73230320
715     00 0000         3035          DCX   000000                                    73230330
716     00 0000         3036          DCX   000000                                    73230340
717     00 0000         3037          DCX   BF3000                                    73230350
718     BF 3000         3038          DCX   000000                                    73230360
719     00 0000         3039          DCX   000000                                    73230370
71A     00 0000         3040          DCX   000000                                    73230380
71B     00 0000         3041          DCX   305000                                    73230390
71C     30 5000         3042          DCX   34A000                                    73230400
71D     34 A000         3043          DCX   000000                                    73230410
71E     00 0000         3044          DCX   000000                                    73230420
71F     00 0000
```

SYMBOLIC ENTRY-POINT DROM1,DROM2 — LISTING PAGE REFERENCE

- -	2	-
BALR -	31	-
BTCR -	30	-
BFCR -	30	-
NR -	24	-
CLR -	24	-
OR -	25	-
XR -	25	-
LR -	21	-
CR -	33	-
AR -	32	-
SR -	32	-
MHR -	34	-
DHR -	37	-
- -	2	-
- -	2	-
SRLLS SRLS	19	25
SRLLS SLLS	19	25
CHVR -	39	-
- -	2	-
- -	2	-
- -	2	-
- -	2	-
- -	2	-
LPSWR -	40	-
- -	2	-
- -	2	-
- -	2	-
MR -	35	-
DR -	35	-
- -	2	-
- -	2	-

		3046 *			SYMBOLIC		LISTING		73230440
		3047 *			ENTRY-POINT		PAGE		73230450
		3048 *			DROM1,DROM2		REFERENCE		73230460
		3049 *							73230470
720	2B C2CA	3050	DCX	2BC2CA	BTBS	BBS	30	30	73230480
721	2B C2CF	3051	DCX	2BC2CF	BTFS	BFS	30	30	73230490
722	2C 72CA	3052	DCX	2C72CA	BFBS	BBS	30	30	73230500
723	2C 72CF	3053	DCX	2C72CF	BFFS	BFS	30	30	73230510
724	1B 9000	3054	DCX	1B9000	LIS	-	21	-	73230520
725	1B B000	3055	DCX	1BB000	LCS	-	21	-	73230530
726	2E C000	3056	DCX	2EC000	AIS	-	32	-	73230540
727	2F C000	3057	DCX	2FC000	SIS	-	32	-	73230550
728		3058	IFZ	HWFLPT					73230560
728	55 361D	3059	DCX	55361D	LER	LE,LERX	53	60	73230570
729	58 1646	3060	DCX	581646	CER	CE,CER	54	62	73230580
72A	58 1602	3061	DCX	581602	AER	AE,AER	54	59	73230590
72B	58 1600	3062	DCX	581600	SER	SE,SER	54	59	73230600
72C	58 1669	3063	DCX	581669	MER	ME,MER	54	63	73230610
72D	58 169C	3064	DCX	58169C	DER	DE,DER	54	65	73230620
72E	59 2000	3065	DCX	592000	FXR	*	56	-	73230630
72F	5B 6000	3066	DCX	5B6000	FLR	*	57	-	73230640
		3076	ENDC						73230740
		3077 *							73230750
730	4C F000	3078	DCX	4CF000	MPBSR	-	48	-	73230760
731	00 0000	3079	DCX	000000	-	-	2	-	73230770
732	4C 02CC	3080	DCX	4C02CC	PBR	NBR	47	30	73230780
733	00 0000	3081	DCX	000000	-	-	2	-	73230790
734	1F 1000	3082	DCX	1F1000	EXHR		23	-	73230800
735	00 0000	3083	DCX	000000	-	-	2	-	73230810
736	00 0000	3084	DCX	000000	-	-	2	-	73230820
737	00 0000	3085	DCX	000000	-	-	2	-	73230830
738	55 3000	3086	DCX	553000	LDR	-	53	-	73230840
739	58 1000	3087	DCX	581000	CDR	-	54	-	73230850
73A	58 1000	3088	DCX	581000	ADR	-	54	-	73230860
73B	58 1000	3089	DCX	581000	SDR	-	54	-	73230870
73C	58 1000	3090	DCX	581000	MDR	-	54	-	73230880
73D	58 1000	3091	DCX	581000	DDR	-	54	-	73230890
73E	5D 5000	3092	DCX	5D5000	FXDR	-	58	-	73230900
73F	5B 65D0	3093	DCX	5B65D0	FLDR	FLDR,D2	57	57	73230910

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                                3095  *                                                                    73230930
                                3096  *                                                                    73230940
                                3097  *                                                                    73230950
                                3098  *                                                                    73230960
                                3099                DCX   1F9000    STH   -     23  -                      73230970
740   1F 9000                   3100                DCX   2D2000    BAL   -     31  -                      73230980
741   2D 2000                   3101                DCX   2B4000    BTC   -     30  -                      73230990
742   2B 4000                   3102                DCX   2BF000    BFC   -     30  -                      73231000
743   2B F000                   3103                DCX   18D21C    RXH   NH    19 24                      73231010
744   18 D21C                   3104                DCX   18D212    RXH   CLH   19 24                      73231020
745   18 D212                   3105                DCX   18D21E    RXH   OH    19 25                      73231030
746   18 D21E                   3106                DCX   18D220    RXH   XH    19 25                      73231040
747   18 D220                   3107                DCX   18D1B7    RXH   LH    19 21                      73231050
748   18 D1B7                   3108                DCX   18D300    RXH   CH    19 33                      73231060
749   18 D300                   3109                DCX   18D2EA    RXH   AH    19 32                      73231070
74A   18 D2EA                   3110                DCX   18D2FA    RXH   SH    19 32                      73231080
74B   18 D2FA                   3111                DCX   18D341    RXH   MH    19 34                      73231090
74C   18 D341                   3112                DCX   18D38A    RXH   DH    19 37                      73231100
74D   18 D38A                   3113                DCX   000000    -     -      2  -                      73231110
74E   00 0000                   3114                DCX   000000    -     -      2  -                      73231120
74F   00 0000                   3115  *                                                                    73231130
                                3116                DCX   1F5000    ST    -     23  -                      73231140
750   1F 5000                   3117                DCX   2EF000    AM    -     32  -                      73231150
751   2E F000                   3118                DCX   000000    -     -      2  -                      73231160
752   00 0000                   3119                DCX   000000    -     -      2  -                      73231170
753   00 0000                   3120                DCX   19121C    RXF   N     19 24                      73231180
754   19 121C                   3121                DCX   191212    RXF   CL    19 24                      73231190
755   19 1212                   3122                DCX   19121E    RXF   O     19 25                      73231200
756   19 121E                   3123                DCX   191220    RXF   X     19 25                      73231210
757   19 1220                   3124                DCX   1911B7    RXF   L     19 21                      73231220
758   19 11B7                   3125                DCX   191300    RXF   C     19 33                      73231230
759   19 1300                   3126                DCX   1912EA    RXF   A     19 32                      73231240
75A   19 12EA                   3127                DCX   1912FA    RXF   S     19 32                      73231250
75B   19 12FA                   3128                DCX   191305    RXF   M     19 33                      73231260
75C   19 1305                   3129                DCX   19134A    RXF   D     19 35                      73231270
75D   19 134A                   3130                DCX   251000    CRC12 -     27  -                      73231280
75E   25 1000                   3131                DCX   258000    CRC16 -     27  -                      73231290
75F   25 8000
```

		3133 *			SYMBOLIC	LISTING			73231310
		3134 *			ENTRY-POINT	PAGE			73231320
		3135 *			DROM1,DROM2	REFERENCE			73231330
		3136 *							73231340
760		3137	IFZ	HWFLPT					73231350
760	57 B573	3138	DCx	57B573	STE	STE,D2	54	54	73231360
		3141	ENDC						73231390
761	2F 6000	3142	DCx	2F6000	AHM	"	32	"	73231400
762	4B 9000	3143	DCx	4B9000	PB	"		"	73231410
763	1C 4000	3144	DCx	1C4000	LRA	"	21	"	73231420
764	27 8280	3145	DCx	278280	ATL	ATL,D2	28	28	73231430
765	27 8287	3146	DCx	278287	ABL	ABL,D2	28	28	73231440
766	29 429C	3147	DCx	29429C	RTL	RTL,D2	29	29	73231450
767	29 42A4	3148	DCx	2942A4	RBL	RBL,D2	29	29	73231460
768		3149	IFZ	HWFLPT					73231470
768	55 A61D	3150	DCx	55A61D	LE	LE,LERx	53	60	73231480
769	58 C646	3151	DCx	58C646	CE	CE,CER	55	62	73231490
76A	58 C602	3152	DCx	58C602	AE	AE,AER	55	59	73231500
76B	58 C600	3153	DCx	58C600	SE	SE,SER	55	59	73231510
76C	58 C669	3154	DCx	58C669	ME	ME,MER	55	63	73231520
76D	58 C69C	3155	DCx	58C69C	DE	DE,DER	55	65	73231530
		3163	ENDC						73231610
76E	00 0000	3164	DCx	000000	"	"	2	"	73231620
76F	00 0000	3165	DCx	000000	"	"	2	"	73231630
		3166 *							73231640
770	55 F000	3167	DCx	55F000	STD	"	55	"	73231650
771		3168	IFZ	HWFLPT					73231660
771	56 5570	3169	DCx	565570	STME	STME,D2	53	54	73231670
772	56 556A	3170	DCx	56556A	LME	LME,D2	53	54	73231680
		3174	ENDC						73231720
773	18 D1E0	3175	DCx	18D1E0	RXH	LHL	19	22	73231730
774	1A 824A	3176	DCx	1A824A	XBIT	TBT	20	26	73231740
775	1A 824B	3177	DCx	1A824B	XBIT	SBT	20	27	73231750
776	1A 824F	3178	DCx	1A824F	XBIT	RBT	20	27	73231760
777	1A 824D	3179	DCx	1A824D	XBIT	CBT	20	27	73231770
778	58 6554	3180	DCx	586554	LD	LOADSDMD	55	53	73231780
779	58 6554	3181	DCx	586554	CD	LOADSDMD	55	53	73231790
77A	58 6554	3182	DCx	586554	AD	LOADSDMD	55	53	73231800
77B	58 6554	3183	DCx	586554	SD	LOADSDMD	55	53	73231810
77C	58 6554	3184	DCx	586554	MD	LOADSDMD	55	53	73231820
77D	58 6554	3185	DCx	586554	DD	LOADSDMD	55	53	73231830
77E	56 5575	3186	DCx	565575	STMD	STMD,D2	53	54	73231840
77F	56 556C	3187	DCx	56556C	LMD	LMD,D2	53	54	73231850

						SYMBOLIC ENTRY-POINT DROM1,DROM2		LISTING PAGE REFERENCE		
		3189 *								73231870
		3190 *								73231880
		3191 *								73231890
		3192 *								73231900
780		3193		DC	16					73231910
780	00 0000	3194		DCX	000000	-	-	2	-	73231920
781	00 0000	3194		DCX	000000	-	-	2	-	73231920
782	00 0000	3194		DCX	000000	-	-	2	-	73231920
783	00 0000	3194		DCX	000000	-	-	2	-	73231920
784	00 0000	3194		DCX	000000	-	-	2	-	73231920
785	00 0000	3194		DCX	000000	-	-	2	-	73231920
786	00 0000	3194		DCX	000000	-	-	2	-	73231920
787	00 0000	3194		DCX	000000	-	-	2	-	73231920
788	00 0000	3194		DCX	000000	-	-	2	-	73231920
789	00 0000	3194		DCX	000000	-	-	2	-	73231920
78A	00 0000	3194		DCX	000000	-	-	2	-	73231920
78B	00 0000	3194		DCX	000000	-	-	2	-	73231920
78C	00 0000	3194		DCX	000000	-	-	2	-	73231920
78D	00 0000	3194		DCX	000000	-	-	2	-	73231920
78E	00 0000	3194		DCX	000000	-	-	2	-	73231920
78F	00 0000	3194		DCX	000000	-	-	2	-	73231920
		3195 *								73231930
790	23 4000	3196		DCX	234000	SRHLS	-	26	-	73231940
791	23 0000	3197		DCX	230000	SLHLS	-	26	-	73231950
792	20 C000	3198		DCX	20C000	STBR	-	24	-	73231960
793	1E E000	3199		DCX	1EE000	LBR	-	23	-	73231970
794	1F 3000	3200		DCX	1F3000	EXBR	-	23	-	73231980
795	C0 0000	3201		DCX	C00000	EPSR	-	40	-	73231990
796	C6 3469	3202		DCX	C63469	WBR	LOOPW	44	44	73232000
797	C6 3475	3203		DCX	C63475	RBR	LOOPR	44	44	73232010
798	C5 9C55	3204		DCX	C59C55	WHR	WHH	44	43	73232020
799	C3 FC41	3205		DCX	C3FC41	RHR	RHRH	43	43	73232030
79A	C4 E000	3206		DCX	C4E000	WDR	-	43	-	73232040
79B	C3 2000	3207		DCX	C32000	RDR	-	42	-	73232050
79C	00 0000	3208		DCX	000000	-	-	2	-	73232060
79D	C2 2000	3209		DCX	C22000	SSR	-	42	-	73232070
79E	C2 A000	3210		DCX	C2A000	OCR	-	42	-	73232080
79F	00 0000	3211		DCX	000000	-	-	2	-	73232090

DROM1 AND DROM2 73229

SYMBOLIC ENTRY-POINT DROM1,DROM2 LISTING PAGE REFERENCE

```
                                3213  *                                                                  73232110
                                3214  *                                                                  73232120
                                3215  *                                                                  73232130
                                3216  *                                                                  73232140
7A0                             3217        DO    16                                                     73232150
7A0  00 0000                    3218        DCX   000000    -  -  2  -                                     73232160
7A1  00 0000                    3218        DCX   000000    -  -  2  -                                     73232160
7A2  00 0000                    3218        DCX   000000    -  -  2  -                                     73232160
7A3  00 0000                    3218        DCX   000000    -  -  2  -                                     73232160
7A4  00 0000                    3218        DCX   000000    -  -  2  -                                     73232160
7A5  00 0000                    3218        DCX   000000    -  -  2  -                                     73232160
7A6  00 0000                    3218        DCX   000000    -  -  2  -                                     73232160
7A7  00 0000                    3218        DCX   000000    -  -  2  -                                     73232160
7A8  00 0000                    3218        DCX   000000    -  -  2  -                                     73232160
7A9  00 0000                    3218        DCX   000000    -  -  2  -                                     73232160
7AA  00 0000                    3218        DCX   000000    -  -  2  -                                     73232160
7AB  00 0000                    3218        DCX   000000    -  -  2  -                                     73232160
7AC  00 0000                    3218        DCX   000000    -  -  2  -                                     73232160
7AD  00 0000                    3218        DCX   000000    -  -  2  -                                     73232160
7AE  00 0000                    3218        DCX   000000    -  -  2  -                                     73232160
7AF  00 0000                    3218        DCX   000000    -  -  2  -                                     73232160
                                3219  *                                                                  73232170
7B0                             3220        DO    16                                                     73232180
7B0  00 0000                    3221        DCX   000000    -  -  2  -                                     73232190
7B1  00 0000                    3221        DCX   000000    -  -  2  -                                     73232190
7B2  00 0000                    3221        DCX   000000    -  -  2  -                                     73232190
7B3  00 0000                    3221        DCX   000000    -  -  2  -                                     73232190
7B4  00 0000                    3221        DCX   000000    -  -  2  -                                     73232190
7B5  00 0000                    3221        DCX   000000    -  -  2  -                                     73232190
7B6  00 0000                    3221        DCX   000000    -  -  2  -                                     73232190
7B7  00 0000                    3221        DCX   000000    -  -  2  -                                     73232190
7B8  00 0000                    3221        DCX   000000    -  -  2  -                                     73232190
7B9  00 0000                    3221        DCX   000000    -  -  2  -                                     73232190
7BA  00 0000                    3221        DCX   000000    -  -  2  -                                     73232190
7B8  00 0000                    3221        DCX   000000    -  -  2  -                                     73232190
7BC  00 0000                    3221        DCX   000000    -  -  2  -                                     73232190
7BD  00 0000                    3221        DCX   000000    -  -  2  -                                     73232190
7BE  00 0000                    3221        DCX   000000    -  -  2  -                                     73232190
7BF  00 0000                    3221        DCX   000000    -  -  2  -                                     73232190
```

		3223 *				SYMBOLIC		LISTING		73232210
		3224 *				ENTRY-POINT		PAGE		73232220
		3225 *				DROM1,DROM2		REFERENCE		73232230
		3226 *								73232240
7C0	2D A2E4	3227		DCx	2DA2E4	BXH	BXH,D2	31	31	73232250
7C1	2D A2E7	3228		DCx	2DA2E7	BXLE	BXLE,D2	31	31	73232260
7C2	BE B000	3229		DCx	BEB000	LPSW	-	40	-	73232270
7C3	19 6222	3230		DCx	196222	RI1	THI	19	25	73232280
7C4	19 621C	3231		DCx	19621C	RI1	NHI	19	24	73232290
7C5	19 6212	3232		DCx	196212	RI1	CLHI	19	24	73232300
7C6	19 621E	3233		DCx	19621E	RI1	OHI	19	25	73232310
7C7	19 6220	3234		DCx	196220	RI1	XHI	19	25	73232320
7C8	19 6187	3235		DCx	1961B7	RI1	LHI	19	21	73232330
7C9	19 6300	3236		DCx	196300	RI1	CHI	19	33	73232340
7CA	19 62EA	3237		DCx	1962EA	RI1	AHI	19	32	73232350
7CB	19 62FA	3238		DCx	1962FA	RI1	SHI	19	32	73232360
7CC	1A 6235	3239		DCx	1A6235	SLRH	SRHL	20	26	73232370
7CD	1A 6231	3240		DCx	1A6231	SLRH	SLHL	20	26	73232380
7CE	1A 63D9	3241		DCx	1A63D9	SLRH	SRHA	20	38	73232390
7CF	1A 63C9	3242		DCx	1A63C9	SLRH	SLHA	20	38	73232400
		3243 *								73232410
7D0	20 0000	3244		DCx	200000	STM	-	23	-	73232420
7D1	1E 2000	3245		DCx	1E2000	LM	-	22	-	73232430
7D2	20 7000	3246		DCx	207000	STB	-	24	-	73232440
7D3	1E A000	3247		DCx	1EA000	LB	-	23	-	73232450
7D4	21 4000	3248		DCx	214000	CLB	-	24	-	73232460
7D5	C7 F475	3249		DCx	C7F475	AL	LOOPR	45	44	73232470
7D6	C5 B469	3250		DCx	C5B469	WB	LOOPW	44	44	73232480
7D7	C5 B475	3251		DCx	C5B475	RB	LOOPR	44	44	73232490
7D8	C5 1C55	3252		DCx	C51C55	WH	WHM,WHB	43	43	73232500
7D9	C3 6C39	3253		DCx	C36C39	RH	RHM,RHB	44	44A45	73232510
7DA	C4 7000	3254		DCx	C47000	WD	-	43	-	73232520
7DB	C2 D000	3255		DCx	C2D000	RD	-	42	-	73232530
7DC	00 0000	3256		DCx	000000	-	-	2	-	73232540
7DD	C1 D000	3257		DCx	C1D000	SS	-	42	-	73232550
7DE	C2 6000	3258		DCx	C26000	OC	-	42	-	73232560
7DF	00 0000	3259		DCx	000000	-	-	2	-	73232570

		3261	*			SYMBOLIC		LISTING		73232590
		3262	*			ENTRY-POINT		PAGE		73232600
		3263	*			DROM1,DROM2		REFERENCE		73232610
		3264	*							73232620
7E0	24 5000	3265		DCX	245000	TS	-	26	-	73232630
7E1	40 7409	3266		DCX	407409	SVC	SVC,D2	40	40	73232640
7E2	99 6403	3267		DCX	996403	RI1	SINT	19	40	73232650
7E3	C9 6000	3268		DCX	C96000	SCP	-	46	-	73232660
7E4	00 0000	3269		DCX	000000	-	-	2	-	73232670
7E5	00 0000	3270		DCX	000000	-	-	2	-	73232680
7E6	18 F000	3271		DCX	18F000	LA	-	21	-	73232690
7E7	26 C000	3272		DCX	26C000	TLATE	-	28	-	73232700
7E8	00 0000	3273		DCX	000000	-	-	2	-	73232710
7E9	00 0000	3274		DCX	000000	-	-	2	-	73232720
7EA	1A 323F	3275		DCX	1A323F	RLRR	RRL	20	26	73232730
7EB	1A 3239	3276		DCX	1A3239	RLRR	RLL	20	26	73232740
7EC	19 E22A	3277		DCX	19E22A	SRLL	SRL	20	25	73232750
7ED	19 E224	3278		DCX	19E224	SRLL	SLL	20	25	73232760
7EE	38 C3CF	3279		DCX	38C3CF	SLRA	SRA	38	38	73232770
7EF	38 C3BF	3280		DCX	38C3BF	SLRA	SLA	38	38	73232780
		3281	*							73232790
7F0	00 0000	3282		DCX	000000	-	-	2	-	73232800
7F1	00 0000	3283		DCX	000000	-	-	2	-	73232810
7F2	00 0000	3284		DCX	000000	-	-	2	-	73232820
7F3	19 8222	3285		DCX	198222	RI2	TI	19	25	73232830
7F4	19 821C	3286		DCX	19821C	RI2	NI	19	24	73232840
7F5	19 8212	3287		DCX	198212	RI2	CLI	19	24	73232850
7F6	19 821E	3288		DCX	19821E	RI2	OI	19	25	73232860
7F7	19 8220	3289		DCX	198220	RI2	XI	19	25	73232870
7F8	19 81B7	3290		DCX	1981B7	RI2	LI	19	21	73232880
7F9	19 8300	3291		DCX	198300	RI2	CI	19	33	73232890
7FA	19 82EA	3292		DCX	1982EA	RI2	AI	19	32	73232900
7FB	19 82FA	3293		DCX	1982FA	RI2	SI	19	32	73232910
7FC	00 0000	3294		DCX	000000	-	-	2	-	73232920
7FD	00 0000	3295		DCX	000000	-	-	2	-	73232930
7FE	00 0000	3296		DCX	000000	-	-	2	-	73232940
7FF	00 0000	3297		DCX	000000	-	-	2	-	73232950

ILLEGAL INSTRUCTION DETECT ROM 73232

```
800  F0 0000  3299  DCX  F00000,000000,000000,000000  00  73232970
801  00 0000
802  00 0000
803  00 0000
804  00 0000  3300  DCX  000000,000000,000000,000000  73232980
805  00 0000
806  00 0000
807  00 0000
808  00 0000  3301  DCX  000000,000000,000000,000000  73232990
809  00 0000
80A  00 0000
80B  00 0000
80C  00 0000  3302  DCX  000000,000000,F00000,F00000  73233000
80D  00 0000
80E  F0 0000
80F  F0 0000
810  00 0000  3303  DCX  000000,000000,000000,F00000  10  73233010
811  00 0000
812  00 0000
813  F0 0000
814  F0 0000  3304  DCX  F00000,F00000,F00000,F00000  73233020
815  F0 0000
816  F0 0000
817  F0 0000
818  00 0000  3305  DCX  000000,F00000,F00000,F00000  73233030
819  F0 0000
81A  F0 0000
81B  F0 0000
81C  00 0000  3306  DCX  000000,000000,F00000,F00000  73233040
81D  00 0000
81E  F0 0000
81F  F0 0000
820  00 0000  3307  DCX  000000,000000,000000,000000  20  73233050
821  00 0000
822  00 0000
823  00 0000
824  00 0000  3308  DCX  000000,000000,000000,000000  73233060
825  00 0000
826  00 0000
827  00 0000
828  90 0000  3309  DCX  900000,900000,900000,900000  73233070
829  90 0000
82A  90 0000
82B  90 0000
82C  90 0000  3310  DCX  900000,900000,900000,900000  73233080
82D  90 0000
82E  90 0000
82F  90 0000
```

ILLEGAL INSTRUCTION DETECT ROM 73232

830	70 0000	3312	DCX	700000,F00000,700000,F00000 30	73233100
831	F0 0000				
832	70 0000				
833	F0 0000				
834	00 0000	3313	DCX	000000,F00000,F00000,F00000	73233110
835	F0 0000				
836	F0 0000				
837	F0 0000				
838	B0 0000	3314	DCX	B00000,B00000,B00000,B00000	73233120
839	B0 0000				
83A	B0 0000				
83B	B0 0000				
83C	B0 0000	3315	DCX	B00000,B00000,B00000,B00000	73233130
83D	B0 0000				
83E	B0 0000				
83F	B0 0000				
840	00 0000	3316	DCX	000000,000000,000000,000000 40	73233140
841	00 0000				
842	00 0000				
843	00 0000				
844	00 0000	3317	DCX	000000,000000,000000,000000	73233150
845	00 0000				
846	00 0000				
847	00 0000				
848	00 0000	3318	DCX	000000,000000,000000,000000	73233160
849	00 0000				
84A	00 0000				
84B	00 0000				
84C	00 0000	3319	DCX	000000,000000,F00000,F00000	73233170
84D	00 0000				
84E	F0 0000				
84F	F0 0000				
850	00 0000	3320	DCX	000000,000000,F00000,F00000 50	73233180
851	00 0000				
852	F0 0000				
853	F0 0000				
854	00 0000	3321	DCX	000000,000000,000000,000000	73233190
855	00 0000				
856	00 0000				
857	00 0000				
858	00 0000	3322	DCX	000000,000000,000000,000000	73233200
859	00 0000				
85A	00 0000				
85B	00 0000				
85C	00 0000	3323	DCX	000000,000000,000000,000000	73233210
85D	00 0000				
85E	00 0000				
85F	00 0000				

860	90 0000	3325	DCX	900000,000000,700000,000000 60	73233230
861	00 0000				
862	70 0000				
863	00 0000				
864	00 0000	3326	DCX	000000,000000,000000,000000	73233240
865	00 0000				
866	00 0000				
867	00 0000				
868	90 0000	3327	DCX	900000,900000,900000,900000	73233250
869	90 0000				
86A	90 0000				
86B	90 0000				
86C	90 0000	3328	DCX	900000,900000,F00000,F00000	73233260
86D	90 0000				
86E	F0 0000				
86F	F0 0000				
870	B0 0000	3329	DCX	B00000,900000,900000,000000 70	73233270
871	90 0000				
872	90 0000				
873	00 0000				
874	00 0000	3330	DCX	000000,000000,000000,000000	73233280
875	00 0000				
876	00 0000				
877	00 0000				
878	B0 0000	3331	DCX	B00000,B00000,B00000,B00000	73233290
879	B0 0000				
87A	B0 0000				
87B	B0 0000				
87C	B0 0000	3332	DCX	B00000,B00000,B00000,B00000	73233300
87D	B0 0000				
87E	B0 0000				
87F	B0 0000				
880	F0 0000	3333	DCX	F00000,F00000,F00000,F00000 80	73233310
881	F0 0000				
882	F0 0000				
883	F0 0000				
884	F0 0000	3334	DCX	F00000,F00000,F00000,F00000	73233320
885	F0 0000				
886	F0 0000				
887	F0 0000				
888	F0 0000	3335	DCX	F00000,F00000,F00000,F00000	73233330
889	F0 0000				
88A	F0 0000				
88B	F0 0000				
88C	F0 0000	3336	DCX	F00000,F00000,F00000,F00000	73233340
88D	F0 0000				
88E	F0 0000				
88F	F0 0000				

890	00 0000	3338	DCX	000000,000000,000000,000000 90	73233360
891	00 0000				
892	00 0000				
893	00 0000				
894	00 0000	3339	DCX	000000,000000,000000,000000	73233370
895	00 0000				
896	00 0000				
897	00 0000				
898	00 0000	3340	DCX	000000,000000,000000,000000	73233380
899	00 0000				
89A	00 0000				
89B	00 0000				
89C	F0 0000	3341	DCX	F00000,000000,000000,F00000	73233390
89D	00 0000				
89E	00 0000				
89F	F0 0000				
8A0	F0 0000	3342	DCX	F00000,F00000,F00000,F00000 A0	73233400
8A1	F0 0000				
8A2	F0 0000				
8A3	F0 0000				
8A4	F0 0000	3343	DCX	F00000,F00000,F00000,F00000	73233410
8A5	F0 0000				
8A6	F0 0000				
8A7	F0 0000				
8A8	F0 0000	3344	DCX	F00000,F00000,F00000,F00000	73233420
8A9	F0 0000				
8AA	F0 0000				
8AB	F0 0000				
8AC	F0 0000	3345	DCX	F00000,F00000,F00000,F00000	73233430
8AD	F0 0000				
8AE	F0 0000				
8AF	F0 0000				
8B0	F0 0000	3346	DCX	F00000,F00000,F00000,F00000 B0	73233440
8B1	F0 0000				
8B2	F0 0000				
8B3	F0 0000				
8B4	F0 0000	3347	DCX	F00000,F00000,F00000,F00000	73233450
8B5	F0 0000				
8B6	F0 0000				
8B7	F0 0000				
8B8	F0 0000	3348	DCX	F00000,F00000,F00000,F00000	73233460
8B9	F0 0000				
8BA	F0 0000				
8BB	F0 0000				
8BC	F0 0000	3349	DCX	F00000,F00000,F00000,F00000	73233470
8BD	F0 0000				
8BE	F0 0000				
8BF	F0 0000				

ILLEGAL INSTRUCTION DETECT ROM 73232

```
8C0  00 0000   3351   DCx  000000,000000,000000,000000 C0   73233490
8C1  00 0000
8C2  00 0000
8C3  00 0000
8C4  00 0000   3352   DCx  000000,000000,000000,000000      73233500
8C5  00 0000
8C6  00 0000
8C7  00 0000
8C8  00 0000   3353   DCx  000000,000000,000000,000000      73233510
8C9  00 0000
8CA  00 0000
8CB  00 0000
8CC  00 0000   3354   DCx  000000,000000,000000,000000      73233520
8CD  00 0000
8CE  00 0000
8CF  00 0000
8D0  00 0000   3355   DCx  000000,000000,000000,000000 D0   73233530
8D1  00 0000
8D2  00 0000
8D3  00 0000
8D4  00 0000   3356   DCx  000000,000000,000000,000000      73233540
8D5  00 0000
8D6  00 0000
8D7  00 0000
8D8  00 0000   3357   DCx  000000,000000,000000,000000      73233550
8D9  00 0000
8DA  00 0000
8DB  00 0000
8DC  F0 0000   3358   DCx  F00000,000000,000000,F00000      73233560
8DD  00 0000
8DE  00 0000
8DF  F0 0000
8E0  00 0000   3359   DCx  000000,000000,000000,000000 E0   73233570
8E1  00 0000
8E2  00 0000
8E3  00 0000
8E4  F0 0000   3360   DCx  F00000,F00000,000000,000000      73233580
8E5  F0 0000
8E6  00 0000
8E7  00 0000
8E8  F0 0000   3361   DCx  F00000,F00000,000000,000000      73233590
8E9  F0 0000
8EA  00 0000
8EB  00 0000
8EC  00 0000   3362   DCx  000000,000000,000000,000000      73233600
8ED  00 0000
8EE  00 0000
8EF  00 0000
```

ILLEGAL INSTRUCTION DETECT ROM 73232

8F0	F0 0000	3364	DCX	F00000,F00000,F00000,000000 F0	73233620
8F1	F0 0000				
8F2	F0 0000				
8F3	00 0000				
8F4	00 0000	3365	DCX	000000,000000,000000,000000	73233630
8F5	00 0000				
8F6	00 0000				
8F7	00 0000				
8F8	00 0000	3366	DCX	000000,000000,000000,000000	73233640
8F9	00 0000				
8FA	00 0000				
8FB	00 0000				
8FC	F0 0000	3367	DCX	F00000,F00000,F00000,F00000	73233650
8FD	F0 0000				
8FE	F0 0000				
8FF	F0 0000				

900 3369 END 73233670

NO ERRORS

A	02EA		
ABL	0278		
ABL.D2	0287		
ABORT	0040		
ADRMW	008A	295	
ADRS	0061	310	
AE	058C		
AE.AER	0602		
AER	0581		
AFAULT	005A	1528	
AGB	063C	2692	
AH	02EA		
AHI	02EA		
AHM	02F6		
AI	02EA		
AIS	02EC		
AL	047F		
AM	02EF		
AR	02EA		
ARESULT	065A	2776	
ATBL2	028E	1142	
ATBL3	0292		
ATL	0278		
ATL.D2	0280		
AUTOIO	0046		
AUTOIO1	0047	379	1683
BAL	02D2		
BALR	02D6		
BBS	02CA		
BCKDIV	03B3	1546	1550
BFBS	02C7		
BFC	02BF		
BFCR	02C3		
BFFS	02C7		
BFS	02CF		
BRESULT	065F	2697	
BTBS	02BC		
BTC	02B4		
BTCR	02B8		
BTFS	02BC		
BXH	02DA		
BXH.D2	02E4		
BXLE	02DA		
BXLE.D2	02E7		
C	0300		
CARRYCK	0634	2893	
CBT	024D		
CE	058C		
CE.CER	0646		
CE2	0658	2792	
CE3	0655	2801	
CE4	065E	2800	
CER	0581		
CH	0300		

NOCOR1	06E7	2988				
NORMAL	061E					
NORMLOOP	0620	2742				
NOVF	05AB	2584				
NR	021C					
NRESTO	036E	1477				
NTRANS	00FC	1120				
O	021E					
OC	0426					
OCR	042A					
OH	021E					
OHI	021E					
OI	021E					
OKDIV1	0355	1446				
OKDIVH	03A6	1523				
OR	021E					
OUEXIT	05E5	2654				
OUTDIS	0069	319	335	352	2075	
OVDIV	038F	1515	1542	1549	1560	1563
OVDIV1	0388	1447	1470	1505		
OVF1	05A8	2576				
PB	04B9					
PBR	04C0					
PLUS1	05B1	2589				
PSWDIS	00A2	370				
PWRDWN	00B6	175	274			
PWRUP	0100					
PWRUP1	010F					
QUEINT	00E4	1661				
RB	045B					
RBL	0294					
RBL.02	02A4					
RBR	0463					
RBT	024F					
RCHKW	0174	629				
RD	042D					
RDR	0432					
RDR1	0434	1724				
RDWTBH	0130	588				
REDCHECK	0165	607	620			
REGDIS	0095					
RETCRC	016A	1100	1988			
RH	0436					
RHB	0438					
RHH	0439					
RHR	043F					
RHRB	0443					
RHRH	0441					
RI1	0196					
RI2	0198					
RLL	0189					
RLL1	023A	1020				
RLRR	01A3					
RLX	023D	1017	2594			
RRL	023F					
RRL1	0240	1029				

RRX	0243	1026
RSTRFLPT	05F6	502
RTBL2	02AB	1180
RTBL3	02B0	
RTL	0294	
RTL.D2	029C	
RTRANW	0164	639
RWSC	04AF	1923
RXF	0191	
RXH	018D	
S	02FA	
SAVEFLPT	05EA	405
SAVREG	00C3	404
SBT	024B	
SCP	0496	
SE	058C	
SE.SER	0600	
SER	0581	
SETG	00F8	828
SETL	00FA	829
SH	02FA	
SHI	02FA	
SI	02FA	
SINT	0403	
SIS	02FC	
SLA	03BF	
SLHA	03C9	
SLHL	0231	
SLHLS	0230	
SLL	0224	
SLLS	0224	
SLOOP1	00C5	400
SLRA	03BC	
SLRH	01A6	
SR	02FA	
SRA	03CF	
SRHA	03D9	
SRHL	0235	
SRHLS	0234	
SRL	022A	
SRLL	019E	
SRLLS	019B	
SRLS	022A	
SS	0410	
SSR	0422	
ST	01F5	
START	0001	
STATR	0477	1870
STATW	046B	1854
STB	0207	
STBR	020C	
STE	057B	
STE.D2	0573	
STEST	0382	1484
STH	01F9	
STR	0200	

STME	0565					
STME.D2	0570					
STMELOOP	0571	2811				
STMLOOP	0203	899				
SUBR	0544	2041	2094			
SUBR1	0549	2123				
SUBR2	054B	2180				
SUM	0630	2724				
SVC	0407					
SVC.D2	0409					
TBT	024A					
TESTR	047D	1864				
TESTW	0471	1848				
THI	0222					
TI	0222					
TLATE	026C					
TQWAIT	03F8	1651				
TRA	0516	2129				
TRANSL	015A	638				
TRCK	04DC	2053				
TRONLY	0514	2012				
TS	0245					
TS1	00F4	1039				
TWAIT	0017	126	162			
TWAIT1	003D	432	525			
TWAIT2	03FA	449				
WAIT	002F	130	182	578	1664	
WAIT1	0031	170				
WAIT2	0034	169				
WB	045B					
WBR	0463					
WBRB	0458					
WBRRBR	0463					
WD	0447					
WDR	044E					
WH	0451					
WHB	0457					
WHH	0455	1812				
WHR	0459					
WRITE2	013C	562				
WRTSC	04AC	1920				
X	0220					
XBIT	01A8					
XH	0220					
XHI	0220					
XI	0220					
XOR1	0269	1096				
XR	0220					
ZRESULT	0664	2645	2647	2734	2762	

HEXADECIMAL DISPLAY

M71-102
HEXADECIMAL DISPLAY
INFORMATION SPECIFICATION

1. INTRODUCTION

The optional Hexadecimal Display Panel provides a means to manually control the Processor, interrogate and display various Processor registers and machine status, set and display Processor memory locations, and may be programmed as an I/O device by the user.

This specification describes the 09-065F02 Hexadecimal Display Panel (Product Number M71-102). It is also applicable to the 09-065F01 Binary Display Panel (Product Number M71-101), which is identical to the Hexadecimal Display Panel except for the omission of the hexadecimal indicators. The Hexadecimal Display Panel provides the following functions:

Displays five bytes of programmable digital information.

Registers and displays five hexadecimal digits of manually entered keyboard data.

Displays the WAIT and Power (PWR) indicators for the Processor.

Provides a 26 key control keyboard for manual input to the display.

Provides two bytes of unbuffered Switch Register data to the Processor.

Provides one byte of status to the Processor.

Provides a three position OFF-ON-LOCK key type switch capable of switching three separate power supply control lines.

Provides a control signal to the Processor that the display requires micro-program support.

2. GENERAL DESCRIPTION

A complete description of the operation of the Hexadecimal Display Panel is provided in the appropriate User's Manual. This specification describes the display from a maintenance view point. Figure 1 shows the Hexadecimal Display Panel.

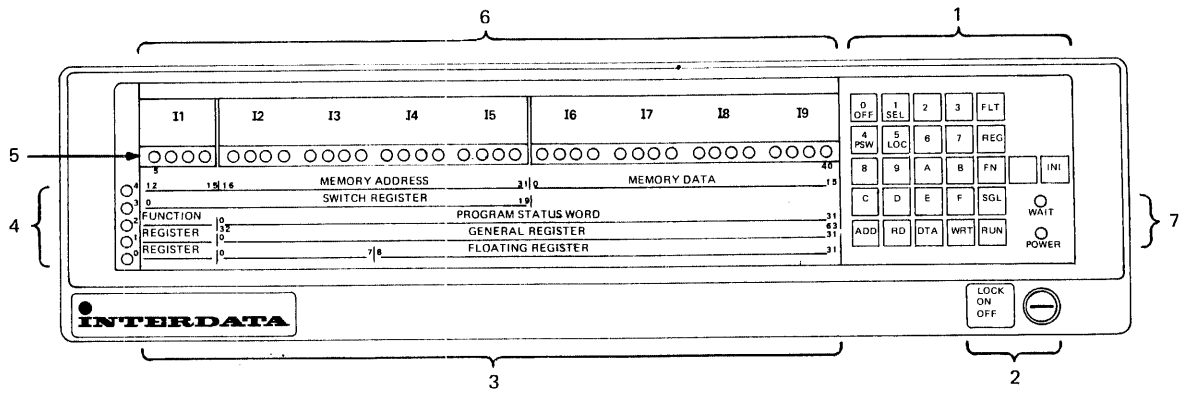


Figure 1. Hexadecimal Display Panel

Various parts of the Hexadecimal Display Panel in Figure 1 are numbered to correlate to the following descriptions.

1. Control Keyboard. The keyboard is the operators manual input to the Processor. The function of the specific keys are:

DTA — The function of the Data (DTA) key is to clear the Switch Register, connect the Switch Register to the display indicators, and enable hexadecimal data to be entered into the register. The Switch Register remains enabled and connected to the display indicators until any non-hexadecimal key other than DTA is depressed.

Hexadecimal Keys 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F supply data to the Switch Register when it is enabled, and the function number or register number for the Processor supported display (see Section 2.2).

ADD — The Address (ADD) key causes the Processor to read the five hexadecimal characters of the Switch Register, store them in the address portion of the Program Status Word (PSW), and display PSW 32:63 on the indicators.

RD — The Read (RD) key causes the Processor to read the memory location specified by the PSW, increment the PSW address by two, and display on the indicators the new address and the data read from memory.

WRT — Depressing the Write (WRT) key causes the data contained in the Switch Register to be written into the address specified by the PSW, the PSW to be incremented by two, and the new address and the data written to be displayed on the indicators.

FLT — Depressing the Floating-Point Register (FLT) key, followed by any hexadecimal key n, causes Floating-Point Register n to be displayed on the indicators.

REG — Depressing the Register (REG) key, followed by any hexadecimal key n, causes general register n to be displayed.

FN — Depressing the Function (FN) key, followed by any hexadecimal key n, causes the Processor to perform "Function n" as described in the appropriate User's Manual.

SGL — Depressing the Single Step (SGL) key causes the Processor to execute one user instruction and display the last register or function selected.

RUN — Depressing the Run (RUN) key causes the Processor to enter the Run mode at the address specified by the PSW.

INI — Depressing the Initialize (INI) key initializes the Processor.

SEL — Depress DTA, then 0 or F, for selection of Register Set 0 or 1 respectively. Then depress the Function (FN) Key followed by SEL to enable the selected register set to be displayed.

NOTE

The display requires support from the micro-program for all functions other than entering or displaying Switch Register data.

2. OFF-ON-LOCK Key Operated Locking Switch. This switch controls the power to the Processor and allows the keyboard to be completely disabled in the LOCK position.

3. Indicator Formats. These formats aid the user in interpreting the display indicators.

4. Format Selectors L0:4. Light Emitting Diode (LED) indicators L0:4 determine the format to be used to interpret display indicators L5:40.

5. Display Indicators L5:40. These LED indicators are used to display the PSW, general registers, etc., as described by the indicator formats.

6. Display Indicators I1:9. These indicators display the corresponding values displayed on L5:40 in the hexadecimal format.

7. WAIT and PWR. These indicators are illuminated when Processor is in the Wait state and Power is supplied to the Processor.

2.1 Switch Register Entries

When the operator is manipulating the Switch Register, there is no interaction between the display and the Processor. Data is entered into this register by first depressing the DTA key. This operation clears the Switch Register; connects the Switch Register to L5:24 of the display, and allows subsequent hexadecimal keyboard entries to be left shifted into the least significant digit of the resigter. The register is disconnected from the display and disabled when any non-hexadecimal key other than DTA is depressed. The register can be momentarily examined when it is disabled without affecting the Processor operation by depressing any hexadecimal key.

2.2 Processor Intervention

Depressing the following single keys causes the signals ESNC0 and ESNO0 to be complimentarily pulsed (ESNC0 is a positive going pulse):

ADD
RD
WRT
SGL
RUN

Depressing one of the following sequences of two keys causes a similar action:

FLT n (n is any hexadecimal digit)
REG n
FN n

3. FUNCTIONAL DIAGRAM ANALYSIS AND CIRCUIT DESCRIPTION

Refer to Figure 2. Hexadecimal Display Panel Block Diagram and Functional Schematic 09-065D08.

3.1 OFF-ON-LOCK Switch

This switch (2K1) controls power to the Processor by completing the circuit between CONT2 and CONT1 in the ON and LOCK positions. The switch is factory wired to provide one set of closures. This switch also provides a hard ground to the Processor as POFF0 in the OFF position which may be used as an early power down indication. When the switch is in the ON position, LP5 (2L1) is provided to the keyboard to enable the sensing of these switch closures.

3.2 Keyboard

The keyboard (Sheet 2) has a 5 x 5 switch array which is used to enter information to the Hexadecimal Display Panel logic, plus an Initialize (INI) key used to transmit this condition to the Processor (2G1). The keyboard is a self-contained unit and connects to the 35-520 logic board by 27 stakes, 00-1 through 26-1. These normally open switches are encoded by diode logic (Sheet 2) to form HEX01:31 (2B8) and FUN00:30 (2C8), plus a few additional control signals mentioned later in this description. The switches are designed to be high active when a switch is depressed by biasing all receiving gates low with a 220 ohm input resistor. A switch being depressed causes an input gate to go high by supplying LP5 through a current limiting resistor from the common input, Pin 0, if the OFF-ON-LOCK switch is in the ON position. There is no keyboard rollover protection and if more than one key is simultaneously depressed, the result is unspecified.

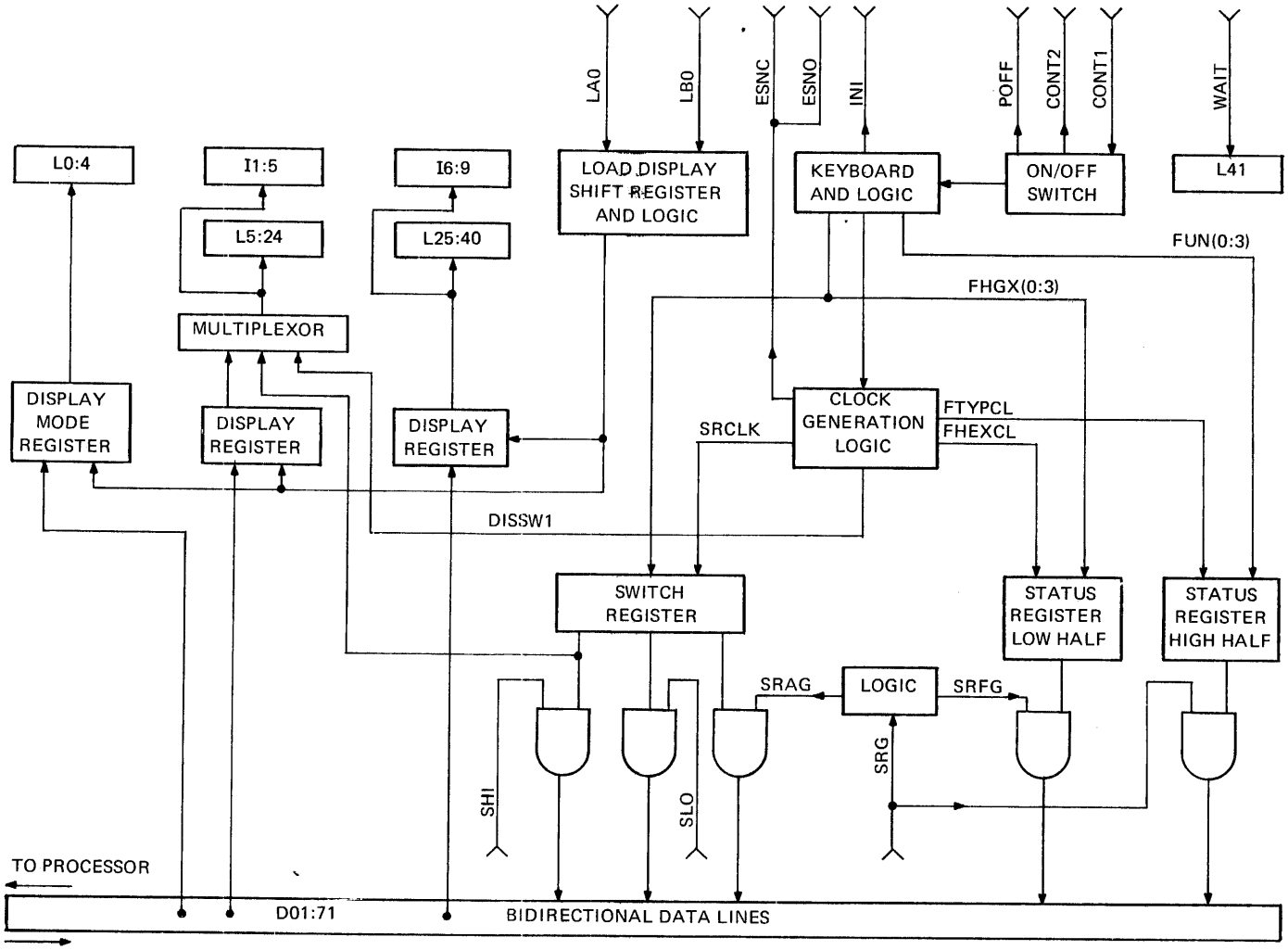


Figure 2. Hexadecimal Display Panel Block Diagram

3.3 Matrix Encoding

The diode matrix is encoded to drive signals HEX01:31 to the hexadecimal equivalent of the respective key 0:F (HEX31 is the LSB) when it is depressed. Depressing any function key other than DTA causes FUN00:30 to yield the codes specified by Table 1.

TABLE 1. FUNCTION KEY ENCODING (FUN00:30)

Key Depressed	FUN00	FUN10	FUN20	FUN30
SGL	0	1	1	1
RUN	1	1	1	1
WRT	1	1	0	1
RD	1	0	1	1
ADD	1	0	0	1
REG	0	1	1	0
FLT	0	1	0	0
FN	0	1	1	1

3.4 Clocking

Depressing any keyboard key other than DTA or INI generates one of three types of clocks used by the Hexadecimal Display Panel logic. This is accomplished by a positive transition of signal KEY1 (2F8) whenever one of these keys is depressed. The one shot triggered by this transition (2G8) is used to allow a one to two millisecond interval for switch bounce to subside before triggering the second one shot STRB1 (2K8) which is used to generate one of the three clocks. Since contact bounce is likely to retrigger these one shots when a key is released, the occurrence of signal KEY1 (any key depressed), HKEY1 (2F9 a hexadecimal key depressed), or FKEY1 (2H7 a function key depressed) being true in coincedence with the one shot is used to derive the clocks.

3.5 Switch Register Clocks

The Switch Register is enabled for clocking by depressing the DTA key. This is accomplished by direct clearing the Switch Register Enable flip-flop (SRENB) (2L6) when DTA is depressed and ANDing the zero output of the flip-flop plus HKEY1 and STRB1 to drive the Switch Register Clock (SRCLK0) (2M7). This clock is disabled by setting SRENB with the occurrence of FKEY1 when any function key is depressed.

3.6 Status Register Clocks

Two different clocks are used to load the status register. FTYPCL0 (2M8) is generated whenever any function key other than DTA is depressed and is used to load FUN00:30 into one half of the status register. The second clock FHEXCL0 (2N8) is generated whenever a hexadecimal key is depressed if the previously depressed key was FN, REG, or FLT. In this case, the hexadecimal input would be the register number or function number desired and FHEXCL0 is used to clock HEX01:31 into the second half of the status register.

3.7 Processor Intervention

The logic of the display signals the Processor that a response is necessary to a console function by signal ESNC0 (2R7) and its compliment ESNO0 (2R7). These signals are complimentarily pulsed whenever a function key other than DTA, FN, REG, or FLT is depressed, or whenever a hexadecimal key is depressed following FN, REG, or FLT (the occurrence of FHEXCL0).

3.8 Switch Register Loading

The Switch Register (4B1, 4D1, 4G1, 4J1, and 4M1) is loaded with a hexadecimal character with the occurrence of each SRCLK0 as mentioned previously. Data is entered into the least significant character (4B1) from the switches (HEX01:31) and left shifted through the register with each clock. The register is cleared whenever the DTA key is depressed.

3.9 Status Register

The status register is loaded in two parts as described previously. One half is loaded from FUN00:30 when a Function (FN) key is depressed by the occurrence of FTYPCL0. The least significant bit of this register is re-circulated on SGL or RUN and the second LSB is re-circulated on SSL to conform to the status codes indicated in Table 2. The second half of the register is loaded from HEX01:31 with the occurrence of FHEXCL0. These registers are initialized by SCLR0 from the Processor.

TABLE 2. STATUS CODES

KEY	DL1	DL2	DL3	DL4	DL5	DL6	DL7	DL0
SGL	1	U	X	X	X	X	X	X
INITIALIZE	U	U	U	U	U	U	O	U
RUN	0	0	0	X	X	X	X	X
WRT	0	0	1	U	U	U	U	U
RD	0	1	0	U	U	U	U	U
ADR	0	1	1	U	A_1	A_2	A_3	A_4
REG n	1	0	0	1	n_1	n_2	n_3	n_4
FLT n	1	0	1	1	n_1	n_2	n_3	n_4
FN n	1	0	0	0	n_1	n_2	n_3	n_4

A = Most significant hexadecimal digit of Switch Register
U = Unspecified
X = Unchanged
n = Hexadecimal digit associated with function (see Section 6)

The display status is presented to the Processor on the data lines (DL01:71) for the duration of time that control signal SRG0 is at a logical zero level. The data presented for status is in accordance with Table 2.

3.10 Display Register Loading

The Hexadecimal Display Panel registers and displays five bytes of data transmitted from the Processor. Two control signals are transmitted from the Processor to direct the loading of these registers. LA0 (2K5) is a low active pulse which signifies that data is available on bi-directional Data Lines D01:71 and it is to be loaded into the least significant byte of the display register. LA0 is used to initialize a four bit shift register (2M4) to 1000_2 which is used to load subsequent bytes, and generate a load pulse LA1 which is used to load the data into the LSB of the display register (2B6 and 3E6). Four subsequent LB0 pulses sent from the Processor gates data from D01:71 into successive bytes of the display register (3G6 and 3J6, 4C5 and 4E5, 4G5 and 4K5, 4N5 and 3N2). This is accomplished as each LB0 pulse is inverted and gated as LDB1, LDC1, LDD1 and LDE1 (2N4) respectively as controlled by the sequencing shift register (2M4) which is right shifted with each LB0 pulse.

3.11 Display Indicators

The two least significant bytes of the display register are gated directly to LEDs L25:40 and the hexadecimal indicators I6:9 (Sheet 3). LEDs L5:24 and hexadecimal indicators I1:5 are used to display either the most significant bytes of the display registers or the Switch Register. These sets of registers are selected through the 2:1 multiplexors (4C6, 4E6, 4H6, 4K6 and 4N6) as determined by the state of the DISSW1 (2N6). DISSW1 is high whenever the Switch Register is enabled (SRENB1) or a hexadecimal key is depressed (HKEY1).

3.12 Processor Inputs

Data is gated to the Processor in response to control signals SHI0, SLO0 or SRG0. SLO0 gates the two least significant digits of the Switch Register onto the bi-directional Data Lines D01:71 (4C3 and 4C4). SHI0 gates the next two Switch Register digits onto the bi-directional Data Lines D01:71 (4H3 and 4K3). SRG0 causes the status register bits to be gated (3D4) as per Table 2. Note that either the most significant Switch Register character is gated (4N3) if DL11 is low or the hexadecimal portion of the status register if DL11 is high (3H4).

4. PROCESSOR INTERFACING

4.1 Processor Connector

Signals from the display are terminated at a 26-080F06 type connector per the following list:

SIGNAL	PIN	SIGNAL	PIN	*X1-X4	PIN
D01	109	LA0	203	X1	207
D11	110	LB0	114	X2	211
D21	111	SHI0	200	X3	210
D31	112	SLO0	206	X4	209
D41	202	WAIT1	102		
D51	204	SRG0	113		
D61	205	ESNC0	103		
D71	208	ESNO0	104		
POFF0	105	INIT0	101		
CONT1	DB1-C1 & 214	SSGL1	106		
CONT2	DB1-C2	GND	100-3		
CONT3	DB-C3 & 213	GND	108		
SCLR0	107	GND	212	twisted with 114	
		GND	201	twisted with 203	

*X1-X4 A1-8 leads to front terminal strip of chassis.

4.2 Timing

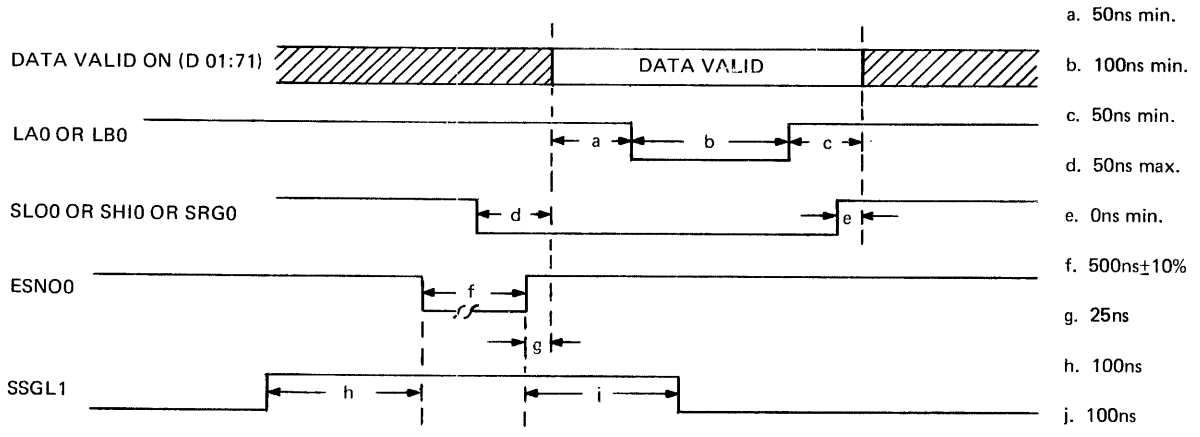


Figure 3. Hexadecimal Display Panel Timing

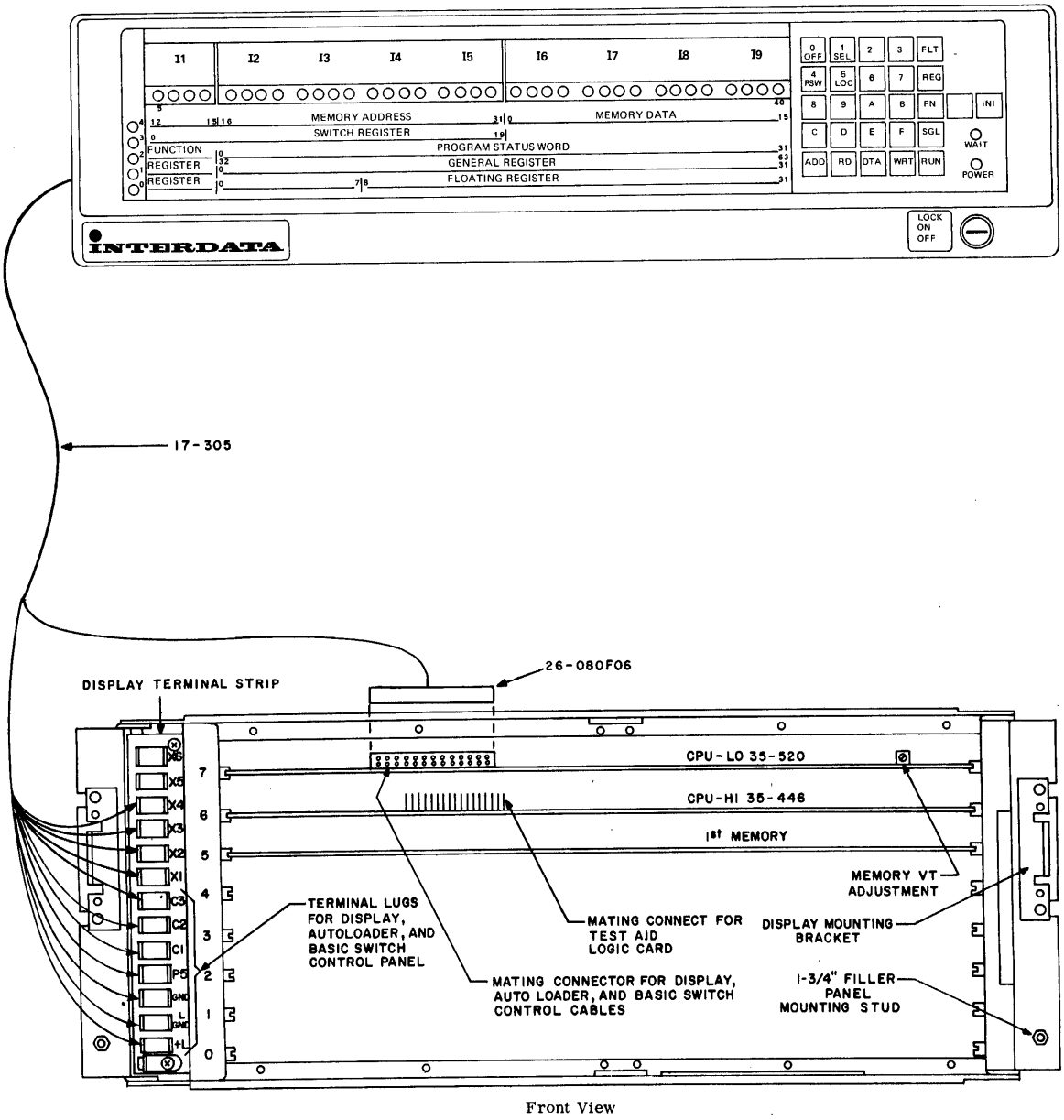
5. INSTALLATION PROCEDURE

The Hexadecimal Display Panel is connected to the Processor via a 17-305 cable. The 26-080F06 30-pin connector of the Hexadecimal Display Panel plugs into the mating connector as shown in Figures 4, 5 and 6.

CNTL1, CNTL2, P5, GND, LGND, +L jumpers go to corresponding lugs on the Processor chassis display terminal strip as shown in Figure 4.

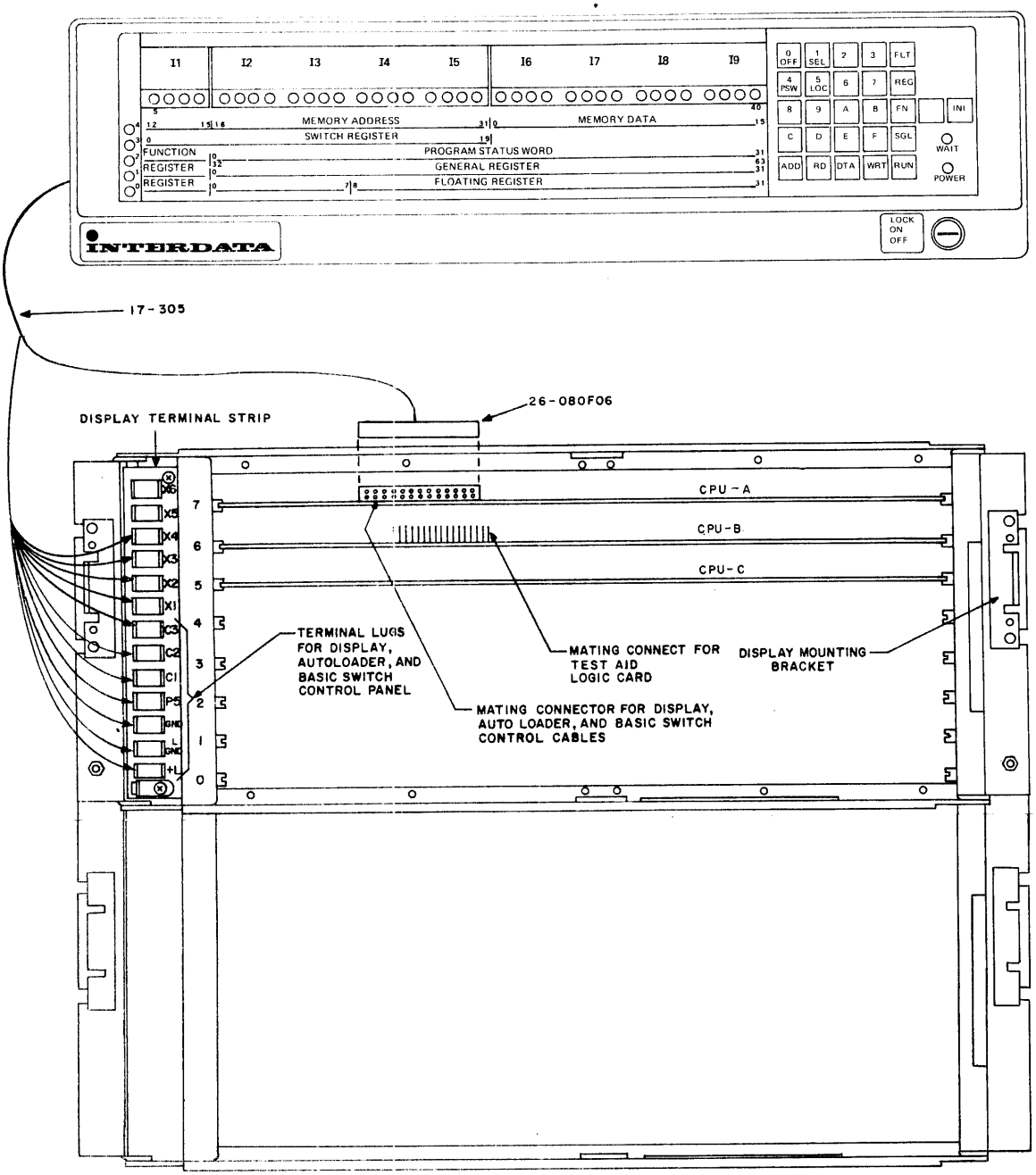
6. POWER

The Hexadecimal Display Panel draws its power from the P5 and +L lugs on the Processor chassis display terminal strip. See Figure 4.



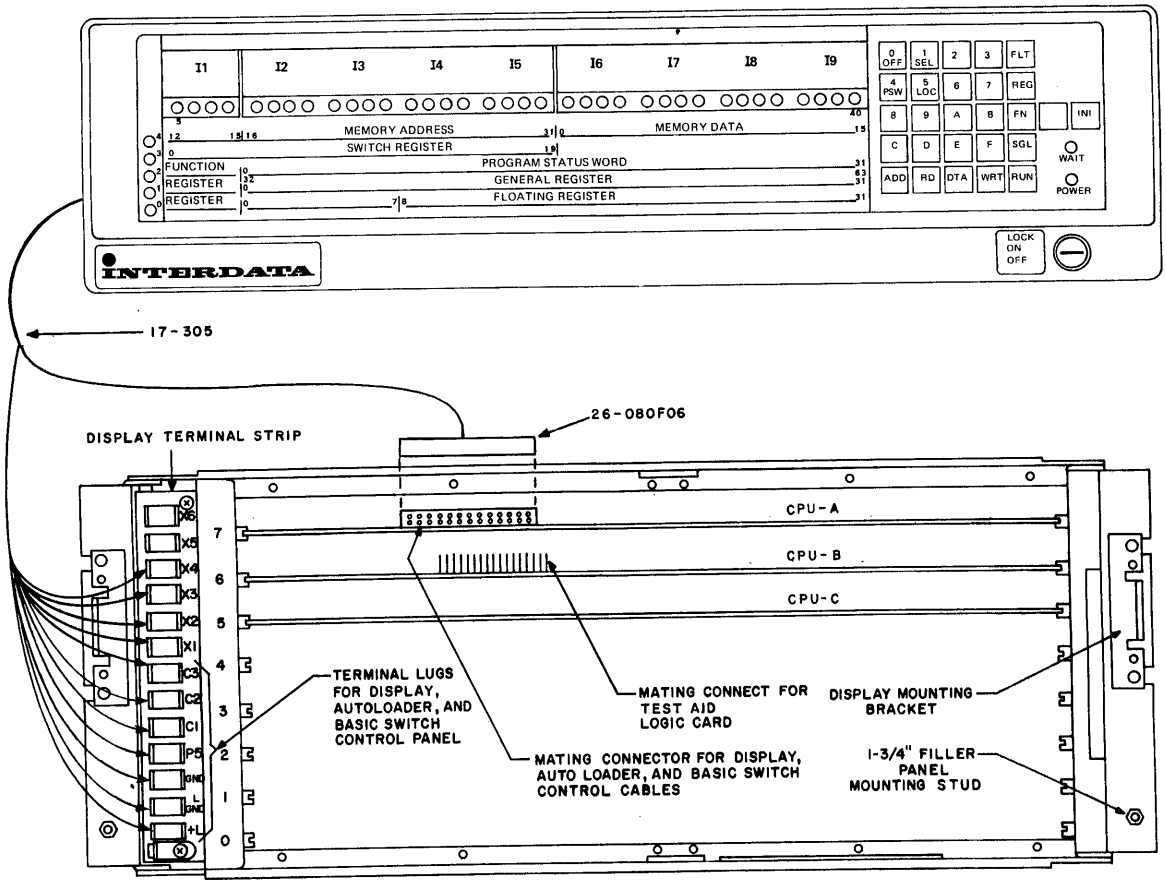
Front View

Figure 4. 7/16 Basic Display Installation



7/16 HSALU OR 7/32 TWIN CHASSIS INSTALLATION

Figure 5. Model 7/16 HSALU or 7/32 Installation



Front View

7/16 HSALU INSTALLATION

Figure 6. Model 7/16 HSALU Installation 7" Chassis

The following list provides a brief description of each mnemonic found in the Hexadecimal Display Panel. The source of each signal on Functional Schematic 09-065D08 is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
CONT1	12 VAC to turn on power supply	2L1
CONT2	12 VAC to turn off power supply	2M1
DISSW1	Controls Display Multiplexors for L5:24	2R6
ESNC0	Execute switch normally open	2R7
ESNO0	Execute switch normally closed	2R7
FTYPCL0	Function type status register clock	2N7
FHEXCL0	Hexadecimal type status register clock	2N8
FUN00:30	Encoded functional keys	Sheet 2
HEX01:31	Encoded hexadecimal keys	Sheet 2
INIT0	Initialize Processor	2H2
LA0	Low active signal from Processor which initializes the loading sequence and loads the least significant byte of the Hexadecimal Display Panel	2K5
LB0	Low active signal from Processor used to control loading of display registers by generating LDB1, LDC1, LDD1, LDE1	2L5
LDB1	Load display registers	2R3
LDC1		2R4
LDD1		2R4
LDE1	Loads display mode register and most significant hexadecimal digit of the display	2R4
POFF0	Early power OFF failure	2K1
SCLR0	System Clear, initialize status registers	3J1
SDA0	DTA key depressed	2J2
SHI0	Switch Register high half gate command	2M2
SLO0	Switch Register low half gate command	2L3
SOR0	SGL or RUN keys depressed	2K2
SRAG1	Switch Register most significant hexadecimal digit gate command	2R2
SRCLK0	Switch Register clock	2M7
SRFG1	Status Register Function high half gate command	2R2
SRG1	Status Register low half gate command	2M2
SSL1	SGL key depressed	2J6
WAIT1	Wait light control	2M6

DRAWINGS

INTERDATA®

RELEASED FOR PRODUCTION
ENG. [illegible] DATE 11/9/76

MNEM.	SCHEMATIC LOCATION CONTROL 'A'	ROM 'B'	ALU 'C'	TYPE
ACKO	25D9 - SOURCE			I/O
ADDO	29A6 - INPUT	14D8 - SOURCE		INT
ADRSO	25A9 - SOURCE			I/O
ARHI20		10G1 - INPUT	21H3 - SOURCE	INT
ARHI30		10G2 - INPUT	21H3 - SOURCE	INT
ARHI40		10G2 - INPUT	21H3 - SOURCE	INT
ARHI50		10G3 - INPUT	21K1 - SOURCE	INT
ATNO	31G1 - INPUT			I/O
B000		13D9 - SOURCE	20B1 - INPUT	INT
B010		13E9	20C1	
B020		13E9	20C1	
B030		13E9	20D1	
B040		13G9	20E1	
B050		13G9	20F1	
B060		13G9	20G1	
B070		13G9	20H1	
B080	26M1 - SOURCE	13J9	20J1	
B090	26M2	13J9	20K1	
B100	26M3	13J9	20L1	
B110	26M3	13J9	20M1	
B120	26M4	13L9	20M1	
B130	26M5	13M9	20N1	
B140	26M6	13M9	20R1	
B150	26M6 - SOURCE	13M9 - SOURCE	20S1 - INPUT	INT
BB001	29C5 - INPUT		29E1 - SOURCE	INT
BRCH1	33G1 - INPUT	14F8 - SOURCE		INT
BADRO	25A9 - SOURCE			EXT HWA
BCNTO	25D5 - SOURCE			EXT HWA
CAO		14E8 - SOURCE	24N3 - INPUT	INT
CDIVO	36E6 - INPUT		36R1 - INPUT	INT
CLO70	25A9 - SOURCE			I/O
CLK1B	32M1 - SOURCE	12A9 - INPUT		INT
CLK1C	32M2 - SOURCE		17C1 - INPUT	INT
CLMDRO	27F9 - SOURCE		19B5 - INPUT	INT
CMDO	25C9 - SOURCE			I/O
CMNDO	30F1 - INPUT	14E8 - SOURCE	36L1 - INPUT	INT
CPLOC1		10A8 - INPUT	17A1 - SOURCE	
CPMAR1		10A5 - INPUT	16D1 - SOURCE	
CRYINO	33M9 - SOURCE		36N1 - INPUT	
CSRH1	36C6 - SOURCE		36J1 - INPUT	
CSV1	30G1 - INPUT	10L9 - INPUT	22C8 - SOURCE	
CSVDIVO	36F6 - SOURCE		36L5 - INPUT	INT
D000			15A1 - SOURCE	I/O
D010			15A2	
D020			15A3	
D030			15A4	
D040			15A5	
D050			15A6	
D060			15A7	
D070			15A8	
D080			15H1	
D090			15H2	
D100			15H3	
D110			15H4	
D120			15H5	
D130			15H6	
D140			15H7	
D150			15H8 - SOURCE	I/O
DACKO	25B9 - SOURCE			I/O
DAO	25C9 - SOURCE			I/O
DCO	31J1 - INPUT			DATA CHA
DCRO	31J1 - INPUT			DATA CHA
DONO	32R5 - SOURCE	11K1 - INPUT		INT
DRO	25B9 - SOURCE			I/O
DS20		8K8 - SOURCE	24J8 - SOURCE	INT
DSB1		14R8 - SOURCE	17A1 - INPUT	INT
DSTOPO	33G9 - SOURCE	12A9 - INPUT	17C1 - INPUT	INT
ENDA1	35M1 - INPUT	14G1 - SOURCE	24C3 - INPUT	INT
ENDB1	35K1 - INPUT	14J8 - SOURCE		INT
ENDC1	35L1 - INPUT	14K8 - SOURCE		INT
ENDD1	35L1 - INPUT	14K8 - SOURCE	24F3 - INPUT	INT
ENM51	27G9 - SOURCE		19B3 - INPUT	INT
ENO	27K9 - SOURCE			DMA
ENSBO		14S8 - SOURCE	17B6 - INPUT	INT
ERO	27F9 - SOURCE			MEM
ESA1	31A3 - SOURCE	8A1 - INPUT		INT
EXBSYO	27N1 - INPUT			EXT MAC
EXDUAO	27G1 - INPUT			EXT MAC
FAIFB00	32J3 - SOURCE	8G1 - INPUT		INT
FDEC10	35B9 - SOURCE	5A1 - INPUT		INT

MNEM.	SCHEMATIC LOCATION CONTROL 'A'	ROM 'B'	ALU 'C'	TYPE
FDEC20	35C9 - SOURCE	5F1 - INPUT	" "	INT
FINRO	35J9 - SOURCE	8D1 - INPUT		INT
FLR121	30H7 - SOURCE		36L5 - INPUT	INT
FMFF1	34E1 - INPUT		36K8 - SOURCE	INT
FPDO	36B6 - SOURCE		36J1 - INPUT	INT
FPSE1	27H6 - SOURCE	10G1 - INPUT	18C1 - INPUT	EXT MAC
FRSTPO		14D8 - INPUT	36M3 - SOURCE	INT
GABB1	29C5 - INPUT		29C4 - SOURCE	INT
GABORT1	33C9 - SOURCE	9J9 - INPUT		INT
GDATO	25D5 - SOURCE		15A9 - INPUT	INT
HWO	33K1 - INPUT	9J1 - INPUT		I/O
ILOC1	35E9 - SOURCE	10A8 - INPUT	17C1 - INPUT	INT
IMAR1	35D9 - SOURCE	10A5 - INPUT	16M1 - INPUT	INT
INHO	27C9 - SOURCE			MEM
INIT1	33C9 - SOURCE	9J4 - INPUT		INT
IRO81	29N7 - SOURCE	12C1 - INPUT		
IRO91	29N6 - SOURCE	12D1		
IR101	29N6 - SOURCE	12F1		
IR111	29N5 - SOURCE	12G1		
IR121	30B6 - INPUT	12C1		
IR131	30C6 - INPUT	12D1		
IR141	30D6 - INPUT	12F1		
IR151	30E6 - INPUT	12G1 - INPUT		INT
LARHI20		10E3 - SOURCE	21H1 - INPUT	INT
LARHI30		10E3 - SOURCE	21J1 - INPUT	
LARHI40		10E3 - SOURCE	21J1 - INPUT	
LARHI50		10E3 - SOURCE	21J1 - INPUT	
LMARO		14K8 - SOURCE	16B1 - INPUT	
LMASO	27D9 - SOURCE	10E5 - INPUT	16A9 - INPUT	
LOADO	30R1 - INPUT	14B8 - SOURCE	16R4 - INPUT	
LPSWLI	31F4 - SOURCE	29J4 - INPUT		
LRARO	33E9 - SOURCE	8F1 - INPUT		INT
LRO	27E9 - SOURCE			MEM
M1		14J8 - SOURCE	22M7 - INPUT	INT
MA000			16B9 - SOURCE	MEM/MAC
MA001			16A9	
MA010			16B9	
MA011			16B9	
MA020			16C9	
MA021			16C9	
MA030			16D9	
MA040			16E9	
MA050			16E9	
MA060			16E9	
MA070			16F9	MEM/MAC
MA080			16H9	MEM
MA090			16H9	
MA100			16J9	
MA110			16J9	
MA120			16L9	
MA130			16L9	
MA140			16L9 - SOURCE	
MD000		8B1 - INPUT	18D7 - SOURCE	
MD010		8B1	18E7	
MD020		8C1	18G7	
MD030		8C1	18H7	
MD040		8E1	18K7	
MD050		8E1	18L7	
MD060		8F1	18N7	
MD070		8F1 - INPUT	18R7	
MD080	29H6 - INPUT		19D7	
MD090	29H6 - INPUT		19E7	
MD100	29H6 - INPUT		19G7	
MD110	29H5 - INPUT		19H7	
MD120		29G3 - INPUT	19K7	
MD130		29G3 - INPUT	19L7	
MD140		29G4 - INPUT	19N7	
MD150		29G4 - INPUT	19R7 - SOURCE	MEM
MDR000		8H1 - INPUT	18C7 - SOURCE	INT
MDR011		8H1 - INPUT	18E7 - SOURCE	INT
MSTOPO	33H9 - SOURCE	8G1 - INPUT		INT
NORMO	31K3 - INPUT		23F2 - SOURCE	INT
P00	33L1 - INPUT	8G8 - SOURCE		INT
P20		8N8 - SOURCE		INT
PERRO	28B6 - INPUT			EXT PAR
PFDTO	32D9 - INPUT			EXT PPF
POWDNO	32J7 - SOURCE			EXT PPF
PSW231	31E8 - SOURCE	5J9 - INPUT		INT
PSW271	31D9 - SOURCE	11G1 - INPUT		INT

MNEM.	SCHEMATIC LOCATION CONTROL 'A'	ROM 'B'	ALU 'C'	TYPE
RD000	35A1 - INPUT	7E1 - SOURCE		INT
RD030	31S8	7E4		
RD041	35G1	7E5		
RD051	35C1	7E6		
RD061	35C1	7E7		
RD071	35B1	7E7		
RD080	29A8	7K1		
RD091	29B8	7K2	36G1 - INPUT	
RD101	29A9	7K3		
RD110	25N1	7K4	23G1 - INPUT	
RD120	29C9	7K5	23G1 - INPUT	
RD131	30R1	7K6	24M3 - INPUT	
RD141	30R1 - INPUT	7K7	24M3 - INPUT	
RD151		7K7	24J3 - INPUT	
RD161	34E1 - INPUT	7S1		
RD171	25B1	7S2		
RD181	25B1	7S3		
RD191	25S1	7S4		
RD201	25R1	7S5		
RD211	25S1	7S6		
RD221	35M1	7S7	24E3 - INPUT	
RD231	35L1 - INPUT	7S7 - SOURCE	24E3 - INPUT	INT
READ1		11K1 - SOURCE	20A1 - INPUT	INT
REQO	27K1 - INPUT			EXT DMA
RR1	35E1 - INPUT	9N3 - SOURCE		INT
RSTOPO	33F9 - SOURCE	7D8 - INPUT		INT
S01		14G8 - SOURCE	22R9 - INPUT	INT
S11		14H8 - SOURCE	22M7 - INPUT	INT
S21		14H8 - SOURCE	22M7 - INPUT	INT
S31		14J8 - SOURCE	22M7 - INPUT	INT
S001	31A4 - INPUT	13E2 - INPUT	22C9 - SOURCE	INT
S011	31B4 - INPUT	13E2	22D9	
S021	31B4 - INPUT	13E2	22E9	
S031		13E2	22F9	
S041	31D4 - INPUT	13G2	22J9	
S051	31D4	13H2	22K9	
S061	31D4	13H2	22L9	
S071	31D4	13H2	22M9	
S081	26K1	13K2	21C9	
S091	26K1	13K2	21D9	
S101	26K2	13K2	21E9	
S111	26K3	13K2	21F9	
S121	26K4	13R4	21J9	
S131	26K5	13R6	21K9	
S141	26K5	13R4	21L9	
S151	26K6 - INPUT	13R6 - INPUT	21M9 - SOURCE	INT
SCLRO	32A5 - SOURCE			I/O
SCLROA	32E5 - SOURCE	7A8 - INPUT		INT
SELA1		10G2 - INPUT	24J8 - SOURCE	
SEQO1	30M1 - INPUT		22N8 - SOURCE	
SHCLKO	36A9 - SOURCE		23R1 - INPUT	
SHCRY1	30H1 - INPUT		29E4 - SOURCE	
SHORT1	31K9 - INPUT	8R8 - SOURCE		
SMPYO	36A1 - SOURCE		36N1 - INPUT	
SRHSO1	36D6 - SOURCE		23B4 - INPUT	
SRHS11	36E6 - SOURCE		23B4 - INPUT	
SRLSO1	36C6 - SOURCE		23J4 - INPUT	
SRLS11	36D6 - SOURCE		23H9 - INPUT	INT
SRO	25D9 - SOURCE			I/O
SUB1	30H1 - INPUT	19H8 - SOURCE		INT
SYNO	25L1 - INPUT			I/O
ULOC1	35R9 - SOURCE	10E7 - INPUT		INT
UMAR1	35N9 - SOURCE	10G5 - INPUT		INT
UMDR1	35N9 - SOURCE	9G9 - INPUT		INT
USRLOC1		14N8 - SOURCE	23G2 - INPUT	INT
WO	27B9 - SOURCE			MEM
WRTO	27H9 - SOURCE			MEM
XMA120		10L5 - SOURCE		MEM/MAC
XMA130		10L5 - SOURCE		
XMA140		10L4 - SOURCE		
XMA141		10R5 - SOURCE		
XMA150		10L4 - SOURCE		MEM/MAC
P15	32J8 - 15VDC			

SUPPLEMENTARY INFORMATION

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL:

CPU-A	35-624 R01
CPU-B 7/32 BASIC	35-625F01 R01
CPU-B 7/32 BAS, COM, SLO	35-625F02 R01
CPU-B 7/32 BAS, COM, FAST	35-625 F03 R01
CPU-C	35-529 M01 R01
15" TERMINATOR	35-933 R02
PRI. POWER FAIL	35-948 R01
7/16 HSALU	35-544 ROS
PARITY OPTION	35-533

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

SHEET INDEX	REV. LEVEL / SHEET NO.
	1 1A 2 2A 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36

NOTES:

NAME	TITLE	DATE
R. CERO	DRAFT	12-24-75
D. FRANKENBERGER	CHK	12-24-75
W. MULLER	ENGR	4-28-76
S. MESSINA	TEST ENG	4-28-76
	MGR	4-[illegible]-76

TITLE FUNCTIONAL SCHEMATIC
MODEL 7/16 HSALU & 7/32O PROCESSOR

03073
01-097
SIZE D
DOB 1 36

(TOTAL 38 SHEETS)

BRUNING 44231 16042

INTERDATA

MNEM	CONN 2 PIN INDEX CPU-A		CONN. NO.	TYPE
RDSETO	34H9 - SOURCE		101	EXT MAC
CWRO	27G1 - INPUT		111	EXT PRT
DMAC0	35C9 - SOURCE		100	EXT MAC
HALTO	27J1 - INPUT		113	EXT MAC
IRI	35H1 - SOURCE		103	EXT MAC
MACO	31F1 - INPUT		104	EXT MAC
MEMI	35E9 - SOURCE		110	EXT MAC
MWI	35A9 - SOURCE		108	EXT PRT
PBY0	28D7 - SOURCE		109	EXT MAC
PRTECTO	35A9 - SOURCE		107	EXT PRT
XMEMO	27N1 - INPUT		112	EXT MAC

	PRIMARY POWER FAIL	
C1	32K9 12VAC	EXT
C3	32K8 12VAC	
PFDTO	32K9 SOURCE	
POWDNO	32K7 SOURCE	
PIS	32K7 15VDC	EXT

MNEM	CONN 3 PIN INDEX CPU-A		CONN.NO.	TYPE
ESN00	26A2 - INPUT		104	EXT DIS
ESNCO	26A1 - INPUT		103	
INITO	32B7 - INPUT		101	
LAO	26J6 - SOURCE		203	
LBO	26J6 - SOURCE		114	
POFFO	32B7 - INPUT		105	
SCLROD	26J9 - SOURCE		107	
SD001	26R1 - SOURCE		109	
SD011	26R2		110	
SD021	26R2		111	
SD031	26R3		112	
SD041	26R4		202	
SD051	26R5		204	
SD061	26R5		205	
SD071	26R6 - SOURCE		208	
SHIO	26J5 - SOURCE		200	
SLOO	26J5 - SOURCE		206	
SRGO	26F3 - SOURCE		113	
SSGLI	26A2 - INPUT		106	
WAITI	26J3 - SOURCE		102	EXT DIS
PS				
GND				
GND				
GND				
GND				

	PARITY OPTION BOARD	
LRO	28E4 - INPUT	MEM
MD000	28A1 - INPUT	MEM
MD010	28A1	
MD020	28A1	
MD030	28A1	
MD040	28A1	
MD050	28A1	
MD060	28A2	
MD070	28A2	
MD080	28A3	
MD090	28A3	
MD100	28A3	
MD110	28A3	
MD120	28A3	
MD130	28A3	
MD140	28A4	
MD150	28A4	
MD160	28A4 - INPUT	MEM
PERRO	28D2 - SOURCE	EXT PAR
WRTO	28E3 - INPUT	MEM
WRTOA	28E2 - INPUT	DMA
PS	28R2	
GND	28R3	

MNEM	CONN. 3 PIN INDEX CPU-B		CONN.NO.	TYPE
CLKO	11N1 - SOURCE		104	EXT TEST
RAR050	5S7 - SOURCE		119	
RAR060	5N6		108	
RAR070	5N6		109	
RAR080	5N6		110	
RAR090	5N5		107	
RAR100	5M3		113	
RAR110	5M3		118	
RAR120	5L1		117	
RAR130	5L1		116	
RAR140	5M1		114	
RAR150	5M1 - SOURCE		115	
SCLR0A	7A8 - INPUT		134	EXT TEST
PS	11N1			
PS	11N1			
GND	11N1			
GND	11M1			
GND	11M1			

MNEM	CONN 3 PIN INDEX CONN.NO.		CPU-A	TYPE
MA001A	221		16A6 - SOURCE	EXT PRT
MA011A	223		16A6	
MA021A	222		16A6	
MA031A	122		16A6	
MA041A	123		16H5	
MA051A	129		16H9	
MA061A	224		16H9 - SOURCE	EXT PRT

TEST POINT INDEX		
DESIG.	MNEM	LOC.
	CONTROL A	
TP1	SCATNO	26F1
TP2	FTITO	33J1
TP3	FPSELI	27J6
TP4	ARSTI	31K6
TP5	FLR131	30K7
TP6	FLR151	30R7
TP7	FLR141	30L7
TP8	FLR121	30H7
TP9	STPSYNO	25L1
TP10	FSTO	25H7
TP11	XRD2	27N8
TP12	GND	27M1
TP13	GND	31K6
TP14	GND	26F1
TP15	GND	25H8
	ROM B	
TP1	FTITO	11R1
TP2	XRSTO	TD9
TP3	RD020	7E3
TP4	RD010	7E2
TP5	X511	10S8
TP6	X531	10S7
TP7	X521	10S7
TP8	X501	10S8

TRUTH TABLES

19-038

SELECT INPUTS B	SELECT INPUTS A	DATA INPUTS C0	C1	C2	C3	STROBE G	OUTPUT Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

SELECT INPUTS A AND B ARE COMMON TO BOTH SECTIONS. H = HIGH LEVEL
L = LOW LEVEL X = IRRELEVANT

19-073

ADDRESS INPUT B	ADDRESS INPUT A	DATA INPUTS C0	C1	C2	C3	STROBE G	OUTPUT Y
X	X	X	X	X	X	1	HiZ
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

X = DON'T CARE

19-066 + 19-065

INPUTS STROBE	SELECT	A	B	OUTPUT Y 19-065	19-066
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H=HIGH LEVEL, L=LOW LEVEL
X=IRRELEVANT

19-028

INPUT A1/A3	INPUT B1/B3	INPUT A2/A4	INPUT B2/B4	WHEN CO=L, WHEN C2=L Σ1/Σ3	Σ2/Σ4	C2/C4	WHEN CO=H, WHEN C2=L Σ1/Σ3	Σ2/Σ4	C2/C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	H	L	L	L	L	H
H	L	H	L	L	H	L	L	L	H
L	H	H	L	L	H	L	H	H	L
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	H	L	H	L	H	H
H	L	H	H	L	H	H	H	H	H
L	H	H	H	H	L	H	H	H	H
H	H	H	H	L	H	H	H	H	H

H=HIGH LEVEL, L=LOW LEVEL
INPUT CONDITIONS AT A3, A2, B2, AND CO ARE USED TO DETERMINE OUTPUTS Σ1 AND Σ2 AND THE VALUE OF THE INTERNAL CARRY C2. THE VALUES AT C2, A3, B3, A4, AND B4 ARE THEN USED TO DETERMINE OUTPUTS Σ3, Σ4, AND C4.

NAME J. HELVATY 7-10-74 FUNCTIONAL SCHEMATIC MODEL 7/16 HSALU & 7/32C PROCESSOR
03073
01-097 D08 1A 36

INTERDATA®

UPPER BACK PANEL MAP

CONN.	TITLE	CONTROL "A"		ROM "B"		ALU "C"		MAC		CONN.
	BD LOC	07		06		05		04		
	TERM.	ROW		ROW		ROW		ROW		
	NO.	1	2	1	2	1	2	1	2	
	41	P5	P5	P5	P5	P5	P5	P5	GND	
	40	GND	GND	GND	GND	GND	GND	GND	GND	
	39	SHCLKO	FDEC20	FDEC20	MD150	MD150	SHCLKO			
	38	CRYINO	FDEC10	FDEC10	MD140	MD140	CRYINO			
	37	FMPYQ	PSW231	PSW231	MD130	MD130	FMPYQ	MD150	MD160	
	36	CDIVO		ERSWBO	MD120	MD120	CDIVO	MD130	MD140	
	35	MD110	INITI	INITI	CA0	CA0	MD110	MD110	MD120	
	34	MD100	FINRO	FINRO	ENSBO	ENSBO	MD100	MD090	MD100	
	33	MD090	GABORTI	GABORTI	USRLOC1	USRLOC1	MD090	MD070	MD080	
	32	MD080	ADDO	BDDO	CPMARI	CPMARI	MD080	MD050	MD060	
	31	SRLSO1	RD211	RD211	MD070	MD070	SHCLK21	MD030	MD040	
	30	SRLS11	RD201	RD201	MD060	MD060	SHCLK11	MD010	MD020	
	29	BBOO1	RD191	RD191	MD050	MD050	BBOO1		MD000	
	28	FMFF1	RD181	RD181	MD040	MD040	FMFF1			
	27	SEQO1	RD171	RD171	MD030	MD030	SEQO1	WRTO		
	26		RD161	RD161	MD020	MD020	RD091	DMA170	DGND	
	25	ENMS1	RD101	RD101	MD010	MD010	ENMS1	DMA150	DMA160	
	24	GDATO	RD091	RD091	MD000	MD000	GDATO	DMA130	DMA140	
	23	RD231	RD221	RD231	RD221	RD231	RD221	DGND	DMA120	
	22	RD131	RD141	RD131	RD141	RD131	RD141	DMA110	DMA100	
1	21	SO91	CSV1	RD151	CSV1	RD151	CSV1	DMA090	DMA080	1
	20	GND	GND	GND	GND	GND	GND	DMA070	DMA060	
	19	SO01	SO11	SO01	SO11	SO01	SO11	DMA050	DGND	
	18	LRARO	FLRI21	LRARO	SO31	FLRI21	SO31	LMA030	DMA040	
	17	RSTOPO	SHCRY1	RSTOPO	SO41	SHCRY1	SO41	DMA010	DMA020	
	16	SO21	SO51	SO21	SO51	SO21	SO51	DGND	DMA000	
	15	SO61	SO71	SO61	SO71	SO61	SO71		DMX140	
	14	SO81	SO91	SO81	SO91	SO81	SO91	DMX150	DMX120	
	13	SI01	SI11	SI01	SI11	SI01	SI11	DMX130	DGND	
	12	SI21	SI31	SI21	SI31	SI21	SI31	M3BZO	M2BZO	
	11	SI41	SI51	SI41	SI51	SI41	SI51	M1BZO	M0BZO	
	10	RD080	NORMO	RD080	LMARO	NORMO	LMARO	LORDO	ANSO	
	09	RD071	CSVDIVO	RD071	CPLOC1	CSVDIVO	CPLOC1	LMRQO		
	08	RD110	RD120	RD110	RD120	RD110	RD120	SOTO	EOTO	
	07	RD061	CSRN1	RD061	READ1	CSRN1	READ1	XREQO	QUEO	
	06	RD051	GABB1	RD051	MDR011	GABB1	MDR011			
	05	RD000	CLMDRO	RD000	MDR000	CLMDRO	MDR000		TPCO	
	04	LOADO	ENDA1	LOADO	ENDA1	LOADO	ENDA1		BHO	
	03	FPSELO	CLKIC	FPSELO		FPSELO	CLKIC	FPSELO	CLKIC	
	02	DSTOPO	CLK1B	DSTOPO	CLK1B	DSTOPO	SMPYO	PERRO		
	01	GND	GND	GND	GND	GND	GND	GND	GND	
	00	P5	P5	P5	P5	P5	P5	P5	GND	
		1	2	1	2	1	2	1	2	

CONN.	TITLE	MEM		MEM/IO		MEM/IO		MEM/IO		TITLE	CONN.
	BD.LOC.	03		02		01				BD.LOC.	
	TERM.	ROW		ROW		ROW				TERM	
	NO.	1	2	1	2	1	2	1	2	NO.	
	41	P5	GND	P5	GND	P5	GND	P5	GND	41	
	40	GND	GND	GND	GND	GND	GND	GND	GND	40	
	39	P15	P15	P15	P15	P15	P15	P15	P15	39	
	38	N15	N15	N15	N15	N15	N15	N15	N15	38	
	37	MD150	MD160	MD150	MD160	MD150	MD160	MD150	MD160	37	
	36	MD130	MD140	MD130	MD140	MD130	MD140	MD130	MD140	36	
	35	MD110	MD120	MD110	MD120	MD110	MD120	MD110	MD120	35	
	34	MD090	MD100	MD090	MD100	MD090	MD100	MD090	MD100	34	
	33	MD070	MD080	MD070	MD080	MD070	MD080	MD070	MD080	33	
	32	MD050	MD060	MD050	MD060	MD050	MD060	MD050	MD060	32	
	31	MD030	MD040	MD030	MD040	MD030	MD040	MD030	MD040	31	
	30	MD010	MD020	MD010	MD020	MD010	MD020	MD010	MD020	30	
	29	EXVT	MD000	EXVT	MD000	EXVT	MD000	EXVT	MD000	29	
	28	TEMPA	VT	TEMPA	VT	TEMPA	VT	TEMPA	VT	28	
	27	WRTO	TEMPB	WRTO	TEMPB	WRTO	TEMPB	WRTO	TEMPB	27	
	26	SCLRO	HWO	SCLRO	HWO	SCLRO	HWO	SCLRO	HWO	26	
	25	PERRO	LRO							25	
	24	MPARO	ENMSI							24	
	23	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO	23	
	22	RACKO	TACKO	RACKO	TACKO	RACKO	TACKO	RACKO	TACKO	22	
1	21	CLO70	DAO	CLO70	DAO	CLO70	DAO	CLO70	DAO	21	1
	20	DRO	CMDO	DRO	CMDO	DRO	CMDO	DRO	CMDO	20	
	19	SRO	ADRSO	SRO	ADRSO	SRO	ADRSO	SRO	ADRSO	19	
	18	DI40	DI50	DI40	DI50	DI40	DI50	DI40	DI50	18	
	17	DI20	DI30	DI20	DI30	DI20	DI30	DI20	DI30	17	
	16	DI00	DI10	DI00	DI10	DI00	DI10	DI00	DI10	16	
	15	DO80	DO90	DO80	DO90	DO80	DO90	DO80	DO90	15	
	14	DO60	DO70	DO60	DO70	DO60	DO70	DO60	DO70	14	
	13	DO40	DO50	DO40	DO50	DO40	DO50	DO40	DO50	13	
	12	DO20	DO30	DO20	DO30	DO20	DO30	DO20	DO30	12	
	11	DO00	DO10	DO00	DO10	DO00	DO10	DO00	DO10	11	
	10	WRTOA	MS000	WRTOA	MS000	WRTOA	MS000	WRTOA	MS000	10	
	09	MS010	MS020	MS010	MS020	MS010	MS020	MS010	MS020	09	
	08	MS030	MS040	MS030	MS040	MS030	MS040	MS030	MS040	08	
	07	MS050	MS060	MS050	MS060	MS050	MS060	MS050	MS060	07	
	06	MS070	MS080	MS070	MS080	MS070	MS080	MS070	MS080	06	
	05	MS090	MS100	MS090	MS100	MS090	MS100	MS090	MS100	05	
	04	MS110	MS120	MS110	MS120	MS110	MS120	MS110	MS120	04	
	03	MS130	MS140	MS130	MS140	MS130	MS140	MS130	MS140	03	
	02	MS150	MS160	MS150	MS160	MS150	MS160	MS150	MS160	02	
	01	GND	GND	GND	GND	GND	GND	GND	GND	01	
	00	P5	GND	P5	GND	P5	GND	P5	GND	00	
		1	2	1	2	1	2	1	2		

CONN.	TITLE	MEM		MEM/IO		MEM/IO		MEM/IO		TITLE	CONN.
	BD.LOC.	03		02		01				BD.LOC.	
	TERM.	ROW		ROW		ROW				TERM	
	NO.	1	2	1	2	1	2	1	2	NO.	
	41	P5	GND	P5	GND	P5	GND	P5	GND	41	
	40	GND	GND	GND	GND	GND	GND	GND	GND	40	
	39	P15	REQO	P15	REQO	P15	REQO	P15	REQO	39	
	38	N15	ENO	N15	ENO	N15	ENO	N15	ENO	38	
	37	ACTO	TACO	ACTO	TACO	ACTO	TACO	ACTO	TACO	37	
	36									36	
	35									35	
	34	BCNTO	BADRO							34	
	33	MA130	MA140	MA130	MA140	MA130	MA140	MA130	MA140	33	
	32	MA110	MA120	MA110	MA120	MA110	MA120	MA110	MA120	32	
	31	MA090	MA100	MA090	MA100	MA090	MA100	MA090	MA100	31	
	30	MA070	MA080	MA070	MA080	MA070	MA080	MA070	MA080	30	
	29	MA050	MA060	MA050	MA060	MA050	MA060	MA050	MA060	29	
	28	RDACKO	TDACKO	RDACKO	TDACKO	RDACKO	TDACKO	RDACKO	TDACKO	28	
	27	DCO	DCRO	DCO	DCRO	DCO	DCRO	DCO	DCRO	27	
	26	SCLRO	HWO	SCLRO	HWO	SCLRO	HWO	SCLRO	HWO	26	
	25									25	
	24									24	
	23	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO	23	
	22	RACKO	TACKO	RACKO	TACKO	RACKO	TACKO	RACKO	TACKO	22	
0	21	CLO70	DAO	CLO70	DAO	CLO70	DAO	CLO70	DAO	21	0
	20	DRO	CMDO	DRO	CMDO	DRO	CMDO	DRO	CMDO	20	
	19	SRO	ADRSO	SRO	ADRSO	SRO	ADRSO	SRO	ADRSO	19	
	18	DI40	DI50	DI40	DI50	DI40	DI50	DI40	DI50	18	
	17	DI20	DI30	DI20	DI30	DI20	DI30	DI20	DI30	17	
	16	DI00	DI10	DI00	DI10	DI00	DI10	DI00	DI10	16	
	15	DO80	DO90	DO80	DO90	DO80	DO90	DO80	DO90	15	
	14	DO60	DO70	DO60	DO70	DO60	DO70	DO60	DO70	14	
	13	DO40	DO50	DO40	DO50	DO40	DO50	DO40	DO50	13	
	12	DO20	DO30	DO20	DO30	DO20	DO30	DO20	DO30	12	
	11	DO00	DO10	DO00	DO10	DO00	DO10	DO00	DO10	11	
	10	MA030	MA040	MA030	MA040	MA030	MA040	MA030	MA040	10	
	09	MA020	MA021	MA020	MA021	MA020	MA02	MA020	MA021	09	
	08	XMA150	XMA190	MA01	MA02	MA01	MA02	MA01	MA02	08	
	07	MA010	MA011	MA010	MA011	MA010	MA011	MA010	MA011	07	
	06	MA000	MA001	MA000	MA001	MA000	MA001	MA000	MA001	06	
	05	PARO	XMA181	PARO	MA00	PARO	MA00	PARO	MA00	05	
	04	INHO	ERO	INHO	ERO	INHO	ERO	INHO	ERO	04	
	03	WO	LRO	WA	LRO	WA	LRO	WA	LRO	03	
	02	P15	N15	P15	N15	P15	N15	P15	N15	02	
	01	GND	GND	GND	GND	GND	GND	GND	GND	01	
	00	P5	GND	P5	GND	P5	GND	P5	GND	00	
		1	2	1	2	1	2	1	2		

7/32C 7/16 HSALU 7/16 HSALU 7/16 HSALU

NOTES

REVISIONS

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 7/16 HSALU & 7/32C PROCESSOR

TASK NO. 03073
DWG NO. 01-097 D08
SHEET OF 2-36

INTERDATA®

BACK PANEL MAP

CONN.	TITLE BD. LOC. TERM. NO.	MEM/IO OR EDMAB/IO 07 ROW 1	MEM/IO OR EDMAB/IO 07 ROW 2	MEM/IO OR EDMAB/IO 06 ROW 1	MEM/IO OR EDMAB/IO 06 ROW 2	MEM/IO OR EDMAB/IO 05 ROW 1	MEM/IO OR EDMAB/IO 05 ROW 2	MEM/IO OR EDMAB/IO 04 ROW 1	MEM/IO OR EDMAB/IO 04 ROW 2	CONN.	TITLE BD. LOC. TERM. NO.	EDMA/IO 03 ROW 1	EDMA/IO 03 ROW 2	EDMA/IO 02 ROW 1	EDMA/IO 02 ROW 2	EDMA/IO 01 ROW 1	EDMA/IO 01 ROW 2	EDMA/IO 00 ROW 1	EDMA/IO 00 ROW 2	TITLE BD. LOC. TERM. NO.	CONN.
	41	P5	GND	P5	GND	P5	GND	P5	GND		41	P5	GND							41	
	40	GND	GND	GND	GND	GND	GND	GND	GND		40	GND	GND							40	
	39	P15	P15	P15	P15	P15	P15	P15	P15		39	P15	P15							39	
	38	N15	N15	N15	N15	N15	N15	N15	N15		38	N15	N15							38	
	37	MD150	MD160	DMA170	DGND	MD150	MD160	DMA170	DGND		37	DMA170	DGND							37	
	36	MD130	MD140	DMA150	DMA160	MD130	MD140	DMA150	DMA160		36	DMA150	DMA160							36	
	35	MD110	MD120	DMA130	DMA140	MD110	MD120	DMA130	DMA140		35	DMA130	DMA140							35	
	34	MD090	MD100	DGND	DMA120	MD090	MD100	DGND	DMA120		34	DGND	DMA120							34	
	33	MD070	MD080	DMA110	DMA100	MD070	MD080	DMA110	DMA100		33	DMA110	DMA100							33	
	32	MD050	MD060	DMA090	DMA080	MD050	MD060	DMA090	DMA080		32	DMA090	DMA080							32	
	31	MD030	MD040	DMA070	DMA060	MD030	MD040	DMA070	DMA060		31	DMA070	DMA060							31	
	30	MD010	MD020	DMA050	DGND	MD010	MD020	DMA050	DGND		30	DMA050	DGND							30	
	29	EXVT	MD000	DMA030	DMA040	EXVT	MD000	DMA030	DMA040		29	DMA030	DMA040							29	
	28	TEMPA	VT	DMA010	DMA020	TEMPA	VT	DMA010	DMA020		28	DMA010	DMA020							28	
	27	WRTO	TEMPB	DGND	DMA000	WRTO	TEMPB	DGND	DMA000		27	DGND	DMA000							27	
	26	SCLRO	HWO	SCLRO	HWO	SCLRO	HWO	SCLRO	HWO		26	SCLRO	HWO							26	
	25										25									25	
	24										24									24	
	23	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO		23	SYNO	ATNO							23	
	22	RACKO	TACKO	RACKO	TACKO	RACKO	TACKO	RACKO	TACKO		22	RACKO	TACKO							22	
1	21	CL070	DAO	CL070	DAO	CL070	DAO	CL070	DAO	1	21	CL070	DAO							21	1
	20	DRO	CMDO	DRO	CMDO	DRO	CMDO	DRO	CMDO		20	DRO	CMDO							20	
	19	SRO	ADRSO	SRO	ADRSO	SRO	ADRSO	SRO	ADRSO		19	SRO	ADRSO							19	
	18	D140	D150	D140	D150	D140	D150	D140	D150		18	D140	D150							18	
	17	D120	D130	D120	D130	D120	D130	D120	D130		17	D120	D130							17	
	16	D100	D110	D100	D110	D100	D110	D100	D110		16	D100	D110							16	
	15	D080	D090	D080	D090	D080	D090	D080	D090		15	D080	D090							15	
	14	D060	D070	D060	D070	D060	D070	D060	D070		14	D060	D070							14	
	13	D040	D050	D040	D050	D040	D050	D040	D050		13	D040	D050							13	
	12	D020	D030	D020	D030	D020	D030	D020	D030		12	D020	D030							12	
	11	D000	D010	D000	D010	D000	D010	D000	D010		11	D000	D010							11	
	10	WRTOA	MS000	WRTOA	DMX140	WRTOA	MS000	WRTOA	DMX140		10	WRTOA	DMX140							10	
	09	MS010	MS020	DMX150	DMX120	MS010	MS020	DMX150	DMX120		09	DMX150	DMX120							09	
	08	MS030	MS040	DMX130	DGND	MS030	MS040	DMX130	DGND		08	DMX130	DGND							08	
	07	MS050	MS060	M3BZO	M2BZO	MS050	MS060	M3BZO	M2BZO		07	M3BZO	M2BZO							07	
	06	MS070	MS080	M1BZO	M0BZO	MS070	MS080	M1BZO	M0BZO		06	M1BZO	M0BZO							06	
	05	MS090	MS100	LOADO	ANSO	MS090	MS100	LOADO	ANSO		05	LOADO	ANSO							05	
	04	MS110	MS120	LMRQO	DGND	MS110	MS120	LMRQO	DGND		04	LMRQO	DGND							04	
	03	MS130	MS140	SOTO	EOTO	MS130	MS140	SOTO	EOTO		03	SOTO	EOTO							03	
	02	MS150	MS160	XREQO		MS150	MS160	XREQO	QUEO		02	XREQO	QUEO							02	
	01	GND	GND	GND	GNL	GND	GND	GND	GND		01	GND	GND							01	
	00	P5	GND	P5	GND	P5	GND	P5	GND		00	P5	GND							00	
		1	2	1	2	1	2	1	2			1	2	1	2	1	2	1	2		
	41	P5	GND	P5	GND	P5	GND	P5	GND		41	P5	GND							41	
	40	GND	GND	GND	GND	GND	GND	GND	GND		40	GND	GND							40	
	39	P15	REQO			P15	REQO				39									39	
	38	N15	ENO			N15	ENO				38									38	
	37	ACTO	TACO	RPCO	TPCO	ACTO	TACO	RPCO	TPCO		37	RPCO	TPCO							37	
	36			DGND	BHO			DGND	BHO		36	DGND	BHO							36	
	35										35									35	
	34							XRACKO			34									34	
	33	MA130	MA140	MA130	MA140	MA130	MA140	MA130	MA140		33	MA130	MA140							33	
	32	MA110	MA120	MA110	MA120	MA110	MA120	MA110	MA120		32	MA110	MA120							32	
	31	MA090	MA100	MA090	MA100	MA090	MA100	MA090	MA100		31	MA090	MA100							31	
	30	MA070	MA080	MA070	MA080	MA070	MA080	MA070	MA080		30	MA070	MA080							30	
	29	MA050	MA060	MA050	MA060	MA050	MA060	MA050	MA060		29	MA050	MA060							29	
	28	RDACKO	TDACKO	RDACKO	TDACKO	RDACKO	TDACKO	RDACKO	TDACKO		28	RDACKO	TDACKO							28	
	27	DCO	DCRO			DCO	DCRO				27									27	
	26	SCLRO	HWO	SCLRO	HWO	SCLRO	HWO	SCLRO	HWO		26	SCLRO	HWO							26	
	25										25									25	
	24										24									24	
	23	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO		23	SYNO	ATNO							23	
	22	RACKO	TACKO	RACKO	TACKO	RACKO	TACKO	RACKO	TACKO		22	RACKO	TACKO							22	
0	21	CL070	DAO	CL070	DAO	CL070	DAO	CL070	DAO	0	21	CL070	DAO							21	0
	20	DRO	CMDO	DRO	CMDO	DRO	CMDO	DRO	CMDO		20	DRO	CMDO							20	
	19	SRO	ADRSO	SRO	ADRSO	SRO	ADRSO	SRO	ADRSO		19	SRO	ADRSO							19	
	18	D140	D150	D140	D150	D140	D150	D140	D150		18	D140	D150							18	
	17	D120	D130	D120	D130	D120	D130	D120	D130		17	D120	D130							17	
	16	D100	D110	D100	D110	D100	D110	D100	D110		16	D100	D110							16	
	15	D080	D090	D080	D090	D080	D090	D080	D090		15	D080	D090							15	
	14	D060	D070	D060	D070	D060	D070	D060	D070		14	D060	D070							14	
	13	D040	D050	D040	D050	D040	D050	D040	D050		13	D040	D050							13	
	12	D020	D030	D020	D030	D020	D030	D020	D030		12	D020	D030							12	
	11	D000	D010	D000	D010	D000	D010	D000	D010		11	D000	D010							11	
	10	MA030	MA040	MA030	MA040	MA030	MA040	MA030	MA040		10	MA030	MA040							10	
	09	MA020	MA021	MA020	MA021	MA020	MA021	MA020	MA021		09	MA020	MA021							09	
	08	XMA150	XMA140	XMA150	XMA140	XMA150	XMA140	XMA150	XMA140		08	XMA150	XMA140							08	
	07	MA010	MA011	MA010	MA011	MA010	MA011	MA010	MA011		07	MA010	MA011							07	
	06	MA000	MA001	MA000	MA001	MA000	MA001	MA000	MA001		06	MA000	MA001							06	
	05	PARO	XMA141	PARO	XMA141	PARO	XMA141	PARO	XMA141		05	PARO	XMA141							05	
	04	INHO	ERO	INHO	ERO	INHO	ERO	INHO	ERO		04	INHO	ERO							04	
	03	WO	LRO	WO	LRO	WO	LRO	WO	LRO		03	WO	LRO							03	
	02	P15	N15	P15	N15	P15	N15	P15	N15		02	P15	N15							02	
	01	GND	GND	GND	GND	GND	GND	GND	GND		01	GND	GND							01	
	00	P5	GND	P5	GND	P5	GND	P5	GND		00	P5	GND							00	
		1	2	1	2	1	2	1	2			1	2	1	2	1	2	1	2		
		SHOWN AS MEM/IO		SHOWN AS EDMAB/IO		SHOWN AS MEM/IO		SHOWN AS EDMAB/IO													

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

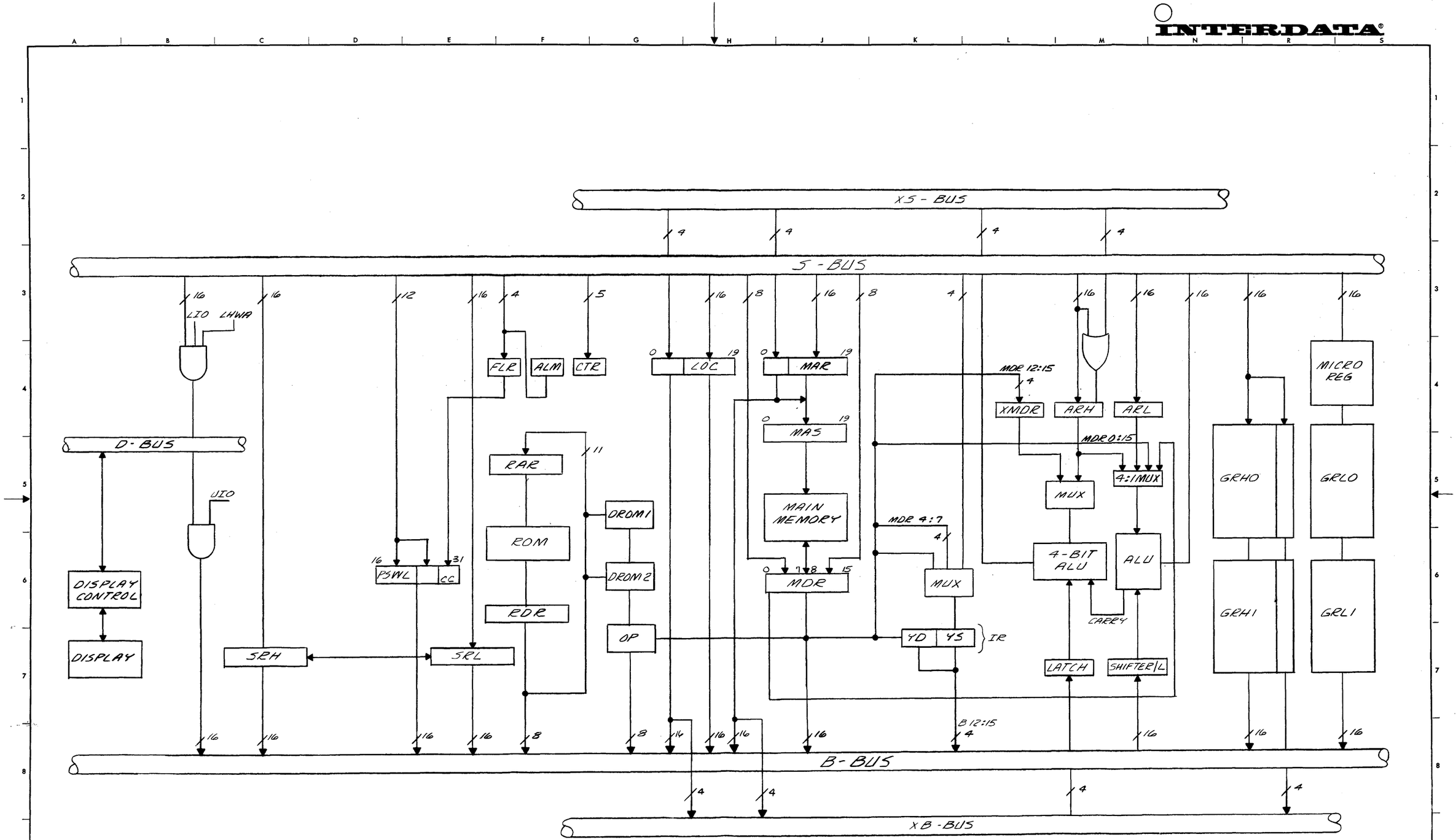
TITLE FUNCTIONAL SCHEMATIC

7/32C PROCESSOR

TASK NO. 03073

DWG NO. 01-097 208

SHEET OF 2A-36



BLOCK DIAGRAM

NOTES

NAME	TITLE	DATE
V. PERRI	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

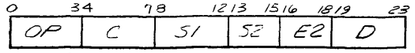
TITLE FUNCTIONAL SCHEMATIC
MODEL 7/16 HSALU & 7/32C PROCESSOR

TASK NO. 03073
DWG NO. 01-097 D08
SHEET OF 3 - 36

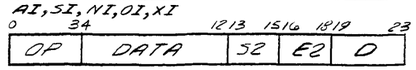
BRUNING 44-231 18042

MICRO INSTRUCTION FORMATS

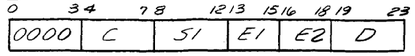
1. A,S,N,O,X,C,A



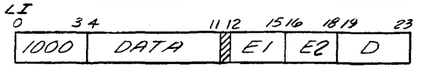
2. AI,SI,NI,OI,XI



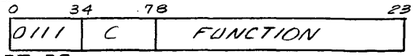
3. L



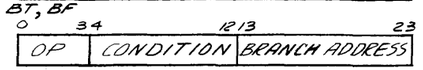
4. LI

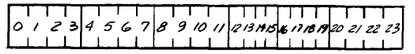


5. C



6. BT, BF





OP FIELD

0	1	2	3	
0	0	0	0	LOAD-L
0	0	0	1	AND-N
0	0	1	0	OR-O
0	0	1	1	XOR-X
0	1	0	0	ADD-A
0	1	0	1	SUB-S
0	1	1	0	CALCULATE ADR-CA
0	1	1	1	COMMAND
1	0	0	0	LOAD IMM.
1	0	0	1	AND IMM.
1	0	1	0	OR IMM.
1	0	1	1	XOR IMM.
1	1	0	0	ADD IMM.
1	1	0	1	SUB IMM.
1	1	1	0	BRANCH ON TRUE
1	1	1	1	BRANCH ON FALSE

CONTROL (C)

4	5	6	7	
0	0	0	0	NO ACTION
0	0	0	1	MRI
0	0	1	0	DI
0	0	1	1	DI2
0	1	0	0	IR
0	1	0	1	IRJH
0	1	1	0	IRJF
0	1	1	1	IRJ
1	0	0	0	MR
1	0	0	1	MR2
1	0	1	0	MRD
1	0	1	1	XR2
1	1	0	0	MWD
1	1	0	1	MRD2
1	1	1	0	MW
1	1	1	1	MW2

FIRST SOURCE (S1)

	8	9	10	11	12	
	0	0	0	0	0	MR0
	0	0	0	0	1	MR1
	0	0	0	1	0	MR2
	0	0	0	1	1	MR3
	0	0	1	0	0	MR4
	0	0	1	0	1	MR5
	0	0	1	1	0	MR6
	0	0	1	1	1	PSWL
	0	1	0	0	0	
	0	1	0	0	1	
	0	1	0	1	0	
	0	1	0	1	1	
	0	1	1	0	0	YS1
SA	0	1	1	0	1	YD1
	0	1	1	1	0	
	0	1	1	1	1	OP
	1	0	0	0	0	NULL
	1	0	0	0	1	LOCH
	1	0	0	1	0	SRL
	1	0	0	1	1	SRH
	1	0	1	0	0	LOC
	1	0	1	0	1	IO
SB	1	0	1	1	0	MDR
	1	0	1	1	1	MAR
	1	1	0	0	0	YDH
	1	1	0	0	1	YDL
	1	1	0	1	0	YDLP1
	1	1	0	1	1	YDLM1
	1	1	1	0	0	YSH
	1	1	1	0	1	YSL
	1	1	1	1	0	YSLX
	1	1	1	1	1	YSHX

SECOND SOURCE (S2)

13	14	15	
0	0	0	NULL
0	0	1	ONE
0	1	0	ARL
0	1	1	TWO
1	0	0	MDR
1	0	1	SIGN
1	1	0	AE
1	1	1	ARH

OP EXTENSION (E1)

13	14	15	
1	0	0	SR
0	1	0	SL
1	1	0	CS
X	X	1	LEN

OP EXTENSION (E2)

16	17	18	
1	X	X	CARRY IN
X	1	X	CARRY OUT
X	X	1	FLAGS

OP EXTENSION 1 (E2) FOR I/O

16	17	18	
0	0	0	DCAK
0	0	1	ADRS
0	1	0	DA
0	1	1	OC
1	0	0	ACK
1	0	1	DR
1	1	0	STAT
1	1	1	

DESTINATION

	19	20	21	22	23	
	0	0	0	0	0	MR0
	0	0	0	0	1	MR1
	0	0	0	1	0	MR2
	0	0	0	1	1	MR3
	0	0	1	0	0	MR4
	0	0	1	0	1	MR5
	0	0	1	1	0	MR6
	0	0	1	1	1	PSWL
	0	1	0	0	0	CTR
	0	1	0	0	1	ARL
DA	0	1	0	1	0	ARH
	0	1	0	1	1	AR
	0	1	1	0	0	YSI
DB	0	1	1	0	1	HWA
	0	1	1	1	0	
	0	1	1	1	1	FLR
	1	0	0	0	0	NULL
	1	0	0	0	1	
DC	1	0	0	1	0	SRL
	1	0	0	1	1	SRH
	1	0	1	0	0	LOC
	1	0	1	0	1	IO
DD	1	0	1	1	0	MDR
	1	0	1	1	1	MAR
	1	1	0	0	0	YDH
	1	1	0	0	1	YDL
	1	1	0	1	0	YDLP1
	1	1	0	1	1	YDLM1
	1	1	1	0	0	YSH
	1	1	1	0	1	YSL
	1	1	1	1	0	
	1	1	1	1	1	

FUNCTION (FOR COMMAND)

8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
1	0				1											MPY
1	1				1											UNMPY
		1				1										DIV
			1	0	0											SLI
			1	0	1											SLZ
			0	1	0											SRI
			0	1	1											SRZ
						1										CI
									1							CO
								0								
								0		1	0	0				SUT
								0		0	1	0				CUT
								0		1	1	0				TUT
								0				1				RPT
								0					1			SWA
								0					0			CWA
								0						1		POW
								0							1	ALRM
								1								
								1		1						TABT
								1			1					PW
								1				1				JH
								1					1			
								1						1		TS
								1							1	CYD

BRANCH CONDITION

4	5	6	7	8	9	10	11	12	
0	0	1							C
0	0		1						V
0	0			1					G
0	0				1				L
0	0					1			MSKI
0	0						1		WAIT
0	0							1	
0	1	1							ATNX
0	1		1						HWL
0	1			1					QUE
0	1				1				ER
0	1					1			ATN
0	1						1		MAC
0	1							1	
1	0	1							SNGL
1	0		1						CATN
1	0			1					DC
1	0				1				DRD
1	0					1			MALF
1	0						1		PPF
1	0							1	
1	1	1							HWIO
1	1		1						NORM
1	1			1					CNTR
1	1				1				ARST
1	1	0	0	0	0	1	0	0	UT
1	1						1		SHORT
1	1							1	

MICRO PROGRAM FORMAT

NOTES

NAME	TITLE	DATE
V. PERRI	DRAFT	8-21-73
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 7/16 HSALU & 7/32C PROCESSOR

TASK NO. 03073
DWG NO. 01-097 D08
SHEET 4 OF 36

BRUNING 44-231 16042

INTERDATA®

138-1 FDEC10
8B9 IR001
8B9 IR011
8C9 IR021
8C9 IR031
8D9 IR041
8E9 IR051
8E9 IR061
8F9 IR071

F (NOTE 2) G GND

FDEC20 139-1
9G1

(SEE NOTE 2)

F9 SRA150 A12
F9 SRA140 B11
F8 SRA130 C10
F8 SRA120 D09

A04 7/16 HSALU 19-122F01 7/32 19-193F03

A05 7/16 HSALU 19-122F04 7/32 19-193F04

A06 7/16 HSALU 19-122F05 7/32 BCS 19-193F07 7/32 B&BCF 19-193F10

R58 1K P5

657 SRD050 657 SRD070

A16 7/16 HSALU 19-122F02 7/32 19-193F02

A18 7/16 HSALU 19-122F06 7/32 BCS 19-193F06 7/32 B&BCF 19-193F09

A27 7/16 HSALU 19-122F03 7/32 19-193F01 DROM 1 (F-7/16)

A29 7/16 HSALU 19-122F07 7/32 BCS 19-193F05 7/32 B&BCF 19-193F08 DROM 2

J9 PRIVO

14F8 BRCH1
7K6 RD131
7K7 RD141
7K8 RD151
7S2 RD161
7S2 RD171
7S3 RD181
7S4 RD191
7S5 RD201
7S6 RD211
7S7 RD221
7S8 RD231

A30 19-043 HGO
A19 19-043 HGO
A07 19-043 HGO

SRA50 SRA60 SRA70 SRA80 SRA90 SRA100 SRA110 SRA120 SRA130 SRA140 SRA150

9N4 A2 9N2, A2 9N2, A2 9N5, A6

P5 R11 470 R13 470 R12 470 R7 470 R10 470 R8 470 R9 470 R2 470 R1 470 R3 470 R4 470

(FALSE BUS)

8G9 P01
8N1 DSTOPO
A103 19-017 HG

12A9 CLK1B
8G9 RARSTPO
7D8 RSTOPO
A101 19-058 HG

A03 19-035
A15 19-035
A26 19-035

COUNT UP COUNT DOWN CARRY BORROW LOAD CLEAR

RAR120 119-3 RAR130 118-3 RAR140 117-3 RAR150 115-3

A01 19-015 HG
A02 19-101 B

RAR151 6B1 RAR15IA 6E2
RAR141 6A2 RAR14IA 6S2
RAR131 6B1 RAR13IA 6E2
RAR121 6A2 RAR12IA 6S2

RAR110 118-3 RAR100 113-3

A13 19-015 HG
A14 19-101 B

RAR111 6B1 RAR11IA 6E1
RAR101 6A1 RAR10IA 6S1
RAR091 6B1 RAR09IA 6E1
RAR081 6A1 RAR08IA 6S1

RAR090 107-3
RAR080 110-3
RAR060 108-3
RAR070 109-3

A25 19-015 HG
A24 19-016 HG

RAR071 6R1
RAR061 6N1
RAR051 6C1
RAR050 6M1 119-3
EN000 6K1
EN010 6D1
EN100 6F1, 6R1
EN110 6H1

RAREQSTP 6G1

R6 1K P5

8G4 FLRARO
R57 1K P5
A5 PRIVO

A08 19-024 NA

137-1 PSW231

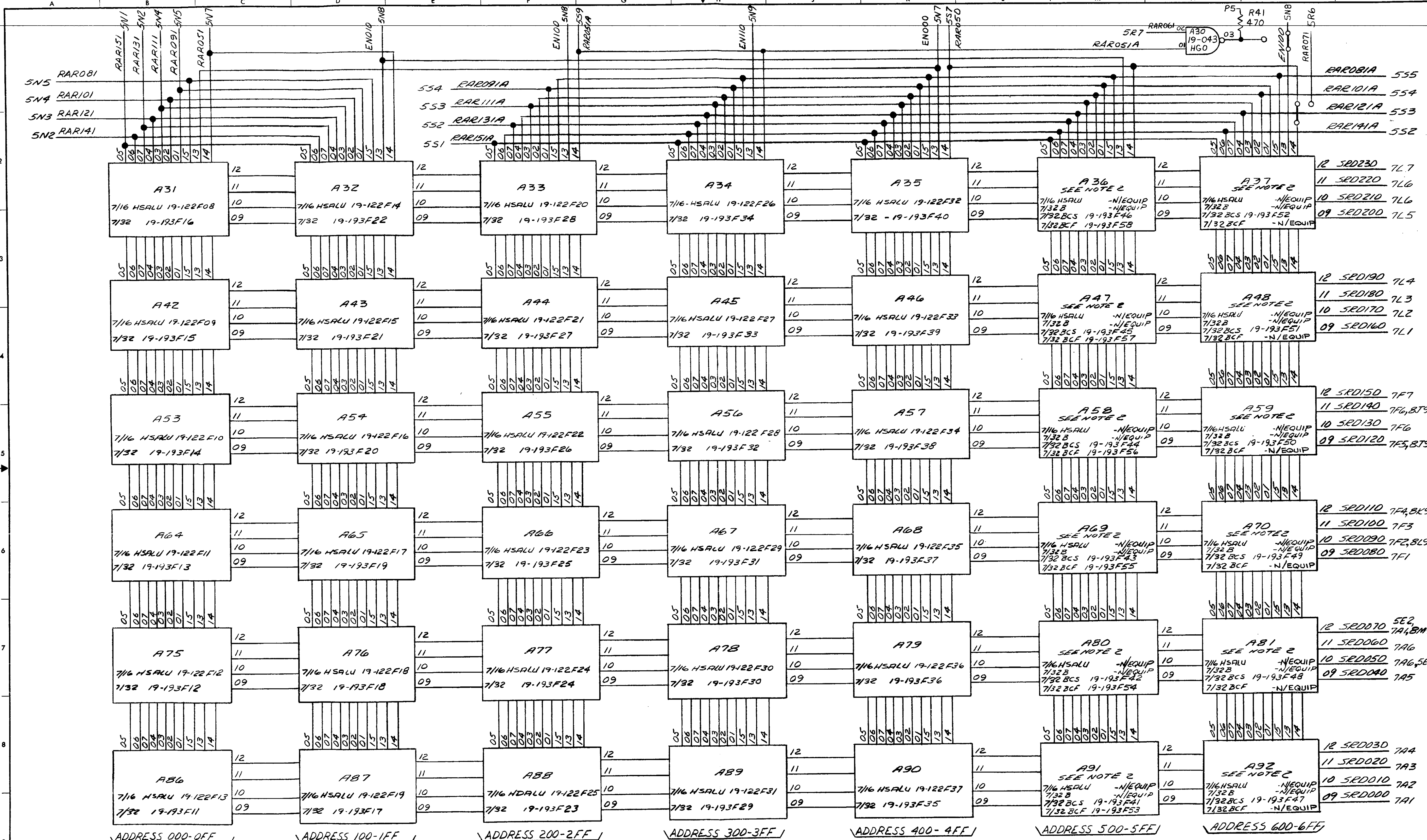
NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-B BOARD.
2. FOR 7/32 OPTION TERMINAL 'G' IS STRAPPED TO 'GND', AND 'E' TO 'H, J, K OR L'. FOR 7/16 HSALU, TERMINAL 'F' IS STRAPPED TO TERMINAL 'G', 'E' TO GND 'T' TO 'H' AND 'V' TO 'J'. SEE STRAPPING OPTIONS ON SHEET 9.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODELS 7/16 HSALU & 7/32C PROCESSOR

TASK NO. 03073 DWG NO. 01-097 D08 SHEET OF 5-36

BRUNING 44-231 16X42



READ ONLY MEMORY

NOTES

1. ALL APPARATUS THIS SHEET LOCATED ON CPU-B BOARD.

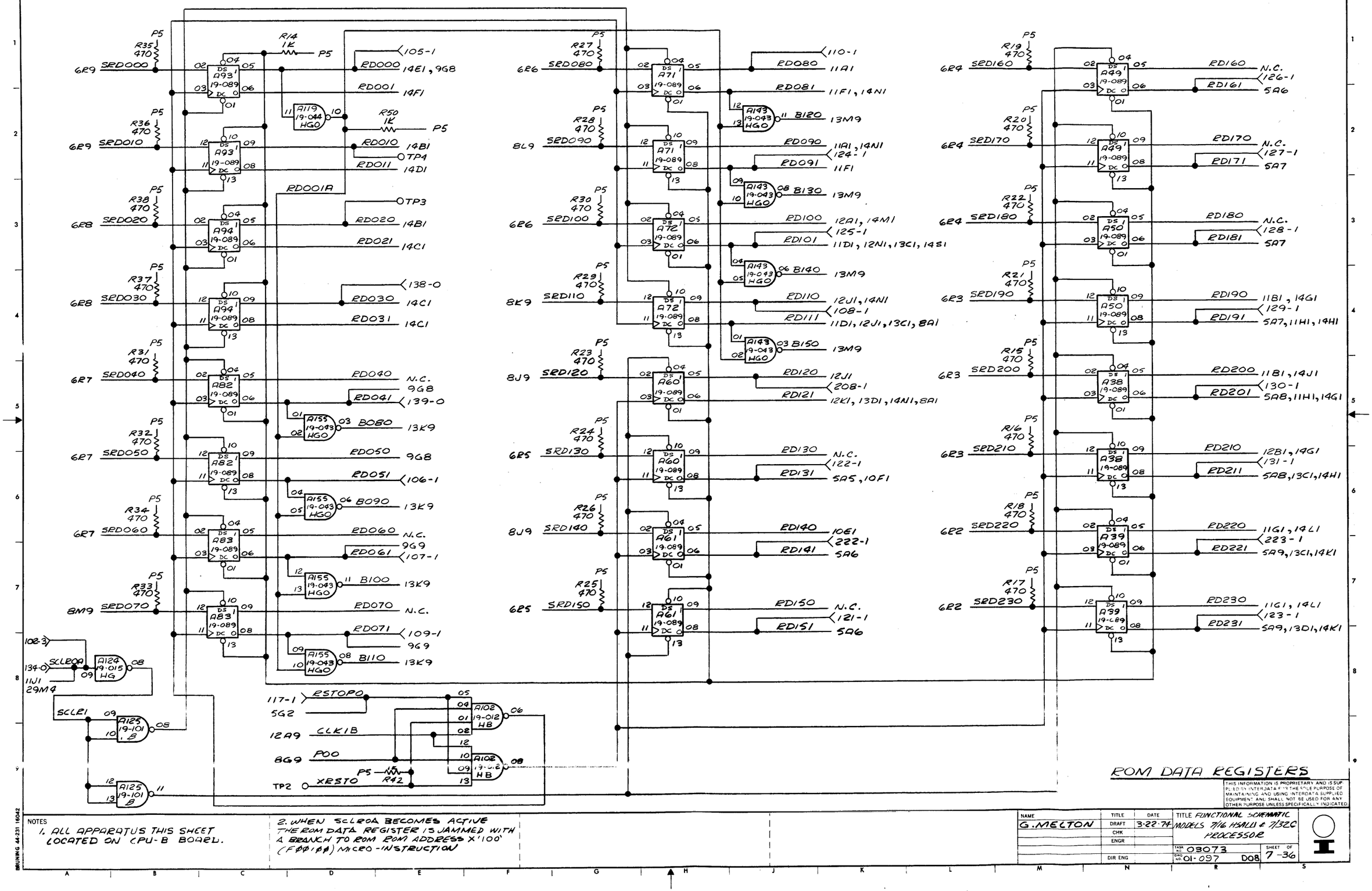
2. 7/32B-35-625F01
7/32BCS-35-625F02
7/32 BCF-35-625F03

NAME	TITLE	DATE
B GRAY	DRAFT	10-19-73
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODELS 7/16 HSALU & 7/32C PROCESSOR

TASK NO. 03073
DWG NO. 01-097 D08
SHEET 6 OF 36

INTERDATA®



ROM DATA REGISTERS

NOTES

1. ALL APPARATUS THIS SHEET LOCATED ON CPU-B BOARD.
2. WHEN SCLR0A BECOMES ACTIVE THE ROM DATA REGISTER IS JAMMED WITH A BRANCH TO ROM ROM ADDRESS X'100' (F00/100) MICRO-INSTRUCTION

NAME	TITLE	DATE
G.MELTON	DRAFT	3-22-74
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODELS 7/16 H5A11 & 7/32C PROCESSOR

TASK NO. 03073

DWG NO. 01-097 D08

SHEET 7 OF 36

BRUNING 44-231 16042

ESAI 211-0 7K5 2D121 2D111 7K5

MD000 224-1 · MD010 225-1 · MD020 226-1 · MD030 227-1

FINRO R1,29G1 137-1 · MD040 228-1 29G4 · MD050 229-1 29F4 · MD060 230-1 29F4 · MD070 231-1 · LEAPO 118-1 · FAIFB00 137-0 9F6

MSTOPO 132-0 N1 · CLK1B 118 · MDR000 205-1 · MDR011 206-1 10R3 · FAMOD0 29R4

CLK1B 299,9G1 · DSTOPO 102-1 5J1, 96B, 104A, 112, 142 · CA0 14E9 · FINRO D1

P5 · R43 1K · FLEAPO 5U8 9E6 · P11 · P30 · B1 · B0 · A1 · A0

FINEIA 9J5

B000 13E9 9J1, 5A1 IR001 · B010 13E9 5A1 IR011 · B020 13E9 5A1 IR021 · B030 13E9 9J2, 5A1 IR031

B040 13G9 9J2, 5A1 IR041 · B050 13G9 5A1 IR051 · B060 13H9 5A1 IR061 · B070 13H9 5A1 IR071

EAESTPO 5G1 · P00 14K1, 7D9 133-0 · P01 5H1

GRX130 10E7 14R1 · SED120 6E5 · SRD140 6R5 · SRD110 6R6 · DS20 223-0 · AX3P10 14K1 · DRX3P10 29G3 · SRD090 6R6 · SRD070 6R7

10R4 P11 · P20 969, 146 1 · SHORT 113-0

CALCULATE ADDRESS AND IR OP CODE LOGIC

NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-B BOARD.

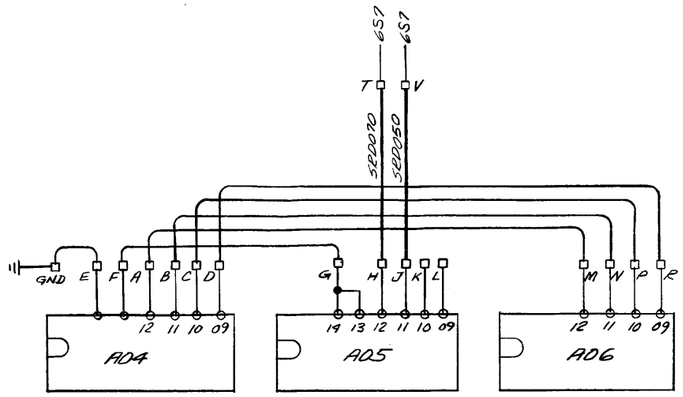
REVISIONS

NAME	TITLE	DATE
G. MELTON	DRAFT	3-20-74
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODELS 7/16H5AIII & 7/32C PROCESSOR

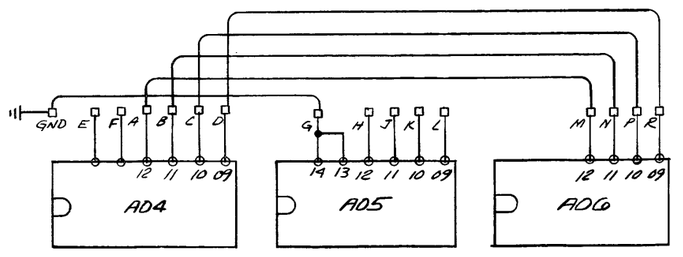
TASK NO. 03073 · DWG NO. 01-097 D08 · SHEET OF 8-36

BRUNING 44-231 16042

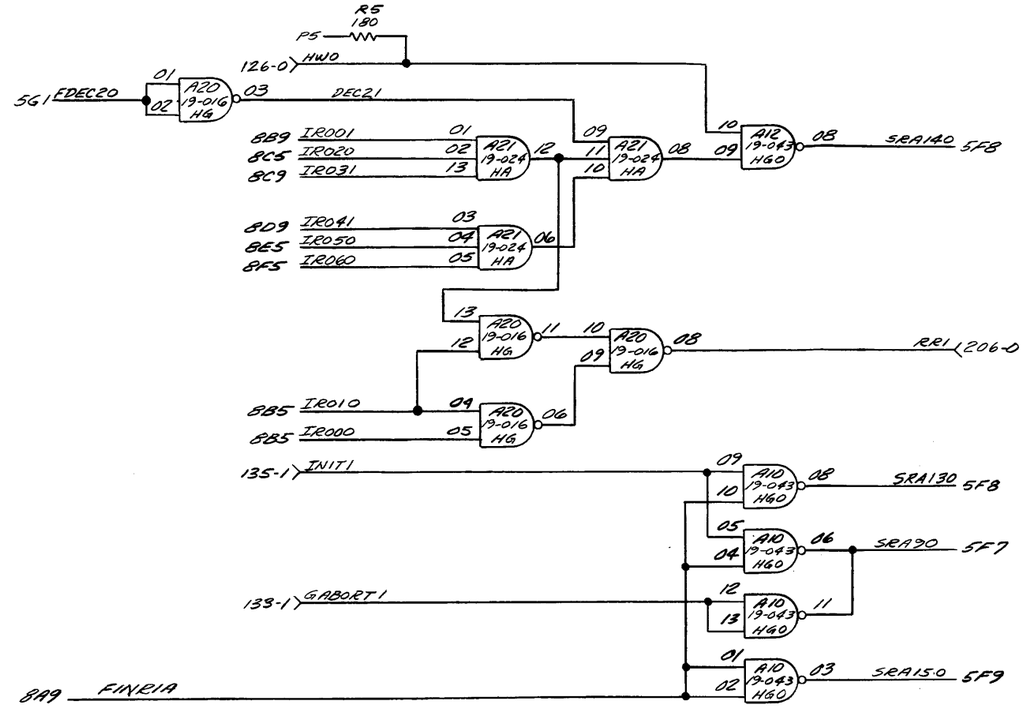


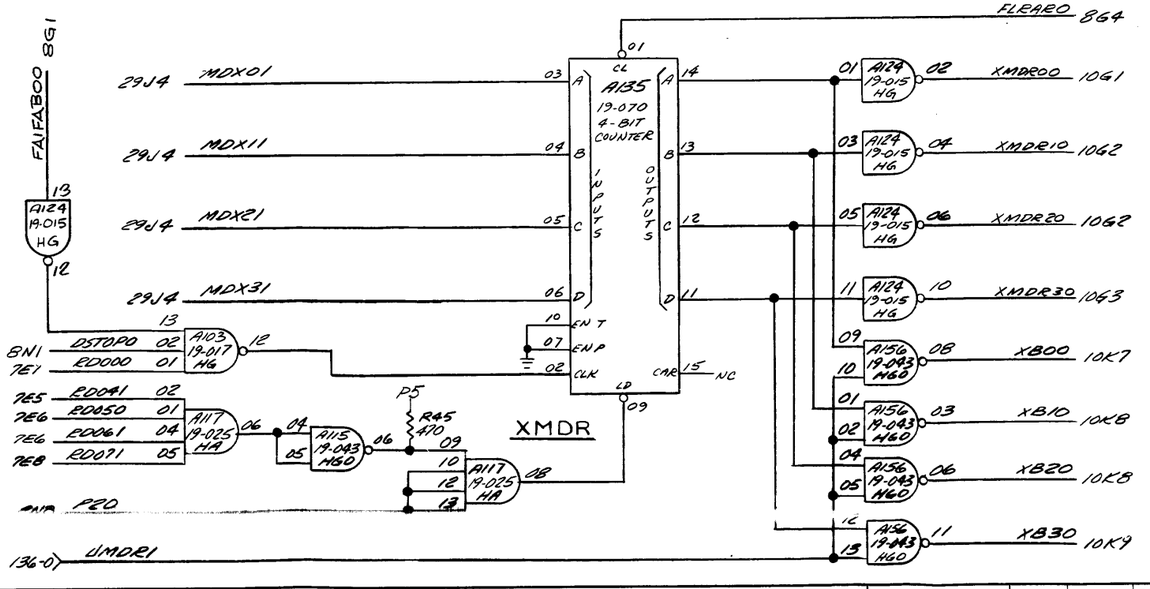
DEOM STRAPPING FOR 7/16 HSALU

FOR 7/32C BASIC INSTRUCTION SET STRAP "E" TO "H".
FOR 7/32C BASIC + COMM. INSTRUCTION SET STRAP "E" TO "H", "L".
FOR 7/32C BASIC + COMM. + SLO FLT POINT STRAP "E" TO "H", "L", "J".
FOR 7/32C BASIC + COMM. + FST FLT POINT STRAP "E" TO "H", "L", "K".
FOR 7/32C BASIC + SLO FLT POINT STRAP "L" TO "H", "J".
FOR 7/32C BASIC + FST FLT POINT STRAP "E" TO "H", "K".



DEOM STRAPPING FOR 7/32





STRAPPING OPTIONS FOR 7/32 & 7/16 HSALU

NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-B BOARD.

NAME	TITLE	DATE
V. PERRI	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODELS 7/16 HSALU & 7/32C PROCESSOR
TASK NO. 03073
DWG NO. 01-097 D08
SHEET 9 OF 36

INTERDATA®

STRAPPING OPTIONS	
7/32 W/ MEMORY ACCESS CONTROL OR DMABC	7/32 W/O MEMORY ACCESS CONTROL OR DMABC
TERMINAL 'A1' TO TERMINAL 'A3'	TERMINAL 'A2' TO TERMINAL 'A3'
TERMINAL 'B1' TO TERMINAL 'B3'	TERMINAL 'B2' TO TERMINAL 'B3'
TERMINAL 'C1' TO TERMINAL 'C3'	TERMINAL 'C2' TO TERMINAL 'C3'
TERMINAL 'D1' TO TERMINAL 'D3'	TERMINAL 'D2' TO TERMINAL 'D3'

X BUS LOGIC

X MAR

X MAS

X LOC

4 BIT ALU

XB-BUS LATCH

SEE NOTE 2

SEE LEGEND IN AREA A1 FOR STRAPPING OPTIONS.

NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-B BOARD.
2. REMOVE JUMPER 'X' TO 'Y' W/MAC OR DMABC.
* NOT EQUIPPED ON 7/16 WITH HSALU.

REVISIONS

NAME	TITLE	DATE
G. MELTON	DRAFT	3-20-74
	CHK	
	ENGR	
	DIR ENG	

TITLE: FUNCTIONAL SCHEMATIC MODELS 7/16 HSALU & 7/32C PROCESSOR

ASY NO 03073 · DWG NO 01-097 D08 · SHEET 10 OF 36

INTERDATA®

REVISIONS

IMCMDO 14F9 · ED080 7K1 · ED090 7K2 · ED190 7S4 · ED200 7S5 · CMNDO 14E9 · AMODO 29E4 · ED101 7K3 · ED111 7K4 · YLS1 12H1 · ED081 7K1 · ED091 7K2 · SEE NOTE 2 · PSW271 111-0 · ED220 7S6 · ED230 7S7 · YHS1 12M1 · XBP1 RAD 1K · P5 · ED191 7S4 · ED201 7S5 · 13D1, 12B1, 10H5 · READO SCLEPOA 7A8 CLKIB 12A9 · CLKO 10A3 · DONO 23J2-0 20J2-1 · EEADI 12M1 · DSTORD 8N1 · DCLKO 10A5

GND 10S-3 · GND 11Z-3 · GND 10D-3 · P5 10I-3 · P5 10G-3 · N.C. 12D-3 · N.C. 11I-3 · TP1 ETTO 10S-3

A108 19-016 HG · A104 19-017 HG · A95 DC19-063 DSDFF · A74 19-029 HA · A170 19-017 HG · A116 19-025 HA · A99 19-029 HA

DCLK1A 12A8, 13A3

A126 19-119 · A137 19-119 · A149 19-119 · A160 19-119 · A171 19-119 · A161 19-119 · A172 19-119

1394 MEMSO · 1396 MEGRL00 · 1398 MEGRL10 · 1246 MEGRH00 · 1248 MEGRH10 · 1249 MEXR00 · 1249 MEXR10

REGISTER STACK DECODING

NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-B BOARD.
2. FOR 7/16 HSALU THIS POINT IS GROUNDED AT THE BACK PANEL.
* NOT EQUIPPED ON 7/16 WITH HSALU

NAME	TITLE	DATE
G. MELTON	DRAFT	3-21-74
	CHK	
	ENGR	
	DIR ENG	

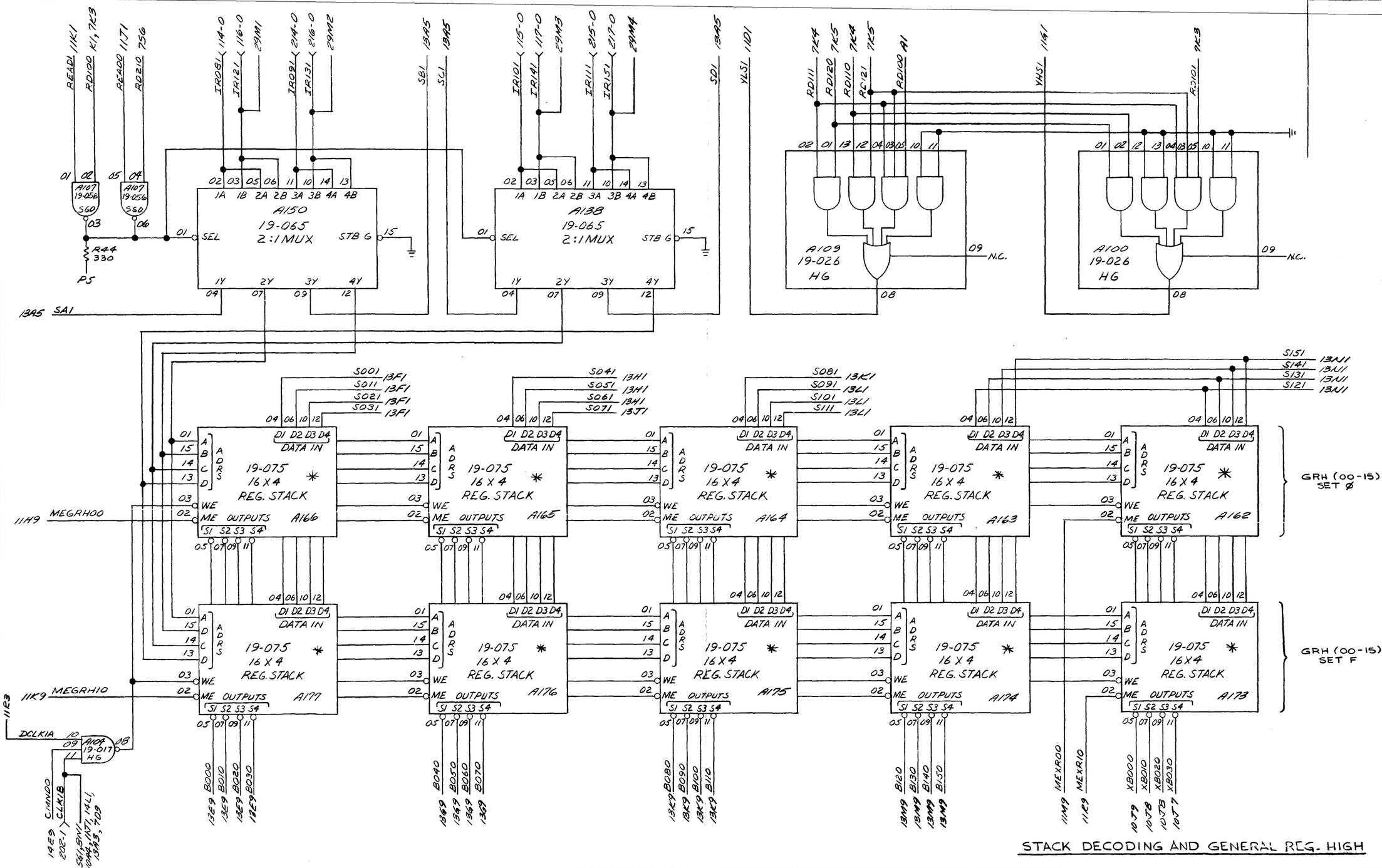
TITLE REFACTORIAL SCHEMATIC MODELS 7/16 HSALU & 7/32C PROCESSOR

TASK NO 03073 · DWG NO 01-097 008 · SHEET OF 11-36

BRUNING 44-231 11042

INTERDATA®

REVISIONS



STACK DECODING AND GENERAL REG. HIGH

NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-B BOARD.

* NOT EQUIPPED ON 7/16 WITH H5ALU.

NAME	TITLE	DATE	TITLE FUNCTIONAL SCHEMATIC
B GRAY	DRAFT		MODELS 7/16 H5ALU & 7/32C PROCESSOR
	CHK		
	ENGR		TASK NO. 03073
	DIR ENG		DWG NO. 01-097 D08 SHEET OF 12-36

BRUNING 44-231 16042

INTERDATA®

REVISIONS

A127 19-065 2:1 MUX STTL — ENB, SEL, 1Y 2Y 3Y 4Y; NC, NC, RD101, RD211, RD111, RD221, RD121, RD231, READO; 7K3 256, 7K4 257, 7K5 258, 11J1

A131 19-075 16x4 REG. STACK — A B C D ADDRS; D1 D2 D3 D4 DATA IN; WE; ME; OUTPUTS S1 S2 S3 S4; 119-1, 219-1, 116-1, 218-1, 1204, 1225, 1205, 1205; 5001, 5011, 5021, 5031

A130 19-075 16x4 REG. STACK — 217-1, 216-1, 115-1, 215-1, 1264, 1265, 1265, 1265; 5041, 5051, 5061, 5071

A129 19-075 16x4 REG. STACK — 114-1, 214-1, 113-1, 213-1, 1274, 1275, 1275, 1275; 5081, 5091, 5101, 5111

A128 19-075 16x4 REG. STACK — 29K1, 29G2, 29K5, 29K5; Y5121, Y5131, Y5141, Y5151

MR0 MR1 MR2 MR3 MR4 MR5 MR6 PSWL

18A9 CLKIB 03
11B3 DCLKIA 04
MEA9 CMNDO 05
1189 MEMSO
A109 19-017 HG — 06

S121 — 112-1 — 10A3, 29G2, 12R5
S141 — 111-1 — 10A3, 29G2, 12R4

1284 SA1
1261 SB1
12C1 SC1
12A1 SD1
11D9 MEGRLOO

A142 19-075 16x4 REG. STACK — B000, B010, B020, B030; 102-0, 202-0, 103-0, 203-0; 8289,12,9, 8289,12,9, 8289,12,9, 8C9,12,9
A141 19-075 16x4 REG. STACK — B040, B050, B060, B070; 104-0, 204-0, 105-0, 205-0; 8C9,12,9, 8C9,12,9, 8C9,12,9, 8C9,12,9
A140 19-075 16x4 REG. STACK — B080, B090, B100, B110; 106-0, 206-0, 107-0, 207-0; 1265,12,9, 1265,12,9, 1265,12,9, 1265,12,9
A139 19-075 16x4 REG. STACK — B120, B130, B140, B150; 105-0, 205-0, 110-0, 210-0, 22-0; 7K2,1089,12,9, 7K3,1068,2C9, 7K4,1068,2C9, 7K5,1067,2C9

GRL (16-31) SET Ø

S131 — 212-1 — 10A3, 29G2, 12R4
S151 — 211-1 — 10A3, 29G2, 12R4

A154 19-075 16x4 REG. STACK * — 11F9 MEGRLIO
A153 19-075 16x4 REG. STACK *
A152 19-075 16x4 REG. STACK *
A151 19-075 16x4 REG. STACK *

GRL (16-31) SET F

C1 THRU C10 — 33 MFD. — P5
C11 THRU C73 — 0.1 MFD. — P5

DECOUPLING CAPACITORS

REGISTER STACKS

NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-B BOARD.

* NOT EQUIPPED ON 7/16 WITH HSALU

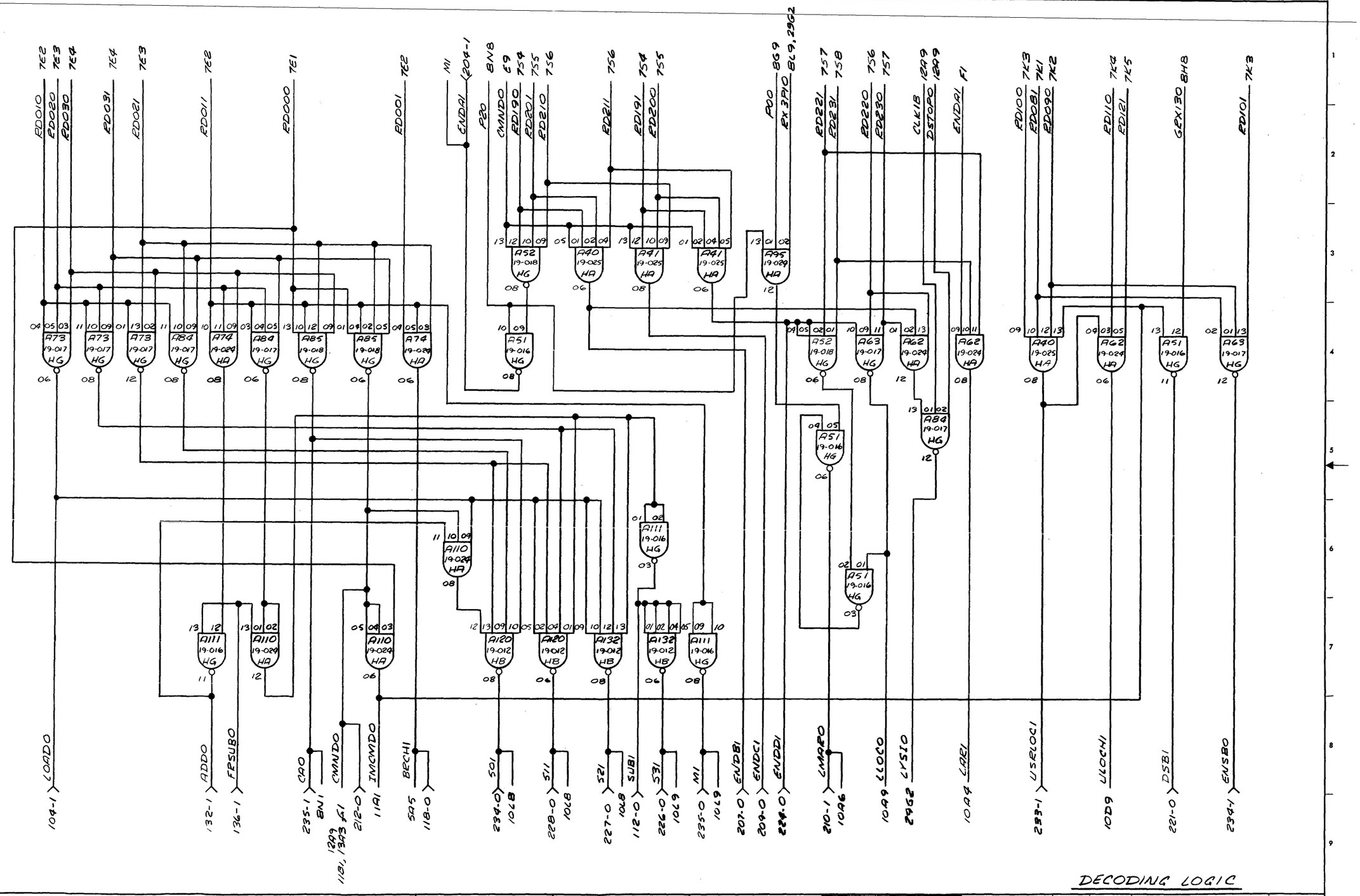
NAME	TITLE	DATE
CHRIS JENSEN	DRAFT	23OCT73
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODELS 7/16 HSALU & 7/32C PROCESSOR

TASK NO 03073 DWG NO 01-097 D08 SHEET OF 13-36

BRUNING 44-231 16C42

INTERDATA®



DECODING LOGIC

NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-B BOARD.

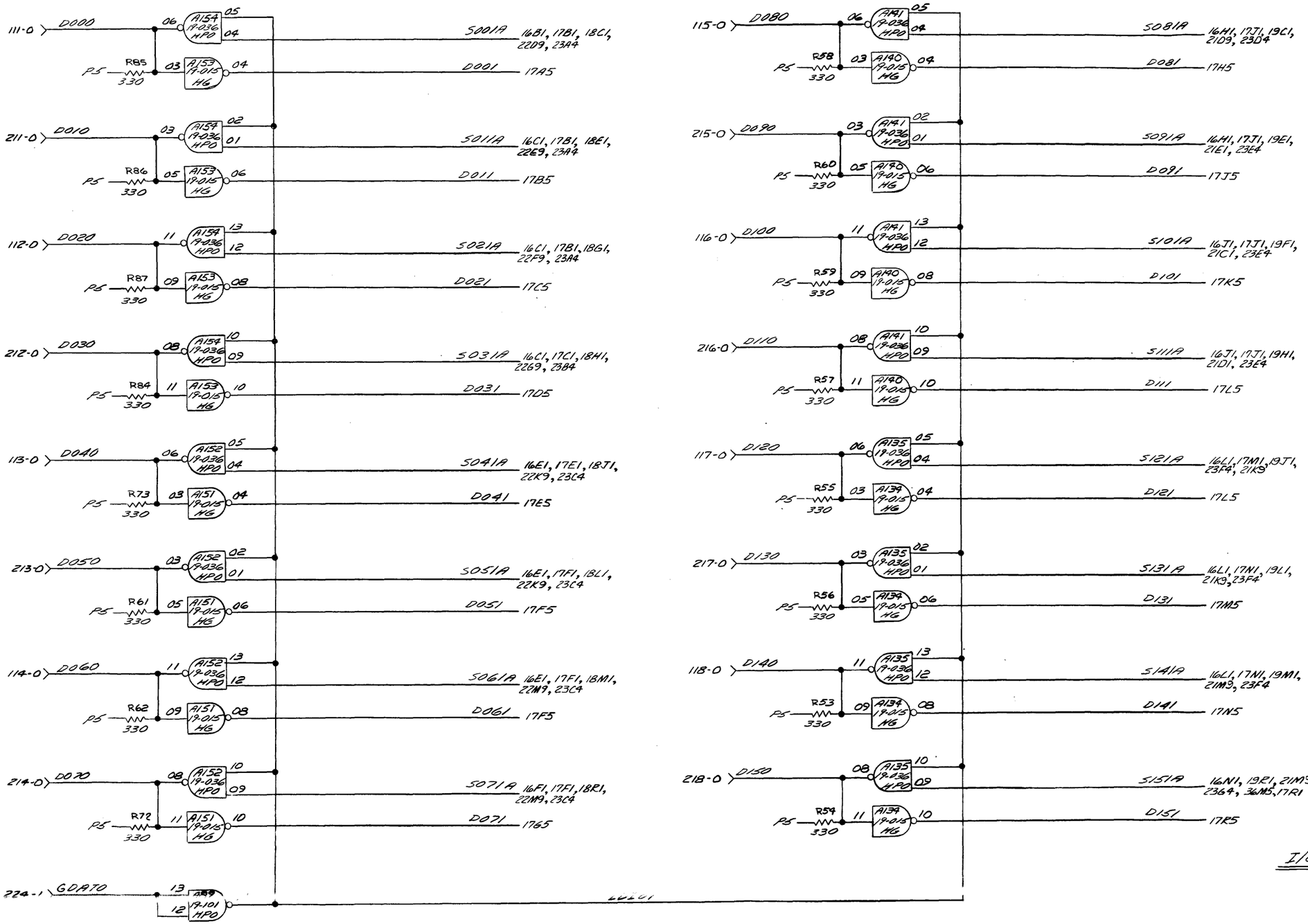
REVISIONS

NAME	TITLE	DATE
G. MELTON	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODELS 7/16 HSALU & 7/32 PROCESSOR

TASK NO. 03073
DWG NO. 01-097
SHEET 14 OF 36

BRUNING 44-231 16042



I/O DRIVERS & RECEIVERS

NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-C BOARD, 35-524 M01.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 5 7/16 HSALU 67/32C PROCESSOR
TASK NO. 030173
DWG NO. 01-097 D08
SHEET OF 15-36

BRUNING 44-231 16042

INTERDATA®

MAR

MAS

W/ MAC OR DMABC	W/O MAC OR DMABC
A1 - A3	A2 - A3
B1 - B3	B2 - B3
C1 - C3	C2 - C3
D1 - D3	D2 - D3
E1 - E3	E2 - E3
F1 - F3	F2 - F3
G1 - G3	G2 - G3
H1 - H3	H2 - H3
REMOVE J1 - J2	J1 - J2

STRAPPING OPTIONS

MAR & MAS

NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-C BOARD, 35-524 MOI.

REVISIONS

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODELS 7/16 HSALU & 7/32X PROCESSOR

TASK NO. 23073 DWG NO. 01-097 DAB

SHEET OF 16-36

BRUNING 44-231 16042

INTERDATA®

LOC

LOCATION COUNTER & B BUS MUX

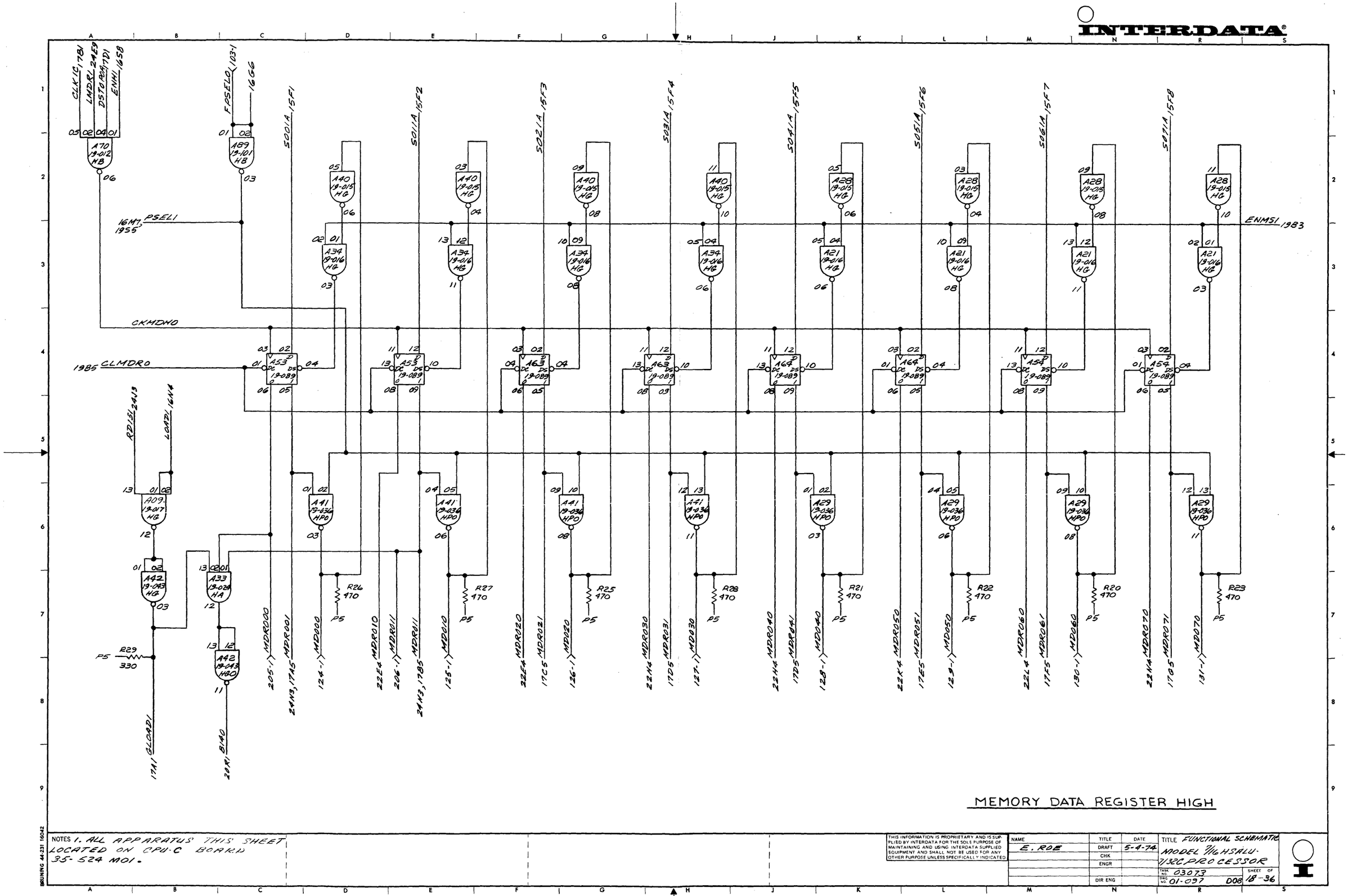
NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-C BOARD, 35-524 MOI.

NAME	TITLE	DATE
E. ROE	DRAFT	5-8-74
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 7/16 MSALU-7/32C PROCESSOR

TASK NO. 03073
DWG NO. 01-097 D08
SHEET 17 OF 36

BRUNING 44-231 16042



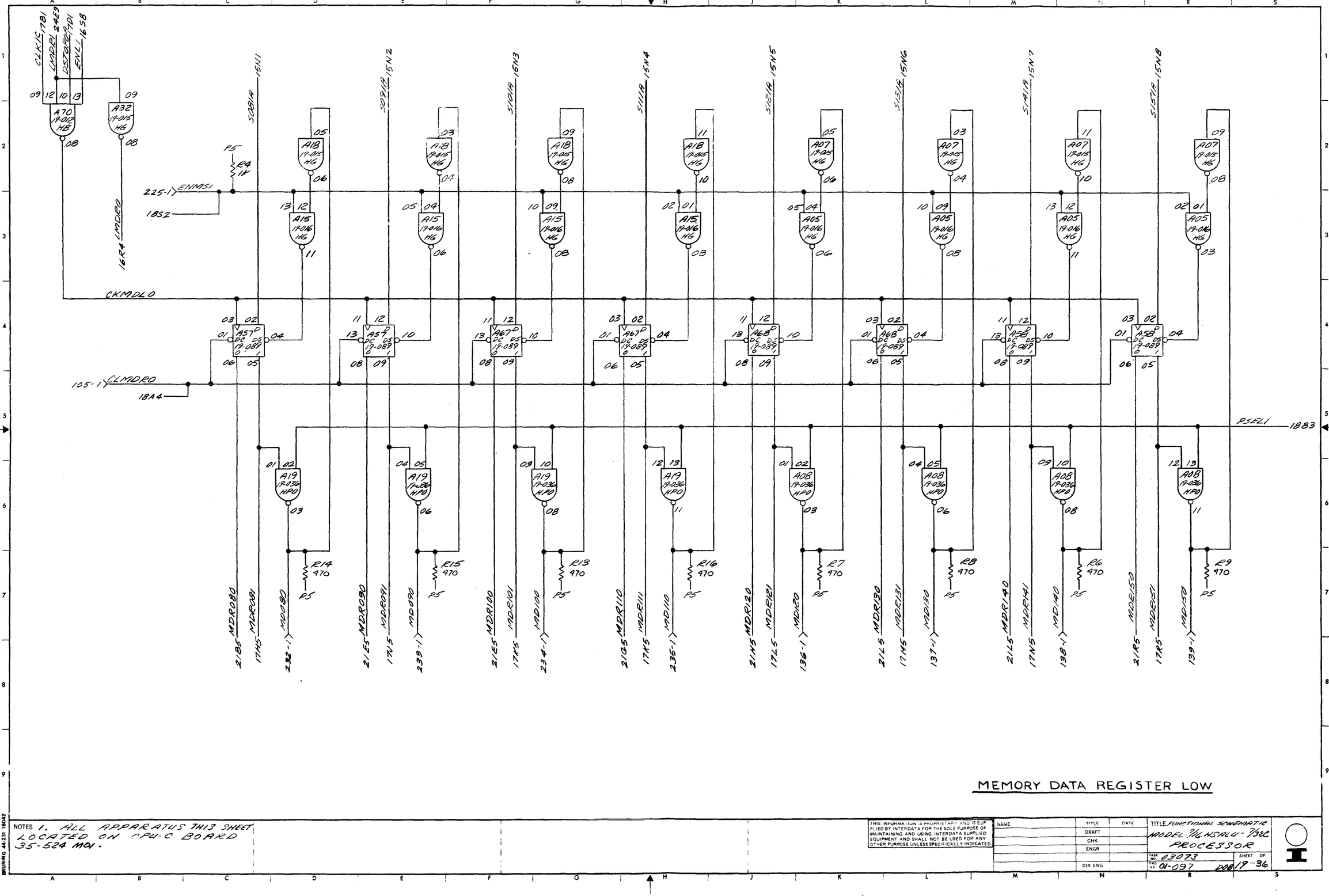
MEMORY DATA REGISTER HIGH

NOTES 1. ALL APPARATUS THIS SHEET LOCATED ON CPU-C BOARD 35-524 M01.

NAME	TITLE	DATE
E. ROE	DRAFT	5-4-74
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 7/16 HSALU-7/32C PROCESSOR
TASK NO. 03073
DWG NO. 01-097 D08
SHEET 18 OF 36

BRUNING 44-231 16042



MEMORY DATA REGISTER LOW

NOTES 1. ALL APPARATUS THIS SHEET LOCATED ON CPU-C BOARD 35-524 MDI.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 7/16 HSALU-7/32C
PROCESSOR

TASK NO 03073
TIMS NO 01-097 DOC

SHEET 18 OF 36

BRUNING 44-231 16042

INTERDATA

B-BUS SHIFTER & LATCH

NOTES
1. ALL APPARATUS ON THIS SHEET LOCATED ON CPU-C BOARD, 35-524 M01.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODELS 7/16 H SALU & 7/32C PROCESSOR

TASK NO. 03073 DWG NO. 01-097 D08 SHEET OF 20-36

BRUNING 44-231 16042

REVISIONS

FUNCTION	RD 1	RD 2	RD 3	M	S_0	S_1	S_2	S_3
LOAD	0	0	0	1	1	1	1	1
AND	0	0	1	1	0	1	1	1
OR	0	1	0	1	1	1	0	1
XOR	0	1	1	1	1	0	0	1
ADD	1	0	0	0	1	0	0	1
SUB	1	0	1	0	0	1	1	0
CMD	1	1	1	0	1	0	0	1
CA	1	1	0	0	1	0	0	1

NOTES:
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-C BOARD, 35-529 M01.
2. ✱ CORRESPONDING TO IC IN POS. A119 THRU A122 INDICATES IC'S ARE INSTALLED WITH PIN 1 IN UPPER RIGHT HAND CORNER.

ALU LOW

NAME

TITLE FUNCTIONAL SCHEMATIC
MODEL 7/16 HSALU-7/32C
PROCESSOR

DWG 03073
REV 01-097 DOB
SHEET 21 OF 36

INTERDATA®

ALU HIGH

NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-C BOARD, 35-524 M01.
2. ** CORRESPONDING TO IC IN POS. A115 THRU A118 INDICATES IC'S ARE INSTALLED WITH PIN1 IN UPPER RIGHT HAND CORNER.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 7/16 HSALU - 7/32C
PROCESSOR

TASK NO 03073
DWG NO 01-097 D08
SHEET OF 22-36

BRUNING 44-231 16042

INTERDATA

TRUTH TABLE 19-048

S1	S0	FUNCTION
0	0	NO OP
0	1	SHIFT RIGHT
1	0	SHIFT LEFT
1	1	LOAD

D9 SRH1111 — A100 19-044 HG0 — 01, 02
D9 SRH1101 — A100 19-044 HG0 — 03, 04
D9 SRH1091 — A100 19-044 HG0 — 13, 12
A100 19-044 HG0 — 05, 06 — NORM0 — 110-1
RS1 470 — P5

208-1 RD120 — 24F3
17B5 RD111A — 24F3,29F1
108-1 RD110
133-1 USRLOC1
A50 19-015 HG — 01, 02 — RD121A 17B5,29E1
A50 19-015 HG — 13, 12
A49 19-017 HG — 09, 10, 11, 08
A49 19-017 HG — 03, 04, 05, 06
36L4 MD0
A92 19-036 HB — 04, 05, 06 — R36 470 — USRH1 — D9
A92 19-036 HB — 01, 02, 03 — R37 470 — USRL1A — K9
SHCLK0 239-1 — 36J3

CISH1 36K9; SRH0H 29F7; SRH0L 29F8
CLSRH0 36J1; USRH1 29F7; SRH1H 29F8; SRH1L 29E8; SRH0L 29E8
CISRL1 36M9; USRL1A 29E8; SRL1H 24F8; SRL1L 24E8; FMPY1 36N7; SELI61 24C8
SELSI1 230-1; SELSO1 231-1; SELI51 36M5; SELO01 36N

A98 19-048 SHIFT REG. SRH — A102 19-048 SHIFT REG. SRH — A83 19-048 SHIFT REG. SRL — A87 19-048 SHIFT REG. SRL
R S0 S1 A B C D INPUT; CLEAR; E F G H L INPUT; CLK; OUTPUT A B C D; OUTPUT E F G H

A97 19-043 HG0 — 2011,H 8000; 2018,A 8010; 2026,B 8020; 2034,C 8030; 2042,D 8040; 2050,E 8050; 2058,F 8060; 2066,G 8070
A101 19-043 HG0 — 2012,H 8080; 2019,A 8090; 2027,B 8100; 2035,C 8110; 2043,D 8120; 2051,E 8130; 2059,F 8140; 2067,G 8150
A90 19-043 HG0 — 2014,H 8000; 2021,A 8010; 2029,B 8020; 2037,C 8030; 2045,D 8040; 2053,E 8050; 2061,F 8060; 2069,G 8070
A91 19-043 HG0 — 2013,H 8080; 2020,A 8090; 2028,B 8100; 2036,C 8110; 2044,D 8120; 2052,E 8130; 2060,F 8140; 2068,G 8150
A93 19-043 HG0 — 2015,H 8080; 2022,A 8090; 2030,B 8100; 2038,C 8110; 2046,D 8120; 2054,E 8130; 2062,F 8140; 2070,G 8150
A94 19-043 HG0 — 2017,H 8080; 2024,A 8090; 2032,B 8100; 2040,C 8110; 2048,D 8120; 2056,E 8130; 2064,F 8140; 2072,G 8150

A85 19-063 — 12 D 1 09; 11 DC 0 08; 10 PS 13

SHIFT REGISTER

NOTES 1. ALL APPARATUS THIS SHEET LOCATED ON CPU-C BOARD 35-529 M01.

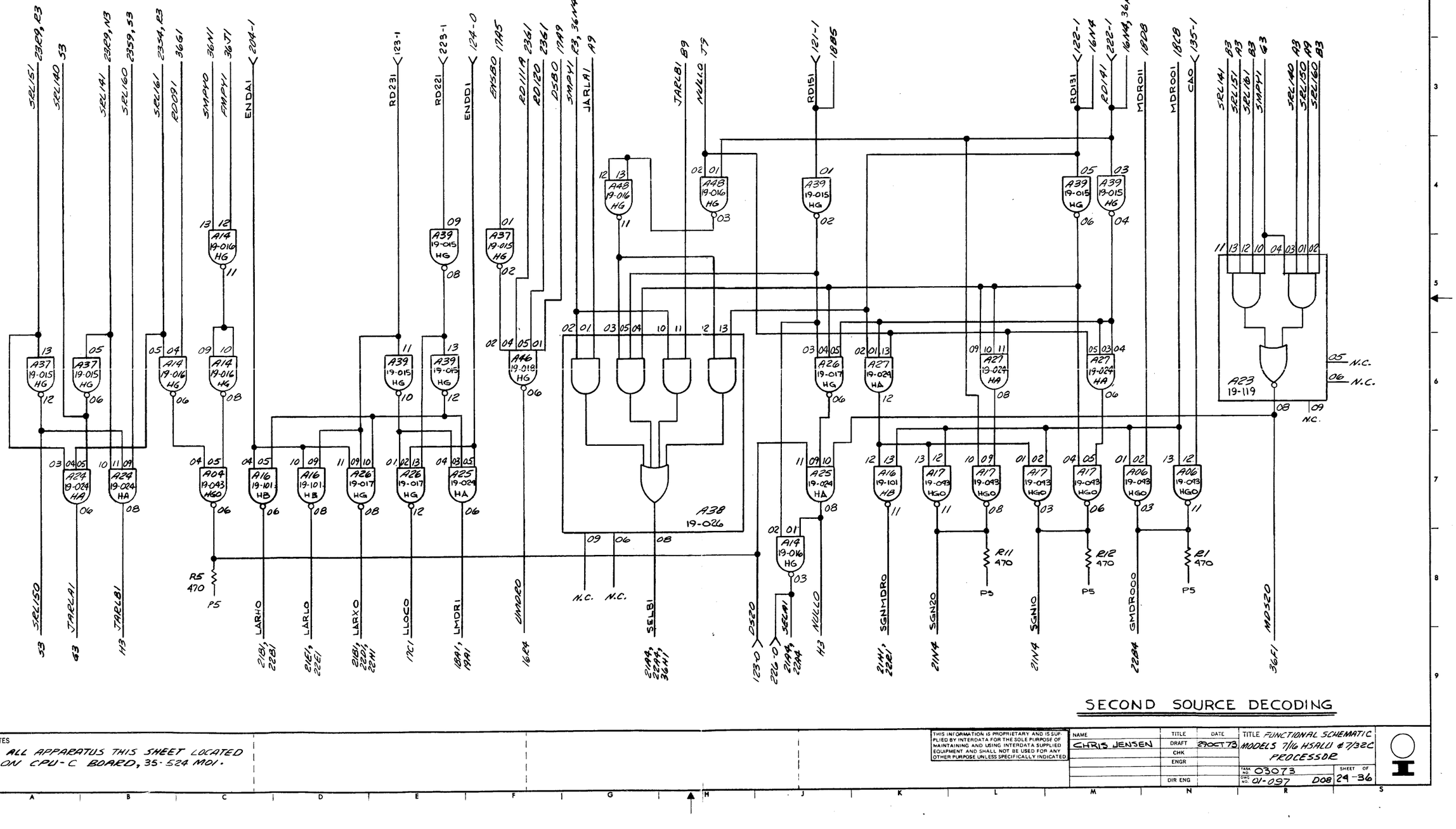
REVISIONS

NAME | TITLE | DATE
DRAFT
CHK
ENGR
DIR ENG

TITLE FUNCTIONAL SCHEMATIC MODEL 7/16 MSALU-7/32C PROCESSOR
TASK NO 03073
DWG NO 01-097 D08
SHEET 23 OF 36

BRUNING 44 231 16042

INTERDATA®



SECOND SOURCE DECODING

NOTES

1. ALL APPARATUS THIS SHEET LOCATED ON CPU-C BOARD, 35-524 MOI.

NAME	TITLE	DATE
CHRIS JENSEN	DRAFT	29OCT73
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODELS 7/16 HSALU & 7/32C PROCESSOR

TASK NO 03073 DWG NO 01-097 D08 SHEET OF 29-36

DRWING 44-231 16042

INTERDATA®

I/O TIMING & CONTROL

NOTES
1. ALL APPARATUS ON THIS SHEET LOCATED ON CPU-A BOARD 35-624.
2. REMOVE THIS JUMPER TO INCREASE MINIMUM WIDTH OF ADRSO # DACKO.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCT. SCHEMATIC
MODEL 7/16 HSALU 7/32C
PROCESSOR

TASK NO. 03073
DWG NO. 01-097 D08
SHEET 25 OF 36

INTERDATA®

R30 2.2K P5 — R31 22 — C71 1000PF — R36 2.2K — R35 22 — C73 1000PF — R33 22 — C72 470PF — R32 2.2K P5

103-3 ESNCO — 104-3 ESNOO — 106-3 SSGLI

A73 19-016 HG — A62 19-115 HA

TP14 GND — TP1 SCATNO — R38 1K P5 — XRPIA

A74 19-089 HDFF — CONSOLE ATTENTION F/F — FCATNI 31HI — GADRO — NC

XRPIA — 25N9

A74 19-089 HDFF — SINGLE F/F — FSNGLI 31GI — NC

32E5 SCLRDA

A50 19-036 HPO — SRGO — R21 1K P5 — 113-3

25D9 SRO — 25B9 DRO — 25C9 CMDO — 25C9 DAO — 25A9 KENDRAI — 25E9 FCOUTI

A142 19-015 HG — A38 19-016 HG — SRGOA

A47 19-016 HG — POLACKO

A01 19-024 HA — A02 19-015 HG — CMG1

A62 19-115 HA — ADR1

A14 19-095 FF — INCREMENTAL F/F

K6 S151 — A01 19-024 HA — A02 19-015 HG

3IE4 S061 — A60 19-015 HG

M1 S080 — M2 S090 — M2 S100 — M3 S110 — M4 S120 — M5 S130 — M15 S140 — A13 19-025 HA — A01 19-024 HA

3IE4 S071 — A60 19-015 HG

K2 S091 — K1 S081

A50 19-036 HPO — FWAITO 34C9 — R27 1K P5 — 31DI, 34HI — WAITI 102-3

A141 19-036 HPO — R71 1K P5 — C79 470PF — A141 19-036 HPO — R67 180 P5 — SYNO 25LI — 123-0

XRPID — R20 1K P5 — DR COUNTER

A61 19-089 HDFF — A51 19-015 HG — A49 19-101 B — R26 1K P5 — SHIO 200-3 — R23 1K P5 — SLOO 206-3

DA COUNTER — A61 19-089 HDFF — A51 19-015 HG — A49 19-101 B — R6 1K P5 — LBO 114-3 — R24 1K P5 — LAO 203-3

A6, 34KI

P5 R7 1K — XRPIC

A26 19-036 HPO — R13 1K P5 — FINCRO

A02 19-015 HG — A26 19-036 HPO — A02 19-015 HG — 02 SCLRDD 107-3

DRGO — SRGOA

A60 19-015 HG — A25 19-036 HPO — A168 19-093 HGO — R9 1K P5 — SDOI 109-3

114-1 S081 D8 — 106-0 B080 — A7 S080

219-1 S091 D8 — 107-0 B090 — A7 S090 — R12 1K P5 — SD11 110-3

113-1 S101 — 108-0 B100 — A7 S100 — R11 1K P5 — SD21 111-3

213-1 S111 — 208-0 B110 — A7 S110 — R10 1K P5 — SD31 112-3

A72 19-015 HG — A37 19-036 HPO — A167 19-093 HGO

112-1 S121 30GI 34JI — 30B9 109-0 B120 — A7 S120 — R18 1K P5 — SD41 202-3

212-1 S131 30JI 34JI — 25K9, 28L5, 30C9 110-0 B130 — A7 S130 — R17 1K P5 — SDSI 204-3

111-1 S141 34JI — 28K5, 30D9 210-0 B140 — A8 30LI S140 — R19 1K P5 — SD61 205-3

211-1 S151 — 30N4 28K7, 30E9 222-0 B150 — A7 S150 — R20 1K P5 — SD71 208-3

DRGO — SRGOA — A73 19-016 HG — A129 19-115 HA

25G9 FDATI — 25J9 FSYNI

TO DISPLAY PANEL

DISPLAY CONTROL LOGIC

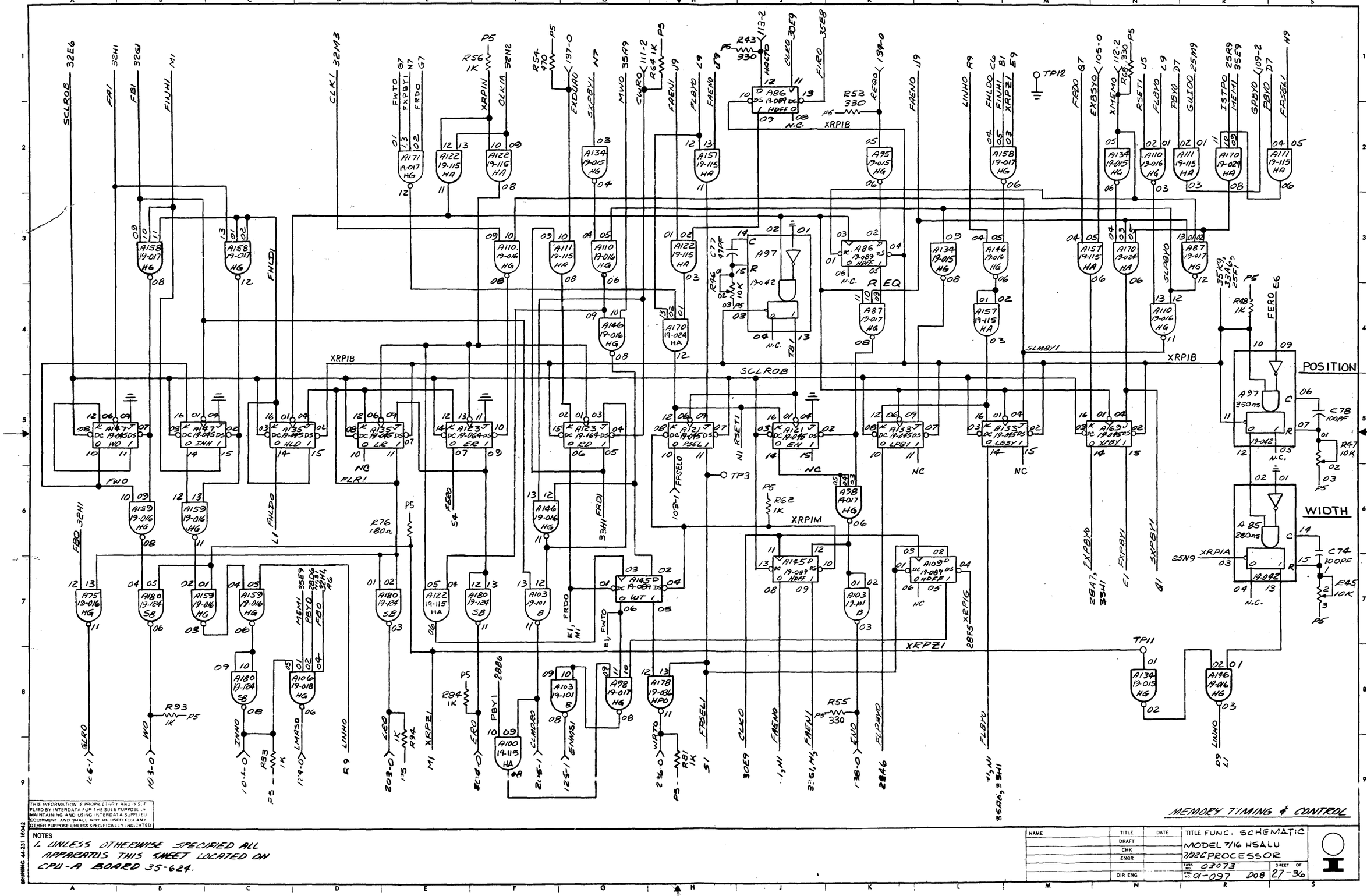
NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-A BOARD 35-624.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE: FUNCTIONAL SCHEMATIC MODEL 7/16 HSALU 7/32C PROCESSOR
TASK NO. 03073
DWG NO. 01-097 D08
SHEET OF 26-36

BRUNING 44-231 16042

INTERDATA®



NOTES
1. UNLESS OTHERWISE SPECIFIED ALL APPARATUS THIS SHEET LOCATED ON CPU-A BOARD 35-624.

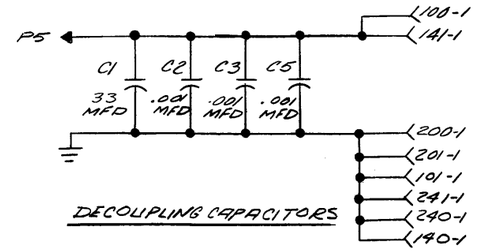
NAME	TITLE	DATE	TITLE FUNC. SCHEMATIC
	DRAFT		MODEL 7/16 HSALU
	CHK		7/32 CPROCESSOR
	ENGR		TASK NO 03073 SHEET OF
	DIR ENG		DWG NO 01-097 D08 27-36

MEMORY TIMING & CONTROL

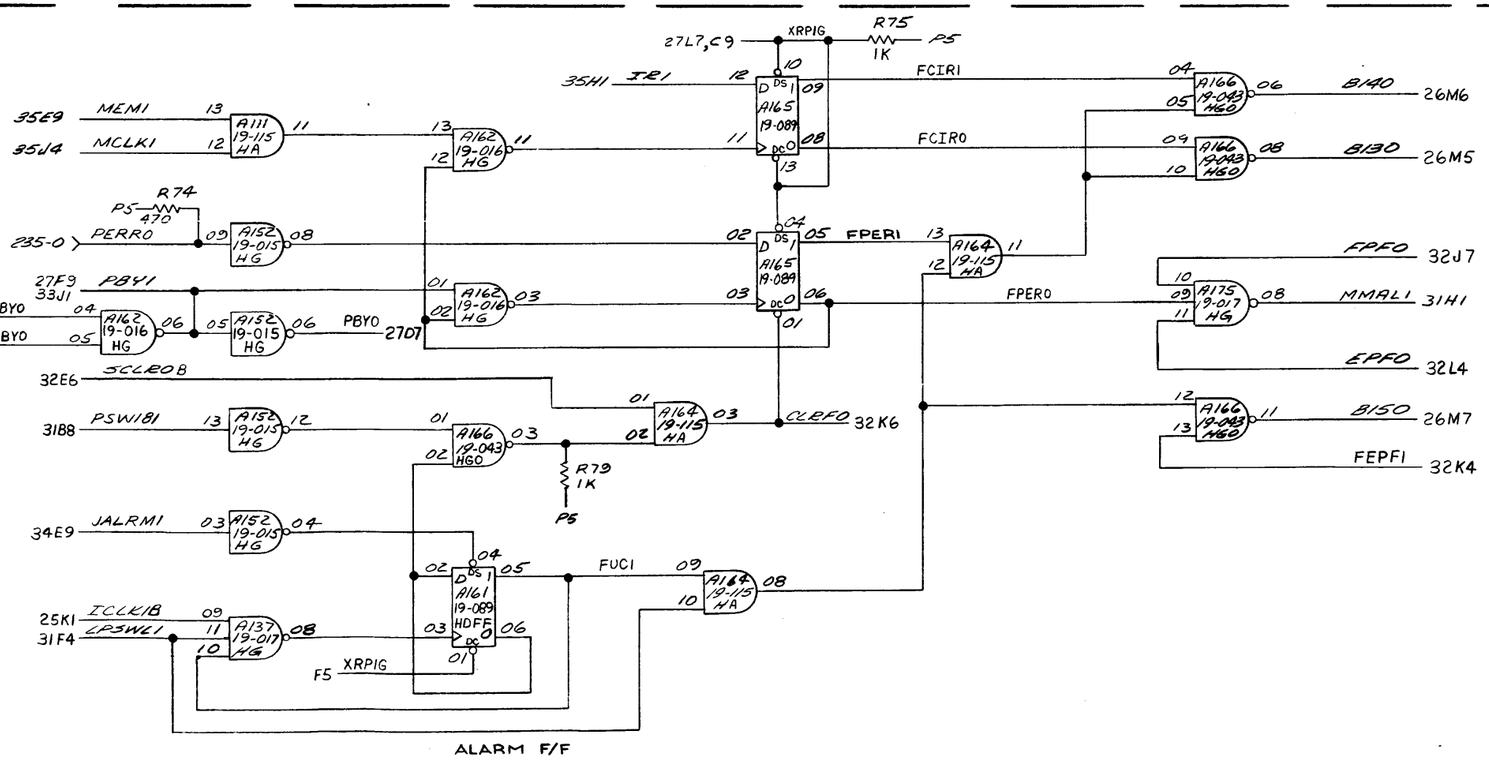
BRUNING 44-231 18042

INTERDATA®

REVISIONS



DECOUPLING CAPACITORS



ALARM F/F

MEMORY PARITY & ALARM REGISTER

NOTES

1. UNLESS OTHERWISE SPECIFIED ALL APPARATUS THIS SHEET LOCATED ON CPU-A BOARD 35-624.

2. THIS OPTION, WHEN EQUIPPED, IS INSTALLED AT THE BACK PANEL ON SLOT 3, CONNECTOR 1.

NAME	TITLE	DATE
	DRAFT	4-23-74
	CHK	
	ENGR	
	DIR ENG	

TITLE
FUNCTIONAL SCHEMATIC
MODEL 7/16 HSALU 7/32C
PROCESSOR

TASK NO. 03073
DWG NO. 01-097 D08
SHEET OF 28-36

BRUNING 44-231 16042

INTERDATA®

PART OF CPU-C BOARD 35-524 M01

PART OF CPU-B BOARD MOD 7/32 ——— 35-625

A MOD F/F

PART OF CPU-A BOARD 35-624

YD & YS LOGIC

A156 19-035 4 BIT COUNTER

NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-A BOARD EXCEPT FOR AREAS DESIGNATED CPU-B & CPU-C BOARDS.

REVISIONS

NAME | TITLE | DATE
DRAFT
CHK
ENGR
DIR ENG

TITLE: FUNCTIONAL SCHEMATIC MODELS 7/16 HSA/D 4/32C PROCESSOR

TASK NO. 03073
DWG NO. 01-097 D08
SHEET OF 29-36

BRUNING 44-231 16042

INTERDATA®

FLAGS AND CONDITION CODES

NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-A BOARD 35-624.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 7/16 HSALU 7/32C PROCESSOR

TASK NO. 03073 SHEET 30 OF 36
DWG NO. 01-097 D08

BRUNING 44-231 16042

INTERDATA®

REVISIONS

BRANCH CIRCUITS AND PSW

NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-A BOARD, 35-624.
2. REMOVE STRAP FROM TP13 TO TP4 FOR POWER FAIL / AUTO RESTART OPTION
3. STRAP 3 TO 4 WHEN INSTALLING FAST FLOATING POINT OPTION.

NAME | DATE
DRAFT
CHK
ENGR
DIR ENG

TITLE FUNC. SCHEMATIC
MODEL 7/16 HSALU 7/32C
PROCESSOR
03073
01-097 D08
SHEET 31 OF 36

BRUNING 44.231 16042

INTERDATA®

REVISIONS

OSC1 36A5 L7
A16 19-015 HG
OSCO
R2 1K
XRPIF
A41 19-063
NC
R4 470
4.7uH L1
22-018 9-35AF C70
R3 2.2K
FB1 27B1
FA1 27A1, 36A5
FB0 27D7
A96 19-115 HA
CLK1B 202-1
CLK1C 203-1
CLK1A 25E1, 27F1, 29D7, 34A1, 35K1
CLK1 25H1, 30F1, 27D1, 36A5, 31H1
A75 19-016 HG
FAIFB00 237-0
FAIFB01 35A1
A177 19-016 HG
R82 1K
P/O SCLR RELAY A17-9
A178 19-036 HPO
SCLRO 126-0
R80 330
A41 19-044 HGD
ST0100
R16 1K
R85 10K
C81 2.2UF
D2
A173 19-092
NC
XRPIH
R78 1K XRPIH
A174 19-089
FEPF1
FEPF0 NC
A175 19-017 HG
PSWIB1 31B9
EPF0 28L6
FEPF1 28L7
FAIFB01
DSTOP0
OSC1 33G9 C1
A19 19-017 HG
DONO 132-0
GLRF0 28K8
A176 19-101 B
SCLR0A 234-0
26A3, 35B9
SCLR0C 25A1, 33D9, 35J9, 36C1, 34C1, 34M1
SCLR0B 25E1, 27A1, 28B1
EARLY POWER FAIL F/F
R77 22K
C80 15MF
A173 19-042
1MS TIMER
A174 19-089
FPF1 31K9
FPF0 28L5
POWER FAIL F/F
P/O DISPLAY
P0FF0 105-3
INIT0 101-3
D 23-001
PFDT0
R86 22
C82 1000 pf
25A1 PDN1
A178 19-036 HPO
R88 470
D3
POWDN0 128-0
R92 47K
R91 (AVAIL)
R90 (AVAIL) P15 102-0
C83 33MF
C84 33MF
34D9 FPOW1
R87 2.2K
R95 220
Q2 20-010
Q1 20-010
N.C. N.C.
PARO
PFDT0
236-1
134-0
202-0

OSCILLATOR & INITIALIZE RELAY

NOTES
1. UNLESS OTHERWISE SPECIFIED ALL APPARATUS THIS SHEET LOCATED ON CPU 'A' BOARD, 35-624.
2. THIS OPTION, WHEN EQUIPPED, IS INSTALLED AT THE BACKPANEL ON SLOT 7, CONNECTOR 0.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE: FUNCTIONAL SCHEMATIC MODEL 7/6 H5A1J 7/32C PROCESSOR
TASK NO. 03073
DWG NO. 01-097 DOB
SHEET 32 OF 36

BRUNING 44-231 16042

INTERDATA®

REVISIONS

CLOCK STOPS.

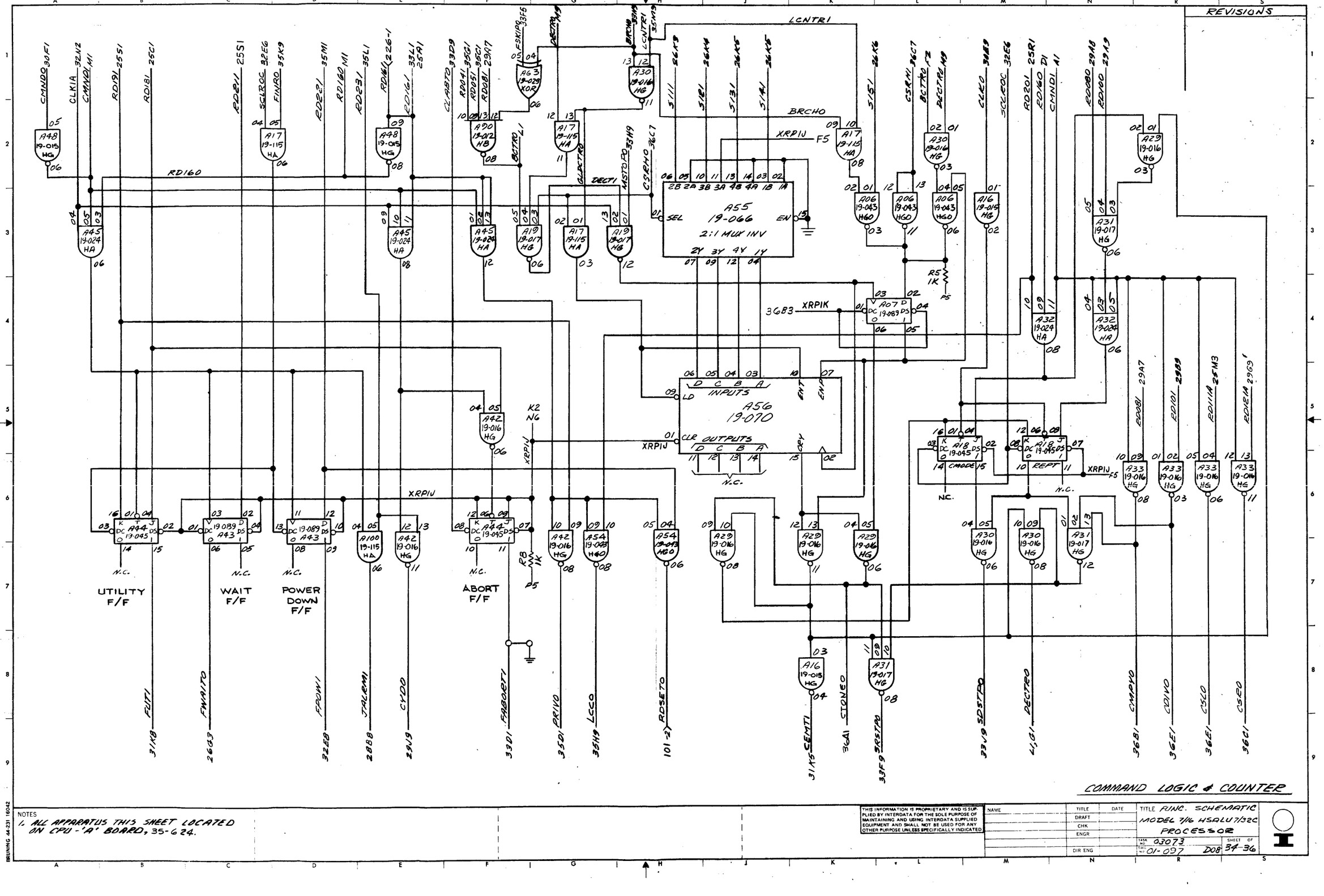
NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-A BOARD, 35-624.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNC. SCHEMATIC
MODEL 7/16 H SALU 7/32C PROCESSOR
TASK NO. 03073
DWG NO 01-097 D08
SHEET OF 33-36

INTERDATA®

REVISIONS



NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU - 'A' BOARD, 35-624.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNC. SCHEMATIC
MODEL 7/16 HSALU 7/32C
PROCESSOR
TASK NO 03073
TASK NO 01-097 D08
SHEET OF 34-36

BRUNING 44-231 16042

INTERDATA®

FIELD CONTROL LOGIC

NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-A BOARD, 35-624.

REVISIONS

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNC. SCHEMATIC
MODEL 7/16 HSALU 7/32C
PROCESSOR
TASK NO. 03073
DWG NO. 01-037 DOB
SHEET OF 35-36

BRUNING 44-231 16042

INTERDATA

REVISIONS

SHIFT REGISTER CONTROL

PART OF CPU-A BOARD 35-624

MULTIPLY LOGIC

PART OF CPU-C BOARD 35-524

DECOUPLING CAPACITORS

P5 .1MF C9 THRU C69 .1MF

P5 15MF C1 THRU C8 15MF

DECOUPLING CAPACITORS

P5 .1MF C11 THRU C56 .1MF

P5 33MF C1 THRU C10 33MF

NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-A BOARD, 35-624. EXCEPT FOR AREA DESIGNATED CPU-C BOARD 35-524 M01.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 7/16 HSALU 7/32C PROCESSOR

TASK NO. 03073
DWG NO. 01-097 D08
SHEET OF 36-36

REVISIONS

ECR	DATE
PRODUCTION RELEASE	REV A 2-24-74
APPROVAL	PROD 4-15-74

REVISED TO SHOW R01 COPPER. A25 WAS ITEM 16. ADDED STRAP BETWEEN STAKES E1E2, AND TP8 J TP15. W2E WAS ITEM 40. ADDED W80.

PCB 03073 REV A
RELEASED FOR PRODUCTION
MFG. ENG. DAT 4-15-74

CPU-A
APP SIDE
25-847

61 TYP. 21 PLACES

10
2 REF
8
6
INSTAL APP. SIDE (6 PLACES)

6
INSTALL FAR SIDE (4 PLACES)

2 TYP.

11 TYP. (4 PLACES)

1

3

A A

3 REF.
9
.530 MAX
.062 REF.
.125 MAX.
7

PARTIAL VIEW A-A

NOTES:

1. HEADER STIFFNER (ITEM 3) TO BE SOLDERED TO GRID BUS AT 2 END POINTS & CENTER FRONT.
2. CONTACTS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO WAVE SOLDERING.

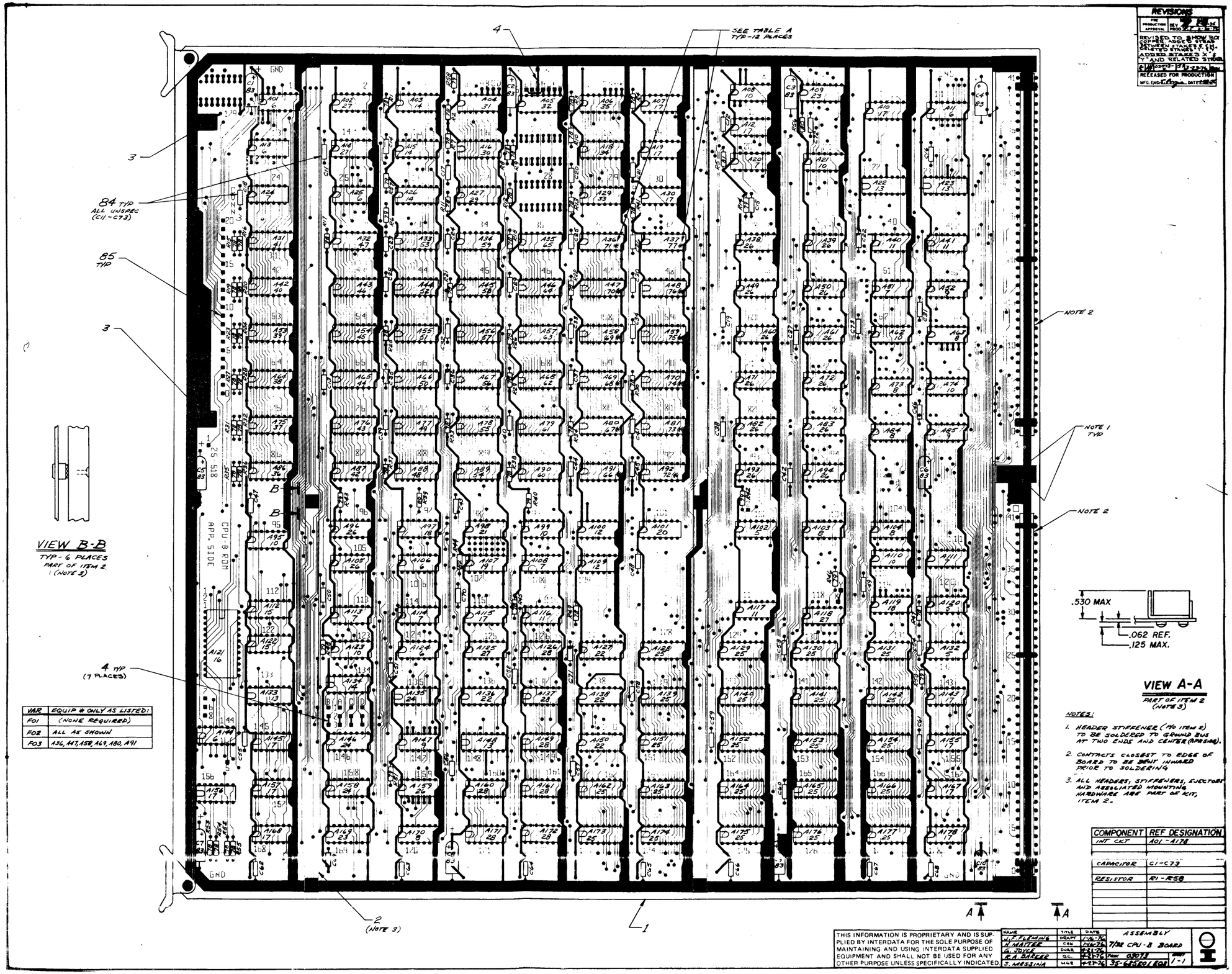
SEE NOTE 2

SEE NOTE 1

COMPONENT	REF DESIGNATION
INTEGRATED CKT	A1,A2,A4 THRU 14, A16 THRU 26, A28 THRU 38, A100 THRU 171, A173
RESISTOR	R1 THRU R89, R92 THRU R94
CAPACITOR	C1 THRU C75, C76 THRU C85
DIODE	D1 THRU D4
TRANSISTOR	Q1, Q2
INDUCTOR	L1

NAME	TITLE	DATE
F.EDWARDS	DRAFT	2-8-74
R.CERO	CHK	4-17-74
G.JOYCE	ENGR	4-15-74
R.BARKER	Q.C.	4-22-74
S.MESSINA	MGR	4-27-74

ASSY PRT. CKT. BD.
CPU-A
4SALU
03073
35-6284 R01
SIZE B
SHEET 1 OF 1



VIEW B-B
TYP - 6 PLACES
PART OF ITEM 2
(NOTE 3)

VAR	EQUIP # ONLY AS LISTED:
F01	(NONE REQUIRED)
F02	ALL AS SHOWN
F03	A36, A47, A58, A69, A80, A91

VIEW A-A
PART OF ITEM 2
(NOTE 3)

NOTES:

1. HEADER STIFFENER (1% ITEM 2) TO BE SOLDERED TO GROUND BUS AT TWO ENDS AND CENTER (PIN 50).
2. CONTACTS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.
3. ALL HEADERS, STIFFENERS, EJECTORS AND ASSOCIATED MOUNTING HARDWARE ARE PART OF KIT, ITEM 2.

COMPONENT	REF. DESIGNATION
INT. CKT	A01 - A178
CAPACITOR	C1 - C73
RESISTOR	R1 - R58

REVISIONS

FOR PRODUCTION APPROVAL	REV	BY
	PROD	

REVISED TO SHOW RC CONNECTION BETWEEN STAKES 15 & 16. DELETED STAKES X & Y AND RELATED STRAP.

RELEASED FOR PRODUCTION

MFG. ENG. _____ DATE _____

NAME	TITLE	DATE
W. FLEMING	DRAFT	1-24-76
H. MAITER	CKR	1-26-76
G. JOYCE	ENGR	4-6-76
R.A. SIEGER	QC	4-21-76
J. MESSINA	MGR	4-27-76

ASSEMBLY
7/32 CPU-B BOARD
DWG. 03073
SIZE D
SHT 1-1
35-665201 B08

NOTES:
1. STIFFENER BAR (ITEM 3) SHALL BE SOLDERED TO GND BUS AT 2 END POINTS & CENTER POINT.
2. CONNECTOR PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.

15.380 REF.

14.880 REF.

SEE NOTE 1

42 SEE NOTE 2

45 TYP 13 PLACES

SEE NOTE 1

43 TYP 26 PLACES

46 TYP 9 PLACES

42 SEE NOTE 2

3 SEE NOTE 1

A A

44

6 MOUNT ON SOLDER SIDE 2 PLACES

10 2 REF 8 6

ON ALL I.C. PACKS MARKED WITH AN ASTERISK (*), NOTE LOCATION OF I.C. ORIENTATION NOTCH, FACING HEADER, 14 PLACES.

CONN 3

CONN 9

CPU-E-BOARD 25-443 APP 5108

5 TYP.

4 TYP.

1

3 9 .530 MAX .062 REF. .125 MAX. 7

PARTIAL VIEW A-A

REVISIONS

RELEASED FOR PRODUCTION	
MFG. ENG.	DATE 4/21/76
IN AREA A164, R95 WAS 1780 OHMS	
27431-05	12-11-78 BDI
IN AREA A1A2, STRAPS 19,37 & W8 NOT SHOWN. REVISED DWG TO SHOW COPPER CHG. OF 25-1003. 549 FROM A10, U43 TO.	
27431-05	12-20-78 BDI

COMPONENT	REF DESIGNATION
CAPACITOR	C1 THRU C56
RESISTOR	R1 THRU R105
JUMPERS	1 THRU 16

NAME	TITLE	DATE
V. PEZRET	DRAFT	3-3-76
E. CERO	CHECK	3-10-76
IRWIN BERGER	ENG'G	3-11-76
H. ROSS	Q.C.	3-11-76
FRAUENBERGER	DIR. ENG.	3-11-76

TITLE: PART. ORT. ASSY MOD 9/16 HSALD 9 7/32 CPU - C BOARD

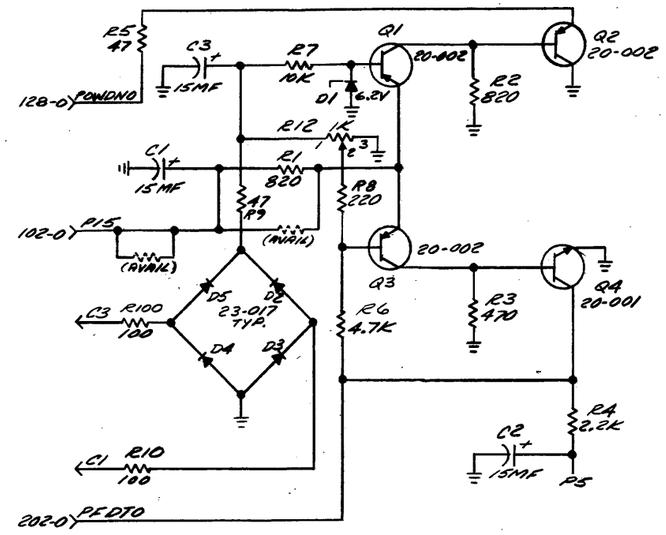
13047

SHEET 1 OF 1

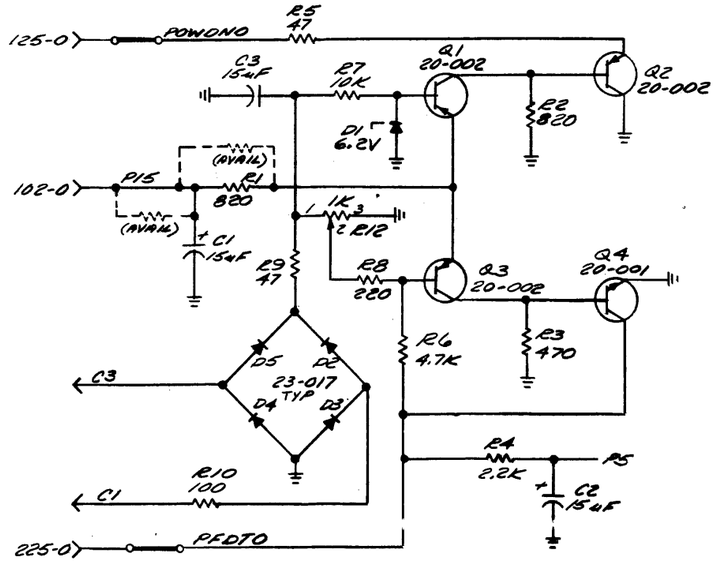
35-324 MAN PRESS

INTERDATA

REVISIONS



*F00



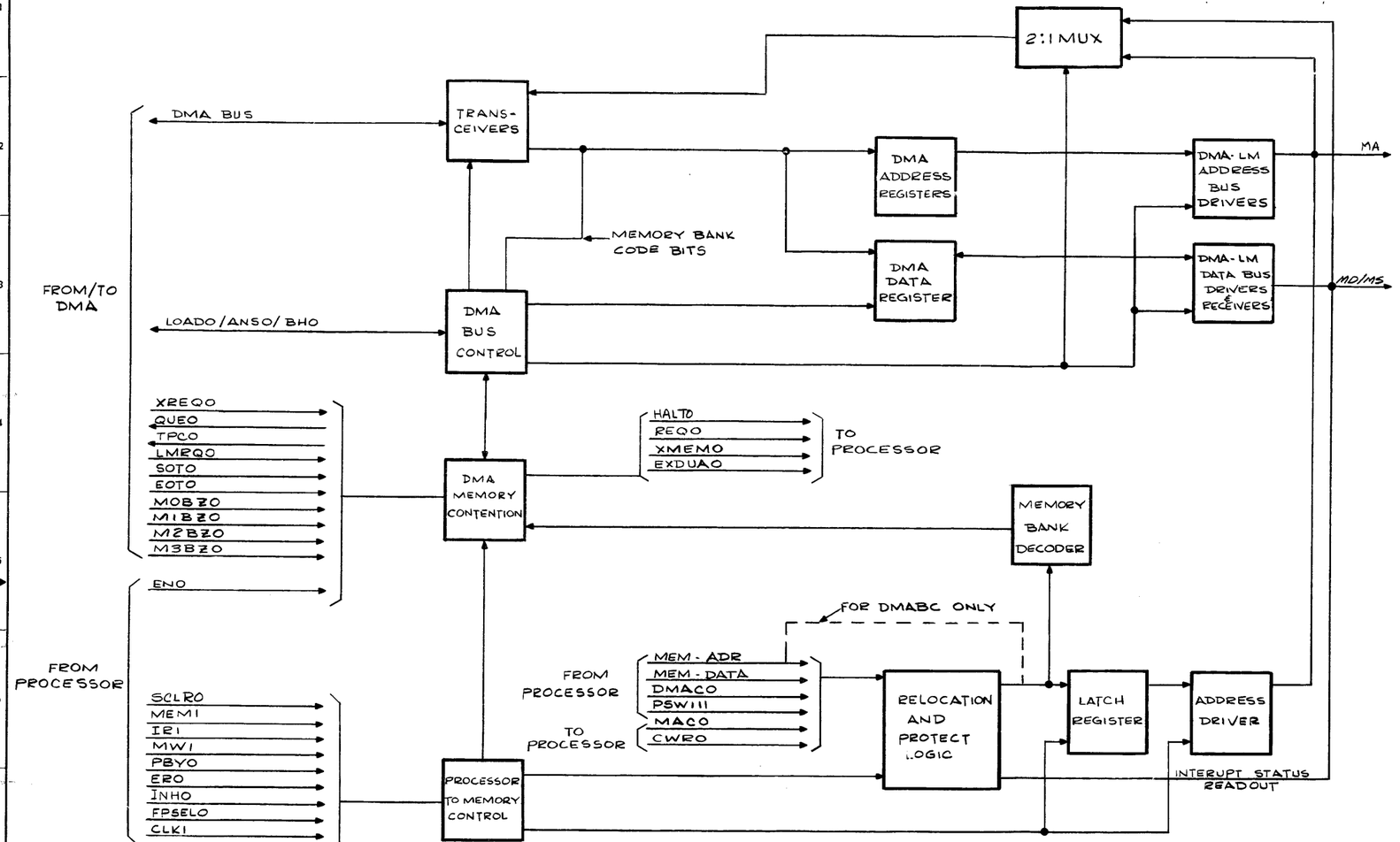
F01

SCALE—N	NAME	TITLE	DATE
TOLERANCE: .XXX ± .005, .XX ± .02, .X ± .05, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	P.EDWARDS	DRAFT	1-19-76
	R. CERO	CHK	4-6-76
	D.F. RINKENBERGER	ENGR	4-6-76
	P. BARKER	Q.C.	4-6-76
	S. MESSINA	MGR.	4-6-76

TITLE: PRIMARY POWER FAIL

DWG. NO. 03745 SHEET OF 1—1

DWG. NO. 35-448 C08



CONN 2

	2	1
00	GND	MEMI
01		IRI
02		MWI
03		CWRO
04		MACO
05		DMACO
06		HALTO
07		RDSETO
08		XMEMO
09		PBYO

NOTES:

1. THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL.

35-527 M01 R06	MEMORY ACCESS CONTROL
35-528 M01 R05	DIRECT MEMORY ACCESS CONTROL

BACK PANEL MAP

TERM NO.	ROW 1	ROW 2
41	P5	GND
40	GND	GND
	P15	P15
	N15	N15
	MD150	MD160
	MD130	MD140
35	MD110	MD120
	MD090	MD100
	MD070	MD080
	MD050	MD060
	MD030	MD040
30	MD010	MD020
		MD000
	WRTO	
		DGNDE
25	DMA150	DMA160
	DMA130	DMA140
	DGNDD	DMA120
	DMA110	DMA100
	DMA090	DMA080
20	DMA070	DMA060
	DMA050	DGNDC
	DMA030	DMA040
	DMA010	DMA020
	DGNDB	DMA000
15		DMX140
	DMX150	DMX120
	DMX130	DGNDA
	M3BZO	M2BZO
	M1BZO	MOBZO
10	LOADO	ANSO
	LMRQO	DGNDF
	SOTO	EOTO
	XREQO	QUEO
05	RPCO	TPCO
		BHO
	FPSELO	CLKI
	PERRO	
01	GND	GND
00	P5	GND

7200

41	P5	GND
40	GND	GND
	P15	REQO
	N15	ENO
	MAR070	EXDUAO
	MAR060	
35	MAR050	PSW111
	MAR040	
	MA130	MA140
	MA110	MA120
	MA090	MA100
30	MA070	MA080
	MA050	MA060
		MXR141
	MAR030	MXR120
	SCLRO	
25		
	MAR020	MXR130
	MAR010	MXR140
	MAR000	MXR150
20		
15		
10	MA030	MA040
	MA020	MA021
	XMA140	XMA150
	MA010	MA011
	MA000	MA001
05	MPARO	XMA141
	INHO	ERO
	P15	N15
01	GND	GND
00	P5	GND

0720U

REVISIONS

RELEASED FOR PRODUCTION
ENG. PB DATE 3/14/75

REVISED SHTS 3,6&7, PC BDS WERE R00
BG VKM 2484 — 5-12-75 R01

REVISED SHT 3,5,7
PB VKM 2505 — 5-22-75 R02

REVISED SHT 7.
PB VKM 2551 — 7-8-75 R03

REVISED SHTS 6&7.
PB VKM 2580 — 7-28-75 R04

REV.	2			2		1	2	4
SHEET NO.	0	1	2	3	4	5	6	7

NOTES

NAME	TITLE	DATE
G. MELTON	DRAFT	3-12-75
R F CERO	CHK	3-12-75
R. BALAS	ENGR	3/14/75
J JAMES	SYS TEST	3/14/75
D FRANKENBERGER	MFG QA	3/14/75

TITLE: FUNCTIONAL SCHEMATIC MEMORY ACCESS CONT.

TASK NO. 03142
DWG NO. 02-3489M01R04DOC
SHEET OF 0-8

BRUNING 44-231 1HOA2

INTERDATA®

REVISIONS

NAME	TITLE / DATE
	DRAFT
	CHK
	ENGR
	DIR ENG

TITLE: FUNCTIONAL SCHEMATIC MEMORY ACCESS CONT.

TASK NO. 03142 | DWG NO. 02-348M01 D08 | SHEET OF 1-8

NOTES
1. ALL PARTS MARKED WITH AN ASTERISK (*) ARE REMOVED FOR DMABC(3S528M01)
2. THE FOLLOWING PINS ARE STRAPPED FOR THE DMABC(3S528M01) WITH

NOTE 2 (CONT.)
WIRE WRAP STAKES ASSOCIATED WITH THE FOLLOWING PIN NUMBERS.
A137-12 TO A105-2; A137-10 TO A105-3;
A137-04 TO A105-06; A137-02 TO A105-07;
A138-02 TO A106-02; A138-10 TO A106-03;

NOTE 2 (CONT.)
A138-12 TO A106-06; A138-06 TO A106-07;
A140-02 TO A107-02; A140-08 TO A107-03;
A140-12 TO A107-06; A140-10 TO A107-07;

BRUNING 44-231 16:42

INTERDATA®

REVISIONS

4C3 4C6 5F3

A35 A34 A35 A23 A24 A23 A16 A15 A15 A16 A05 A04 A04 A05 A30 A33 A32 A31 A33 A34 A35 A36 A37 A38 A39 A40 A41 A42 A43 A44 A45 A46 A47 A48 A49 A50 A51 A52 A53 A54 A55 A56 A57 A58 A59 A60 A61 A62 A63 A64 A65 A66 A67 A68 A69 A70 A71 A72 A73 A74 A75 A76 A77 A78 A79 A80 A81 A82 A83 A84 A85 A86 A87 A88 A89 A90 A91 A92 A93 A94 A95 A96 A97 A98 A99 A100 A101 A102 A103 A104 A105 A106 A107 A108 A109 A110 A111 A112 A113 A114 A115 A116 A117 A118 A119 A120 A121 A122 A123 A124 A125 A126 A127 A128 A129 A130 A131 A132 A133 A134 A135 A136 A137 A138 A139

DMAPDA1 7E8 DMAA001 DMAA011 DMAA021 DMAA031 LDDA01 6J7 DMAAC41 DMAA051 DMAA061 DMAA071 LDDB1 6J7 CUNDS20 6J5 DMAB081 5G2 CUNDB20 6J5 DMAA091 5G2 DMAA101 DMAA111 LDDC1 6J8 IR271 3E1 DMAA121 5F3 IR281 3E2 DMAA131 5F3 IR291 3E3 DMAA141 5F5 IR301 3E4 DMAA151 5F5 IR311 3E5 RSTAI 3H9 DMAPDB1 7E8 GMSB1 7K6 DMAA161 5F5 LDDD1 6D8

GMSA1 7K6

MD000 MD010 MD020 MD030 MD040 MD050 MD060 MD070 MD080 MD090 MD100 MD110 MD120 MD130 MD140 MD150

229-1 130-1 230-1 131-1 231-1 132-1 232-1 133-1 233-1 134-1 234-1 135-1 235-1 136-1 236-1 137-1

1K4 1K6 1K8 5A5

3M7 WREO WR00

5N3 MA100 1A2 MXR120 A 1A4 MAR000 3B5 INMACO 1A6 MAR040 B 1A7 235-1 A112 19-101 B PSW111 PSW110 5N3 MA110 1A5 MXR130 C 1A3 1A6 MAR050 D 5N3 MA120 1A3 MXR140 E 1A5 MAR020 1A7 MAR060 F NOTE 2 5N4 MA130 1A3 MXR150 G 1A5 MAR030 1A7 MAR070 H

INPUTS SEL B STB 1 SEL A SEL/MUX A139 19-116 4 TO 1 A129 19-116 4 TO 1 SEL/MUX

A66 19-075 A75 19-075 A76 19-075 A83 19-075 A81 19-075 A65 19-075 16x4 REG. STK. DATA IN

R46 R47 R48 R58 R51 R50 R49 R59 R35 R34 R33 R32 R23 R24 R26 R25 R4 R5 R13 R11 R45 R44 R56 R55 560Ω

R001 R011 R021 R031 R041 R051 R061 R071 L001 L011 L021 L031 L041 L051 L061 L071 SC241 SC251 SC261 SC271 XR121 XR131 XR141 XR151

1D4 1D6 1D7 1B7 3A5 3A4 3A3 3A2 1D3

A112 19-101 A30 19-089 A33 19-036 HPO GPARE1 7R5 XAP 6N8 XMDIG SA6 237-1

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED

NOTES
1. ALL PARTS MARKED WITH AN ASTERISK (*) ARE REMOVED FOR DMABC(35-528M01)
2. MAC(35-527M01) NORMALLY STRAPPED FOR X'03'.

NAME	TITLE	DATE
J.F.FLEMING	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE: FUNCTIONAL SCHEMATIC MEMORY ACCESS CONT.

TASK NO. 03142 SHEET OF 2-8

DWG NO. 02-348M01 DD6

BRUNING 44-231 16042

INTERDATA®

REVISIONS				
A144-10 WAS CONN TO A77-09 ONLY; A144-13 WAS CONN TO A144-12 ONLY; A150 A WAS GMEM1, A84-04; 10 WERE EOMO,				
BG	WEH	2489	—	5-12-75 R01
AREA E8: ADDED A78. A88-01 WAS TO A143-11, A88-12 WAS TO A144-06.				
PE	WEH	2505	—	5-22-75 R02

NOTES
1. MAC(35-527M01) NORMALLY STRAPPED FOR X'08'.
2. ALL PARTS MARKED WITH AN ASTERISK (*) ARE REMOVED FOR DMABC (35-528 M01)
3. THE FOLLOWING CHANGES MUST BE MADE FOR DMABC(35-528 M01)
   A - BREAK THIS CONNECTION,
   B - GROUND THIS RUN
   C - RESISTOR INSTALLED ON DMABC ONLY
4. STRAP G1 TO G2 FOR MAC OR DMABC WITH PARITY OPTION.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MEMORY ACCESS CONT.
TASK NO. 03142
DWG NO. 02-348 M01 R02 D08
SHEET OF 3-8

BRUNING 44-231 16042

INTERDATA®

REVISIONS

6R1 ENA0

A55 19-118 QUAD BUS XCEIVER

EMX121 EMX131 EMX141 EMX151 DGNDA — IN3 — 213-1

DMX120 214-1 · DMX130 113-1 · DMX140 215-1 · DMX150 114-1

DMX141 DMX151 — 6D5

A54 19-071 D-EDGE TRIG. FF — 2B1 — DMA001 DMA011

A56 19-118 QUAD BUS XCEIVER

EMA001 EMA011 EMA021 EMA031 DGNDB — IN4 — 116-1

DMA000 216-1 · DMA010 117-1 · DMA020 217-1 · DMA030 118-1

DMA021 DMA031

A53 19-071 D-EDGE TRIG. FF — 2E1 — DMA041 DMA051

A57 19-118 QUAD BUS XCEIVER

EMA041 EMA051 EMA061 EMA071 DGNDC — IN6 — 219-1

DMA040 218-1 · DMA050 119-1 · DMA060 220-1 · DMA070 120-1

DMA061 DMA071

A52 19-071 D-EDGE TRIG. FF — 5G2 — DMA081 DMA091

P5 1K R18 — DLDA1 6F5

A151 19-035 4-BIT CNTR

RG3 1K P5 — CNT UP · CNT DWN · LD · CL

CAR N.C. · BOR N.C.

A146 19-035 4-BIT CNTR

R37 1K P5 — EDM1 — 3K2

A97 19-035 4-BIT CNTR

7N7 EPSELA0

A152 19-036 HPD · A153 19-036 HPD · A154 19-015 HB

XAD141 XAD151 — 1K3 — R73 R74 R72 R75 470 P5 — XMA141 205-0 · XMA140 108-0 · XMA150 208-0

AD001 AD011 — 1K4 — MA001 206-0 · MA000 106-0 · MA011 207-0 · MA010 107-0

A147 19-036 HPD · A148 19-036 HPD

AD021 AD031 — R65 R64 470 P5 — MA021 209-0 · MA020 109-0 · MA030 110-0

AD041 AD051 — 1K6 — R66 R67 470 P5 — MA041 210-0 · MA050 129-0

A98 19-036 HPD · A99 19-036 HPD

AD061 AD071 — R38 R39 470 P5 — MA060 229-0 · MA070 130-0

7N6 EPSELI — MA080 230-0 · MA090 131-0

R40 1K P5 — 1K8, 3H8

R41 1K P5 — 1K8, 3F8

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NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE: FUNCTIONAL SCHEMATIC MEMORY ACCESS CONT.

TASK NO. 03142 · DWG NO. 02-348M01 D08 · SHEET OF 4-8

BRUNING 44-231 16042

INTERDATA®

REVISIONS

AT 10C 64 ADDED 3F9 TO XRPA				
-	ARA	2505	6-19-75	R01

A47 19-118 QUAD BUS XCEIVER

A48 19-118 QUAD BUS XCEIVER

A46 19-118 QUAD BUS XCEIVER

A63 19-066 2 TO 1 MUX

A73 19-066 2 TO 1 MUX

A45 19-071 D-EDGE TRIG FF CLR

A44 19-071 D-EDGE TRIG FF

A90 19-035 4 BIT UP/DWN ONTR

A89 19-035 4-BIT UP/DWN CNTR

A100 19-036 HPO

A99 19-036 HPO

C17 THRU C70 .001 MFD

C7 THRU C16 15 MFD

DECOUPLING CAPACITORS

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MEMORY ACCESS CONT.

TASK NO. 03142 ENGR NO. 02-348M01R01D08 SHEET OF 5-8

BRUNING 44-231 16042

INTERDATA

REVISIONS

A134-10 WAS CONNECTED TO A12-07 ONLY.
BG WN 2484 — 5-12-75 R01
NRGA BG, WAS SHOWN THUS:
P5 R92 3.27Ω — LMRQ1 7A3 — LMRQ1 10A0 — A109 — A109 — 04 LMRQAO 7A2 — A125
04 WN 2580 — 7-25-75 R02

NOTES

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED SUBJECT TO AGREEMENT WITHIN A FEW THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE: FUNCTIONAL SCHEMATIC MEMORY ACCESS CONT.

TASK NO 031#2 — SHEET OF 6-8

DWG NO 02-348M01R02D08

BRUNING 44-231 16042

INTERDATA®

REVISIONS				
A93 WAS 19-015				
B	JGH	2984	–	5-12-75 R01
AT LOC NG ADDED 3H8 TO FPSEL1				
–	JGH	2505	–	6-19-75 R02
AREA F2, STRAP "A" WAS NOT SPEC'D.				
A	RM	2551	–	7-8-75 R03
AREA C3, A50-12 WAS CONN. TO ANEM LMRQ1,				
A	RM	2580	–	7-23-75 R04

HB FREQO
N3 CST01
N4 CST31
L8 FEOT1
6L2 CPUW1
6D6 LMRQAO
3K2 EOM1
M9 BUBZO
K3 CAO
K3 CBI
6J9 BRU1

A115 19-058 SG
A43 19-055 SG
A50 19-062 SG
STRAP "A"

R68 2.2K
R69 1K
L2 4.7uH
C5 9.35PF
6R2 GOOS1
L7 FPSELO
A149 19-055 SG
A93 19-057 SG
A121 19-055 SG
LOSC1 6J6

126-0 SCLRO
A145 19-015 HG
SCLROA 3D8, 3H3, 3K2, 3L6
A116 19-101 HP
SCLROB D4, J2
SCLROC 6A7, 6J2, F8, K6, 6L7

R8 10K
R7 6.8K
C2 100PF
LB FEOT1
A31 19-042 05
N.C.
R6 1K
L8 FEOTO
A51 19-059 SA

R2 2.2K
L1 4.7uH
R1 1K
C1 9.35PF
A10 19-055 SG
A41 19-057 SG

6B1 PAO
105-1 RPCO
A87 19-057 SG
R31 270Ω
107-1 XREQO
6K1
R27 1K
N4 SOTO

M1 XRP
PA1 6L1
PB1 6G5, 6L2, C9
PCO, C9, 6L1
PC1 6B2
6J2 POSC1
E6 SCLROB
A69 19-064 SF
A68 19-064 SF
ENOSCO 6R6
A60 19-055 SG
SLADAO 1K7
SLADBO 1C9, 5A3, 5A6
LADO 5A8
LDATO 5A7, C9
A40 19-058 SG
3M1 MWR1
3M1 MRDI
6R8 FANSO
6J4 ANMAO
INOSC1 6L2
A42 19-060 SG
A43 19-055 SG
GMSA1 2G2
GMSO 6D1
GMSB1 2R1
N7 FPSELBO
3K2 EOM1
A102 19-017 HG
A101 19-015 HG
PST41 6J3

3M1 MRDI
H3 PB1
H3 PCO
A51 19-059 SA
A39 19-125 SBO
208-1 EOTO
A41 19-057 SG
P1A 270Ω
K6 LDATO 01
6A7 BH1
A91 19-057 SG

E6 SCLROC
6R2 BARBO1
08 FREQO A1
6L3 EXDUA1
A96 19-063 SDF
NC
6J1
PMDI 6J1
FEOT1 A2, B7
FEOTO D7

6N2 GOOS1
A93 19-057 SG
6J7 BBZO
A42 19-060 SG
A91 19-057 SG
BUBZO A2

P5 R1 1K
XRP E3
CA1
CC1
E6 SCLROB
A3 CAO
A3, 6D6 CBI
CC1 6J2
A59 19-059 SA
CST01 A2
A60 19-055 SG
TPCO 205-1
SOTO 108-1
J7
6J1 CBO
A58 19-124 SB
R16 470Ω P5
CST31 A2
R15 1K
A49 19-063 SDF
NC
QUEO 207-1
R17 470Ω P5
E6 SCLROC
GPAR1 2R6

103-1 FPSELO
A93 19-057 SG
FPSEL1 3A9, 4J9, 3H8
FPSELA1 3L4, 6L3
FPSELAO 4G9
FPSELBO 5K4, F6
6A9, A5, 6F5, 6K5
5H5 DA1S1
A29 19-016 HG
DMR DA1 2A1
DMR DB1 2R1

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE: FUNCTIONAL SCHEMATIC MEMORY ACCESS CONT.

TASK NO 03142
SYS NO 02-348M01R04D08
SHEET 7 OF 8

BRUNING 44-231 15642

NOTES:

1. STIFFENER BAR (ITEM 3) SHALL BE SOLDERED TO GND BUS AT 2 END POINTS AND CENTER POINT.
2. CONNECTOR PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.

15.380 REF

14.880 REF

SEE NOTE 1

62 SEE NOTE 2

63 31 PLACES

66

3 SEE NOTE 1

5 2 PLACES

4 2 PLACES

6 MOUNT ON SOLDER SIDE 2 PLACES

64

PARTIAL VIEW A-A

.530 MAX

.062 REF.

.125 MAX.

REVISIONS				
RELEASED FOR PRODUCTION				
MFG. ENG. [illegible] DATE 2-4-74				
REVISED LAPPER TO REFLECT 02-933 A02, A93 WAS ITEM 11				
BG	WH	248+	5-13-75	R01
REVISED TO REFLECT A02 COPPER				
FC	WH	2505	5-22-75	R02
ADDED CONN BETWEEN A14 AND 8 AND GND				
GH	WEA	2525	6-23-75	R03
REVISED TO REFLECT A02 COPPER.				
FC	WEA	2540	6-6-75	R04
REVISED TO REFLECT A06 COPPER.				
[illegible]	[illegible]	2551	7-8-75	R05
REVISED TO AGREE WITH COPPER. STMAP 41 WAS NOT SPECIFIED				
BF	WH	2580	7-29-75	R06

COMPONENT	REF DESIGNATION
CAPACITOR	C1 THRU C70
RESISTOR	R1 THRU R75 & R78
T.P.	A1 THRU A140

NAME	TITLE	DATE
J. PEREZ	DRAFT	2-24-75
E. CEPO	ENR.	3-12-75
R. BRAAS	ENG.	3-14-75
R.A. BARKER	Q.C.	3-14-75
A. FRANKENBERGER	MGR.	3-14-75

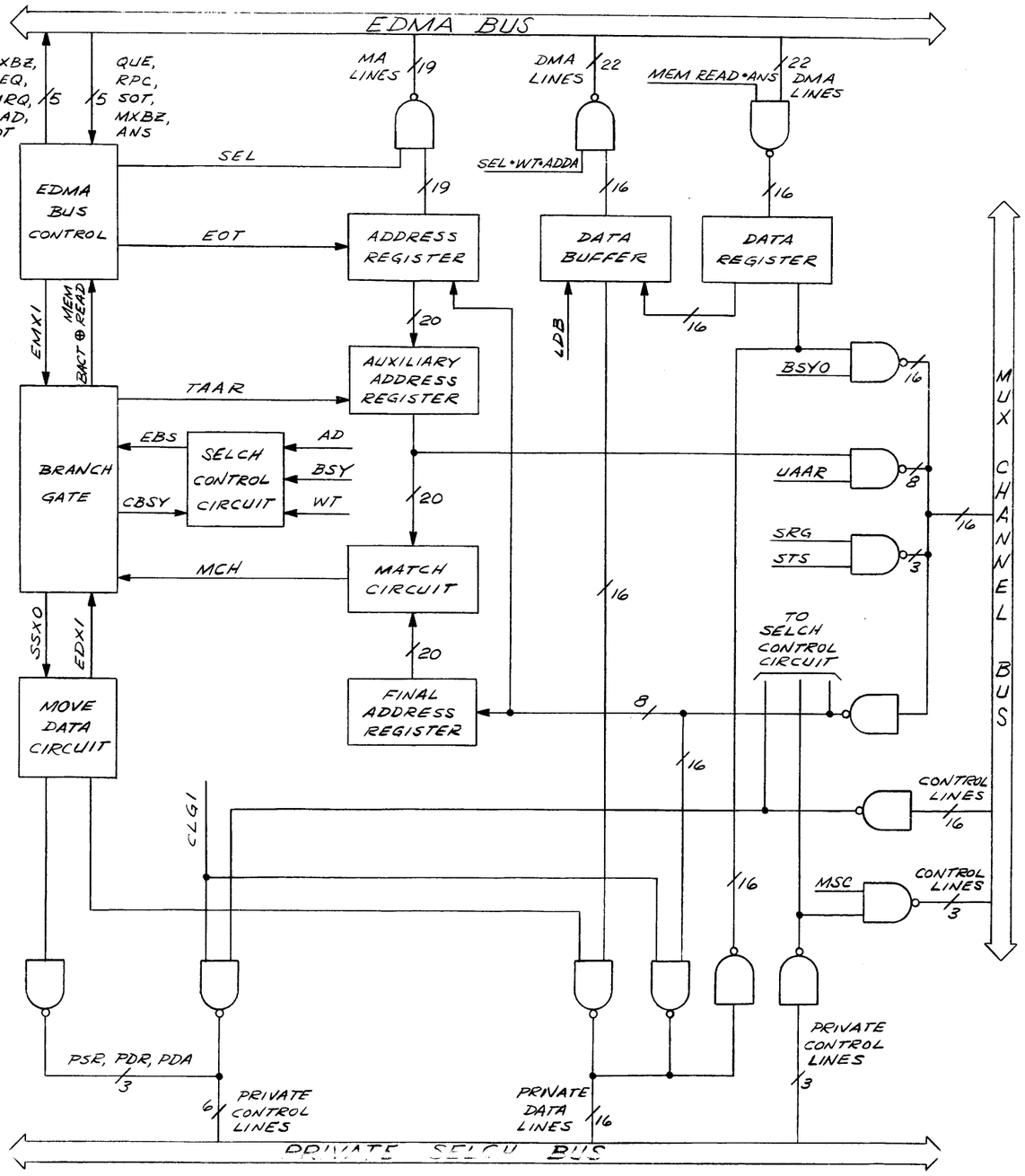
TITLE: ASSY. CKT. ASSY MEMORY ACCESS CONTROL BOARD

03142

35-527 MOD 6/03

1 OF 1

C-01



BACK PANEL MAP

ESELCH			CONN NO
ROW 1	TERM.NO.	ROW 2	
P5	41	GND	1
GND	40	GND	
	39		
	38		
DMA170	37	DGND	
DMA150	36	DMA160	
DMA130	35	DMA140	
DGND	34	DMA120	
DMA110	33	DMA100	
DMA090	32	DMA080	
DMA070	31	DMA060	
DMA050	30	DGND	
DMA030	29	DMA040	
DMA010	28	DMA020	
DGND	27	DMA000	
SCLR0	26	PHW0	
	25		
	24		
PSYN0	23	PATN0	
	22	PTACK0	
PCL070	21	PDA0	
PDR0	20	PCMD0	
PSE0	19	PADRS0	
PDI40	18	PDI50	
PDI20	17	PDI30	
PDI00	16	PDI10	
PDO80	15	PDO90	
PDO60	14	PDO70	
PDO40	13	PDO50	
PDO20	12	PDO30	
PDO00	11	PDO10	
	10	DMXI40	
DMX150	09	DMXI20	
DMX130	08	DGND	
M3B20	07	M2B20	
M1B20	06	M0B20	
LOAD0	05	ANS0	
LMRQ0	04	DGND	
SOT0	03	EOT0	
XREQ0	02	QUE0	
GND	01	GND	
P5	00	GND	
1	TERM.NO.	2	CONN
P5	41	GND	0
GND	40	GND	
	39		
	38		
RPC0	37	TPC0	
DGND	36	BH0	
	35		
	34		
	33		
	32		
	31		
	30		
	29		
	28		
	27		
SCLR0	26	HW0	
	25		
	24		
SYN0	23	ATN0	
RACK0	22	TACK0	
CL070	21	DA0	
DR0	20	CMD0	
SE0	19	ADRS0	
DI40	18	DI50	
DI20	17	DI30	
DI00	16	DI10	
DO80	15	DO90	
DO60	14	DO70	
DO40	13	DO50	
DO20	12	DO30	
DO00	11	DO10	
	10		
	09		
	08		
	07		
	06		
	05		
	04		
	03		
	02		
GND	01	GND	
P5	00	GND	
1	TERM.NO.	2	CONN

TEST POINTS

DESIG.	MNEMONIC	SHT. LOC.
A	ADIA	3N9
B	DXIA	4F8
C	MSCOA	4J5
D	BSYIB	4J3
E	SELIA	3K2
F	WTIA	4J6
G	SXIA	4F7

PRINTED CIRCUIT BOARD AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL:

ESELCH	35-508	M01 B03

NOTE: THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

SHEET INDEX	REV.	03	02	-	01	-	-	-	02	03
	SHT.	1	2	3	4	5	6	7	8	9

REVISIONS

RELEASED FOR PRODUCTION
ENG. I.Y. DATE 4/17/75

REVISED SHTS 2, 4, 8, & 9 ESELCH, 35508 M01, WAS R00

PE	JRC	2577	KY	7-28-75 R01

REVISED SHTS 2 & 9, E SELCH, 35-508 M01 WAS R01

WS	JRC	2659	-	11-12-75 R02

REVISED SHTS 8 & 9, E SELCH, 35-508 M01 WAS R02

WS	WJA	2792	-	3-25-76 C03

NOTES

NAME	TITLE	DATE
J.F. FLEMING	DRAFT	4-17-75
R. CERO	CHK	4-17-75
J. YANG	ENGR	4-17-75
R.A. BARKER	Q.C.	4-17-75
D. FRANKENBERGER	DES MGR	4-17-75

TITLE SCHEMATIC EXTENDED SELECTOR CHANNEL

TASK NO. 03055

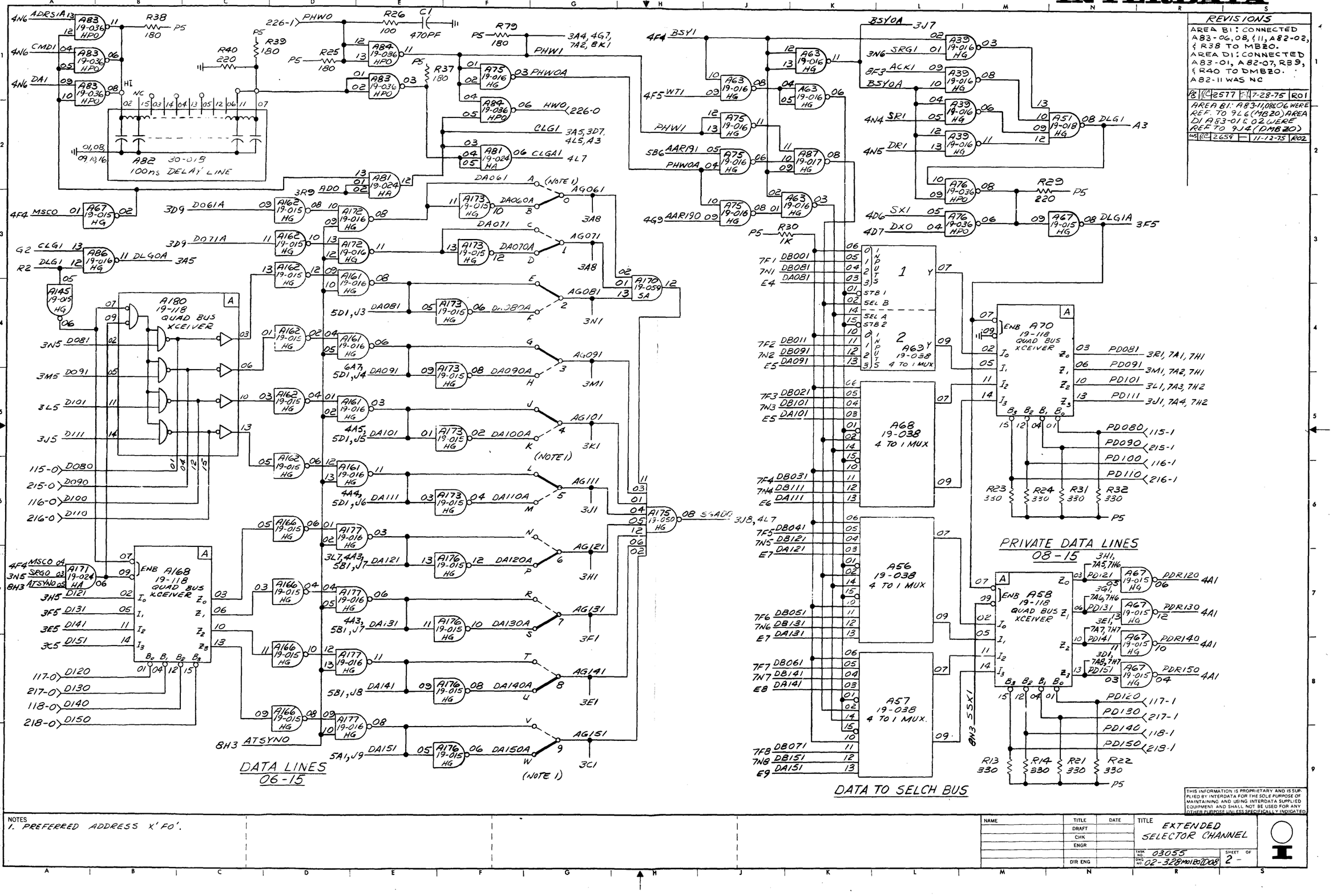
WO 02-328 M01 REC 3008

SHEET OF 1-9

BRUNING 44-231 1C042

INTERDATA

REVISIONS				
AREA B1: CONNECTED A83-06,08, & 11, A82-02, & R38 TO MB20. AREA D1: CONNECTED A83-01, A82-07, RB9, & R40 TO DMB20. A82-11 WAS NC	PB	WC 2577	PN 7-28-75	R01
AREA B1: A83-11,08&06 WERE REF. TO 9L6 (MB20) AREA D1 A83-01 & 02 WERE REF. TO 9J4 (DMB20)	WA	WC 2659	— 11-12-75	R02



NOTES
1. PREFERRED ADDRESS X'F0'.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE: EXTENDED SELECTOR CHANNEL

TASK NO. 03055 | DWG NO. 02-328M01B0D08 | SHEET OF 2 -

BRUNING 44-231 18042

INTERDATA®

REVISIONS

DATA TO DMA BUS

DATA LINES 00-07

PRIVATE DATA LINES 00-07

A131 19-118 QUAD BUS XCEIVER (SEE SH 1)

A130 19-118 QUAD BUS XCEIVER (SEE SH.1)

A106 19-118 QUAD BUS XCEIVER (SEE SH. 1)

A107 19-118 QUAD BUS XCEIVER (SEE SH. 1)

A79 19-069 8 TO 1 MUX

A91 19-069 8 TO 1 MUX

A103 19-069 8 TO 1 MUX

A115 19-069 8 TO 1 MUX

A127 19-069 8 TO 1 MUX

A139 19-069 8 TO 1 MUX

A151 19-069 8 TO 1 MUX

A163 19-069 8 TO 1 MUX

A94 19-069 8 TO 1 MUX

A119 19-065 2 TO 1 MUX

A118 19-065 2 TO 1 MUX

A121 19-089 ADFF

A137 19-050 HG

A169 19-055 SG

A179 19-036 HPO

A145 19-015 HG

A133 19-016 HG

A109 19-017 HG

A103 19-017 HG

A78 19-017 HG

A87 19-017 HG

A136 19-015 HG

A148 19-024 HA

A25 19-016 HG

A65 19-017 HG

A02 19-056 SG0

A14 19-015 HG

A178 19-056 SG0

A38 19-015 HG

R35 1K P5

R84 3.3K P5

C2 470PF

R82 1K P5

R6 1K P5

R83 1K P5

R61 330 P5

R60 330 P5

R53 330 P5

R54 330 P5

R63 330 P5

R62 330

R56 330 P5

R55 330 P5

R9 1K P5

NOTES

BRUNING 44-231 16042

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE: EXTENDED SELECTOR CHANNEL

TASK NO 03055 DWG NO 02-328M01 D08 SHEET 3 OF

INTERDATA®

REVISIONS
AREA E1: A111-09 WAS CBSYO. A111-08 WAS TO A134-01. AREA G1: ADDED A170. AREA K1: A87-03 WAS CBSYO.
02577 7-28-75 R01

PDRI20
PDRI30
PDRI40
PDRI50
SXI
PSYNI
DXO
SCLRI
XRPA
DA13I
CMG1
DA12I
MSCI
DA11I
BSYO
SGADI
SCLR0A
DA10I
SDXO
PSYNO
DARGO
SSXO
PDARI
PSYNI
DXI
PSYNO
SELSTSI
SELST5O
CLUSO
TERMO
BSYO
BSY1
CMDG01
CMDG00
MSCO
MSCI
MSCOA
WT1
WTOA
WT1A
PDAR1
PDRO
PDAO
SXI
PSRO
DXO
DX1
DX1A
ENG1
ENG1A
LDRHI
PHWI
LDRL0
LDRH1
EDXI
SATNO
EBSI
SYNO
PSRO
PCLO7O
PDRO
PCMDO
PADRSO
DRI
DAI
CLO7I
SRI
CLG1
CLGA1
SGADO
ADRSIA
CMDI
TERMO
SBACT1
REQ1
EOT1
SCLR0A
BACT1
BACTO
RBA0A
SELO
DBSY1
BSY1B
MSCOA
WT1A
PDAO
DX1A
ENG1A
LDRL0
LDRH1
EDXI
SATNO
EBSI
PSYNI
SYNO
PSRO
PCLO7O
PDRO
PCMDO
PADRSO
DRI
DAI
CLO7I
SRI
CLG1
CLGA1
SGADO
ADRSIA
CMDI
AAR19I
AAR190
MCH0
BACT1
R18 180
R19 22K
R20 330
R27 1K
R41 22K
R42 10K
R43 1K
R66 1K
R76 1K
R77 330
R78 1K
RB1 220
R11 330
R12 330
R15 330
R16 330
R17 330
R28 10K
A50 19-016 HG
A49 19-015 HG
A66 19-050 HG
A65 19-017 HG
A111 19-015 HG
A134 19-016 HG
A170 19-053 SA
A169 19-055 SG
A112 19-024 HA
A122 19-089 HDFF
A157 19-036 HPO
A87 19-017 HG
A85 19-042 R03 ONE SHOT
A85 19-042 R08 ONE SHOT
A27 19-089 HDFF
A37 19-016 HG
A76 19-036 HPO
A61 19-017 HG
A73 19-015 HG
A74 19-016 HG
A100 19-036 HPO
A62 19-042 R05 ONE SHOT
A179 19-036 HPO
A156 19-015 HG
A60 19-036 HPO
A72 19-036 HPO
A81 19-024 HA
A125 19-017 HG
A136 19-015 HG
A160 19-016 HG
A112 19-024 HA
A62 19-042 R05 ONE SHOT
3B1, 7G5
3A1
2H1, 3A4, 8K2, 8G6
2A7, 2A3, 3B1, 6B5, 6E8, 9J7
M4, A4
3A1, 8C2
G8, 2H1, 6H9, 7A2, 7H9, 8E5, 8J4, 9F8, G1
3A4, 9K4, 9F7, 7H3, 7H8
6H8, 8G5, 8H8, 8E4
A1, 2L3
A1, 2L3
E1, K2
A4
TP(D)
TP(C)
TP(F)
TP(G)
TP(B)
A6
R5
R6
8K2, 8A3
8C3
7H8
G7
8J2
6A2
8K4
8B4
3R7
123-0
F6
119-1
J5
120-1
J6
221-1
220-1
219-1
2L2, 3J6
2A1, 3J6
2A1, 3J8
3J8
3J7
2A1, 3J6
2L3
2H2
5H9
H2
G9, 8H8, 9K6
NC
6A1
3R6, 7G5, 9K4
8K3, 2H2
7A9
G8, 2H1, 6H9, 7A2, 7H9, 8E5, 8J4, 9F8, G1
3A4, 9K4, 9F7, 7H3, 7H8
6H8, 8G5, 8H8, 8E4
9K5, 3G1
6C1, 8N2,
9N4
9J8
3M9
8R6
8R3
9N2
5B7
2E7
3N5
2E6
3R8
3M9
2E5
6C3
8R4
J5
R4
F1
K4
2R7
2R7
2R8
2R8
D6
R9
D7
3K9
F3
F5
F3
2G1
2G2
2J6
119-0
121-0
120-0
2G2
221-0
220-0
219-0
L8
5B7
8K3, 2H2
5H9
H2

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

NOTES

NAME	TITLE	DATE
CHRIS JENSEN	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE: EXTENDED SELECTOR CHANNEL

TASK NO 03055 SHEET OF 4

DWG NO 02-328M01R01D08

BRUNING 44-231 16042

INTERDATA®

REVISIONS

DAG0 3U6 · DA15 2E9 · DA14 2E8 · DA13 2E7 · DA12 2E7 · TAAR0 8N2 · SETAAR0 3R6

MA15 · MA14 · MA13 · MA12 — 6G7

DA11 2E6 · DA10 2E5 · DA09 2E5 · DA08 2E4

MA11 · MA10 · MA09 · MA08 — 6G5

FL07 B5 · FL06 B5 · FL05 C5 · FL04 C5

MA07 · MA06 · MA05 · MA04 — 6G4

FL03 D5 · FL02 E5 · FL01 E5 · FL00 F5

MA03 · MA02 · MA01 · MA00 — 6G2

PG01 6D1 · C00 4F1

MAX15 · MAX14 · MAX13 · MAX12 — 6G1

P5 · R5 1K

N.C.

A07 19-035 4-BIT UP/DWN CNTR AAL

A19 19-035 4-BIT UP/DWN CNTR AAL

A31 19-035 4-BIT UP/DWN CNTR AAH

A43 19-035 4-BIT UP/DWN CNTR AAH

A55 19-035 AAX 4-BIT UP/DWN CNTR — CNTL DWN · CLR · LOAD · BCD REG INPUTS · A B C D INPUTS · A B C D OUTPUTS

AUXILIARY ADDRESS REGISTER

R4 1K · R7 1K · R3 1K · R10 1K

LFRX0 6D6 · PG00 6A1

A04 19-071 HDFF FL · A16 19-071 HDFF FL · A03 19-071 HDFF FH · A28 19-071 HDFF FH

A52 19-071 QUAD-D EDGE TRIG FF FX — CLR D

FINAL ADDRESS REGISTER

FL07 · FL06 · FL05 · FL04 · FL03 · FL02 · FL01 · FL00

FH07 · FH06 · FH05 · FH04 · FH03 · FH02 · FH01 · FH00

A05 19-029 XOR · A15 19-029 XOR · A29 19-029 XOR · A40 19-029 XOR · A53 19-029 XOR

AAR19 · AAR18 · AAR17 · AAR16 · AAR15 · AAR14 · AAR13 · AAR12 · AAR11 · AAR10 · AAR09 · AAR08 · AAR07 · AAR06 · AAR05 · AAR04 · AAR03 · AAR02 · AAR01 · AAR00

MATCH CIRCUIT

A17 19-050 HG · A41 19-050 HG · A51 19-018 HG

A14 19-015 HG

A26 19-017 HG

AG9 8J2 · BRG

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE: EXTENDED SELECTOR CHANNEL

TASK NO. 03055 · DWG NO. 02-328M01 D08 · SHEET 5 OF

INTERDATA®

REVISIONS

5N4 PG00 — A38 19-015 HG — 06 PG01 5M1

4H4 CMDG01 — A38 19-017 HG

4K1 DBSY1 — A25 19-016 HG

R45 1K — P5

4R2 CLUSO

3J7 DRGO — A80 19-024 HA — DARGO 4A6

3J6 DAGO

A89 19-035 4 BIT D CNTR — LD, CL, CNT DN, CNT UP, CAR, BOR

A25 19-016 HG

LOAD/UNLOAD SEQUENCER

A77 19-032 1 OF 10 DECODER — INPUTS A, B, C, D; OUTPUTS 0–9

R34 1K — P5 — UAARLO 3A3

R33 1K — P5 — UAARHO 3A3

UAARXO 3A3

R36 1K — P5

A38 19-015 HG — A26 19-017 HG — 08 LFRXO 5L4

A38 19-015 HG

DAGO

9L8 EOTOA — 9H3 ENDO — A80 19-024 HA

2E5 DA091 — A27 19-089 HDFF — 08 NC

3N5 CMGI

3M9 SCLROA

R1 1K — P5

ADDRESS REGISTER

5N1, 8A6

MAX121 MAX131 MAX141 MAX151

G4 MA0041 MA0051 MA0061 MA0071

A54 19-070 4 BIT CNTR — INPUTS, OUTPUTS, CLK, ENP, ENT, LD, CAR

5K1

MA001 MA011 MA021 MA031

G5 MA0081 MA0091 MA0101 MA0111

A42 19-070 4 BIT CNTR

E1, 5H1

MA041 MA051 MA061 MA071

G7 MA0121 MA0131 MA0141 MA0151

A30 19-070 4 BIT CNTR

E3, 5F1

MA081 MA091 MA101 MA111

5K5 FH001 — 5K5 FH011 — 5J5 FH021 — 5J5 FH031

A18 19-070 4 BIT CNTR

E4, 5C1

MA121 MA131 MA141 MA151

5H5 FH041 — 5G5 FH051 — 5G5 FH061 — 5F5 FH071

4F4 MSCO

A06 19-070 4 BIT CNTR

7F1 DB001 — 7F2 DB011 — 7F3 DB021 — 7F4 DB031

A44 19-065 2:1 MUX

7F5 DB041 — 7F6 DB051 — 7F7 DB061 — 7F8 DB071

A32 19-065 2:1 MUX

7N1 DB081 — 7N2 DB091 — 7N3 DB101 — 7N4 DB111

A20 19-065 2:1 MUX

7N5 DB121 — 7N6 DB131 — 7N7 DB141 — 4F6 WTOA — 7N8 DB151

A08 19-065 2:1 MUX

9J9 ADDA0 — 4F5 WTI — 9J9 ADDA1

A137 19-024 HA

A108 19-065 2:1 MUX — ENB, SEL, 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 1Y, 2Y, 3Y, 4Y

9J2 SELOA

A96 19-118 QUAD BUS XCEIVER — ENB, Io, I1, I2, I3, Bo, B1, B2, B3, Zo Z1 Z2 Z3

01 DMX120 {209-1} — 04 DMX130 {108-1} — 12 DMX140 {210-1} — 15 DMX150 {109-1} — 08 DGND {208-1}

03 06 10 13 — DMX151 8G7 — DMX141 8G8 — DMX131 7G4 — DMX121 7G3

A48 19-118 QUAD BUS XCEIVER

01 DMA000 {227-1} — 04 DMA010 {128-1} — 12 DMA020 {228-1} — 15 DMA030 {129-1} — 08 DGND {127-1}

03 06 10 13 — DMA031 7A4 — DMA021 7A3 — DMA011 7A2 — DMA001 7A1

A36 1.9-118 QUAD BUS XCEIVER

01 DMA040 {229-1} — 04 DMA050 {130-1} — 12 DMA060 {231-1} — 15 DMA070 {131-1} — 08 DGND {230-1}

03 06 10 13 — DMA071 7A8 — DMA061 7A7 — DMA051 7A6 — DMA041 7A5

A24 19-118 QUAD BUS XCEIVER

01 DMA080 {232-1} — 04 DMA090 {132-1} — 12 DMA100 {233-1} — 15 DMA110 {133-1} — 08 DGND {134-1}

03 06 10 13 — DMA111 7H3 — DMA101 7H2 — DMA091 7H2 — DMA081 7H1

A12 19-118 QUAD BUS XCEIVER

01 DMA120 {234-1} — 04 DMA130 {135-1} — 12 DMA140 {235-1} — 15 DMA150 {136-1} — 08 DGND {237-1}

03 06 10 18 — DMA151 7H7 — DMA141 7H7 — DMA131 7H6 — DMA121 7H6

A95 19-118 QUAD BUS XCEIVER

9J8 LOADI

01 DMA160 {236-1} — 04 DMA170 {137-1} — 12 LOADO {105-1} — 15 ANSO {205-1} — 08 DGND {237-1} — DGND {204-1}

03 06 10 18 — NC NC — ANS1 8H7 — N.C.

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE: EXTENDED SELECTOR CHANNEL

TASK NO. 03055 — DWG NO. 02-328M01 D08 — SHEET OF 6

DRUMMG 44-231 16042

INTERDATA®

A71 19-038 4 TO 1 MUX
A35 19-038 4 TO 1 MUX
A47 19-038 4 TO 1 MUX
A59 19-038 4 TO 1 MUX
A23 19-065 2 TO 1 MUX
A11 19-065 2 TO 1 MUX
A46 19-071 HDFF
A37 19-071 HDFF
A22 19-071 HDFF
A10 19-071 HDFF
A126 19-069 HDFF
A114 19-024 HA
A111 19-015 HG
A101 19-016 HG
DA451 19-027 T L 0
DA331 19-027 T L 0
DA211 19-027 T L 0
DA091 19-027 T L 0

RG5 1K P5
RZ NN 1K P5

DB001 2J4, 3D5, 6H3
DB011 2J5, 3D6, 6H3
DB021 2J5, 3D6, 6H4
DB031 2J6, 3D6, 6H4
DB041 2J6, 3D8, 6H5
DB051 2J7, 3D8, 6H5
DB061 2J8, 3D8, 6H5
DB071 2J9, 3D9, 6H5
DB081 2J4, 6H6
DB091 2J5, 6H6
DB101 2J5 6H7
DB111 2J6, 6H7
DB121 2J6 6H8
DB131 2J7, 6H8
DB141 2J8, 6H8
DB151 2J9, 6H9

NOTES

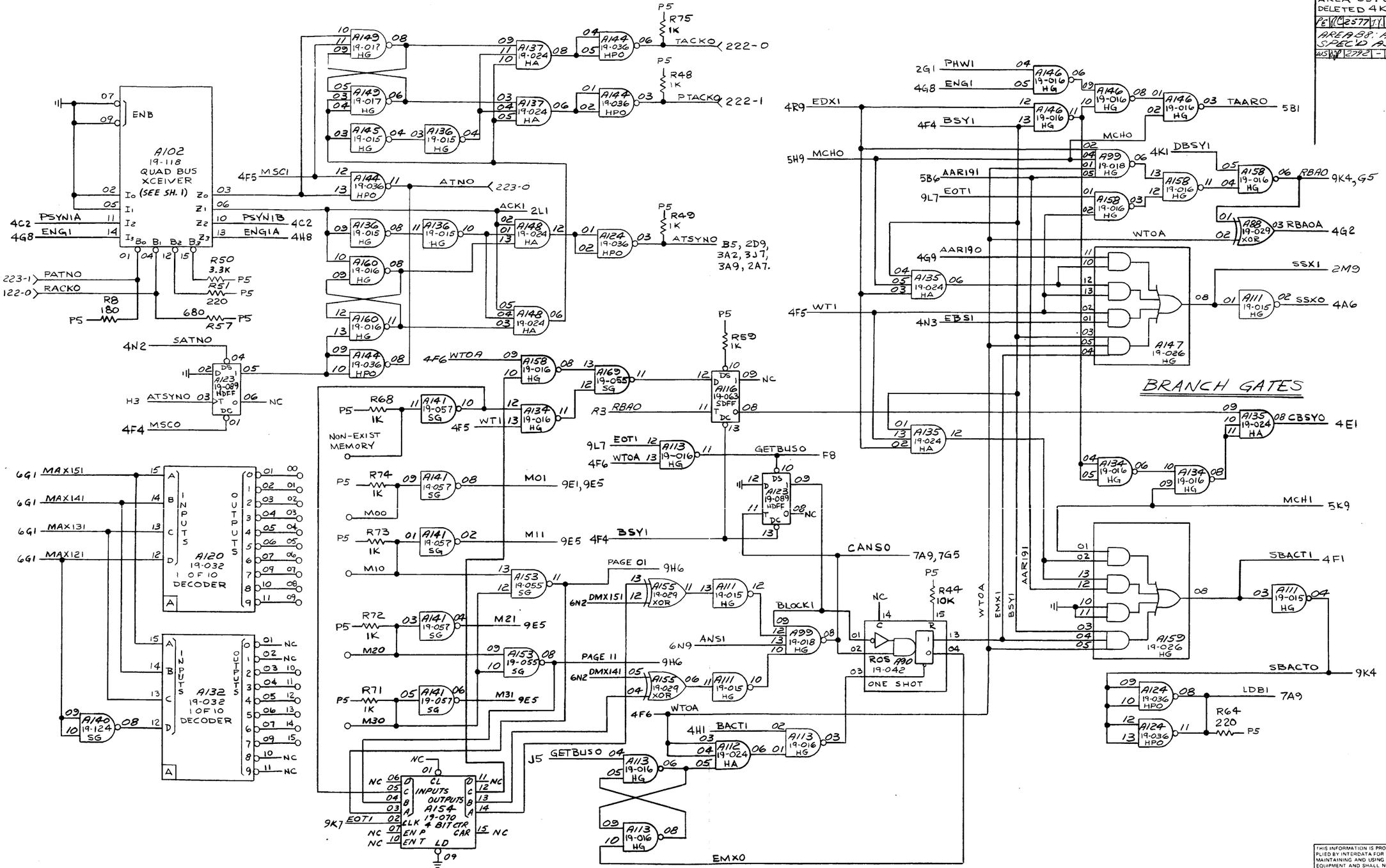
NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE EXTENDED SELECTOR CHANNEL

TASK NO. 03055 DWG NO. 02-328M01 D08 SHEET OF 7

INTERDATA®

REVISIONS			
AREA 55: CBSYO DELETED 4K1 (CROSS REF)			
P6	2577	TY	7-30-75 R01
AREA 88: A140 WAS SPECD AS 19-255			
WSW	2792	-	3-25-76 R02



NOTES

NAME	TITLE	DATE
PEDWARDS	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNTIONAL SCHEMATIC
EXTENDED SELECTOR CHANNEL

TASK NO. 03055 SHEET OF 8 –
DWG NO. 02-328N01R00-08

INTERDATA®

REVISIONS

AREA L7: A84-03 & 08 WAS TO R85 & A167-02. REMOVED R85, R86, R87 & A167. A167-07 WAS DMBZO TO R86 (P5) & R87 (GND).
AREA K3: A92-03 WAS TO E2. A92-06 WAS TO A93-10. ADDED A170.
AREA J6: A142 WAS TO A84-01, 02, 09 & 10. CONNECTED A84-02 to 09 TO MSCO. ADDED NOTE 1.

PC	2577	7-30-75	R01

AREA L3: A92-06 WAS TO A128-02, CO. INJECTED A170-06 TO A128-02. AREA J4 DMBZO WAS REF TO 2D1. AREA H6 A142-05 WAS TO A84-01, 10, A84-02 & 09 WERE REF TO 4F4 (MSCO). AREA L6: A167, A170, A169, R85, R86, R87 & R88 WERE NOT SPEC'D & 84-03 & 08 WERE TO DMBZO (REF TO 2D1)

4	PC 2659	11-19-75	R02

AREA B6: A140 WAS SPEC'D AS 19-055

4	PC 2792	3-25-76	R03

NOTES
1. STRAP OPTION:
E2 TO E3 FOR 7/32
E2 TO E1 FOR 8/32

NAME	TITLE	DATE
P. EDWARDS	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
EXTENDED SELECTOR CHANNEL

TASK NO. 03055 | SHEET 9 OF 9

DWG NO. 02-328M01R03 D08

BRUNING 44-231 16042

RELEASED FOR PRODUCTION
MFG. ENG. [illegible] DATE 1-22-79

REMOVED R85 (NEAR A72 ITEM 49, R86 & R87 (NEAR A16,8) ITEM 49 & 44 RESP. AND A167 ITEM 63. REMOVED STRAPS FROM E1 TO E4 & E5 TO E6. ADDED STRAPS (1) THRU (4) REVISED TO SHOW ROZ COPPER.

A	C	2577	1-30-78	RO1

REROUTED STRAPS #2, ADDED STRAPS 5 & 6, ADDED (3) & (4) STAPES, RELOCATED C-83 & C5 ADDED R90, R91, R92 & R93 ALSO REVISED CIRCUITRY TO REFLECT NEW ARTWORK

A	C	2667	11-17-78	R2

ARTWORK SPEC. DOES NOT ITEM 29, DELETED C76 (ITEM 57), VENDOR 71760

A	F	2792	3-25-76	R3

SEE NOTE 1

60 SEE NOTE 2

APP SIDE

2

1

3

61 TYP. 72 PLACES

B

B

10

2 REF

8

6

VIEW B-B

57 TYP. 76 PLACES C13 THRU C88 ALL UNSPECIFIED

4

5

11 TYP. 10 PLACES

1.38

2.50

3 REF

9

65 REF

.530 MAX

.062 REF.

.125 MAX.

7

PARTIAL VIEW A-A

A

A

NOTES:
1. HEADER STIFFENER (ITEM 3) TO BE SOLDERED TO GND BUS AT 2 ENDS AND CENTER (APP. SIDE).
2. CONTACTS CLOSEST TO EDGE OF BOARD TO BENT INWARD PRIOR TO SOLDERING.

65 ADD TAPE AS SHOWN & WRAP EDGES AROUND STIFFENER

COMPONENT	REF DESIGNATION
INT CKT	A02-A12, A14-A63, A65-A103, A111-A168
CAPACITOR	C1-C75, C77-C88
RESISTOR	R1-R88
STRAPS	7 REQ'D

NAME	TITLE	DATE
E. ROE	DRAFT	5/22/78
R. CERO	CHK	5/24/78
T. YAVIS	ENGR	6/12/78
R. BARKER	Q.C.	6/17/78
D. FRANKENBERGER	MFG. ENG.	6/17/78

TITLE ASSEMBLY EXTENDED IDENTIFIER CHANNEL (ESBLEN)

03162

36-508M01 E03 R03

1 of 1

INTERDATA®

REVISIONS
FOR PREVIOUS REVISION SEE REV R00 VOIDED COPY IN FILE
DSP | XEH | 2040 | [illegible] | 7-18-73 | R01

NOTE: SWITCHES SHOWN ARE IN "OFF" POSITION.

PC2-A04 … PC2-A09 — PCI-12 … PCI-23 — R13 … R24 4.7K — P5 — GB

MCH040 … MCH090 — MCH070 … MCH090

P/O 17-283

RAR150 … RAR040 — 115-3 … 120-3

TO CPU-HI BOARD 35-446

SEE NOTE 3

R27 1K — P5 — 10 — 12 — 11 — 13 — N.C. — N.C.

W/W STAKES — A — B — OPTION SEE NOTE 2

R33 2.2K — C6 .1uF — P5

R32 2.2K — R32 22 — PCI-29 — C5 .1uF

P/O 17-283 PC2 — PC2-ADR MATCH0 — GB

R38 22 — PCI-28 — SNGL0 — GB

NOTE: SWITCHES ARE IN OFF POSITION

P/O 17-283 — P/O 17-283 PC2 — PC2-ADR SYN0 — TP

R29 1K — P5 — R36 22 — PCI-30

SCLR0C — 102-3

FTIT0 — 103-3

TO CPU-HI BOARD 35-446

R28 1K — P5

BCLK0 — 104-3

N.C.

FSADV1

FADV0

P/O 17-283 PC2 — ADV0 — ADV1 — PCI-26 — PCI-27 — R34 22 — R35 22 — R30 2.2K — R31 2.2K — C3 .1uF — C4 .1uF — ADVC0

P/O 17-283

C7 THRU C15 .1uF, 30V — P5

DECOUPLING CAPACITORS

P/O 17-283 — PCI-24 — PCI-25 — C2 2.2uF — C1 2.2uF — P5

106-3 — 101-3 — 105-3 — 100-3 — 112-3

TO CPU-HI BOARD 35-446

ALL DIODES 33-027

LED15 … LED04

R1 … R6 330 — PCI-00 … PCI-05

R7 … R12 330 — PCI-06 … PCI-11

R26 4.7K — R25 4.7K — P5

NOTES

1. UNLESS OTHERWISE SPECIFIED ALL APPARATUS IS LOCATED ON TEST CONTROL BOARD 35-503.
2. REFER TO 02-276 TEST AID INFO SPEC.
3. THIS FLIP FLOP-COULD BE USED AS A TEST AID.

NAME	TITLE	DATE
V. PERRI	DRAFT	7-17-73
E CERO	CHK	7-18-73
G. JOYCE	ENGR	12-19-72
H. ROSS	Q.C.	12-19-72
D. FRANKENBERGER	DIR ENG	1-3-73

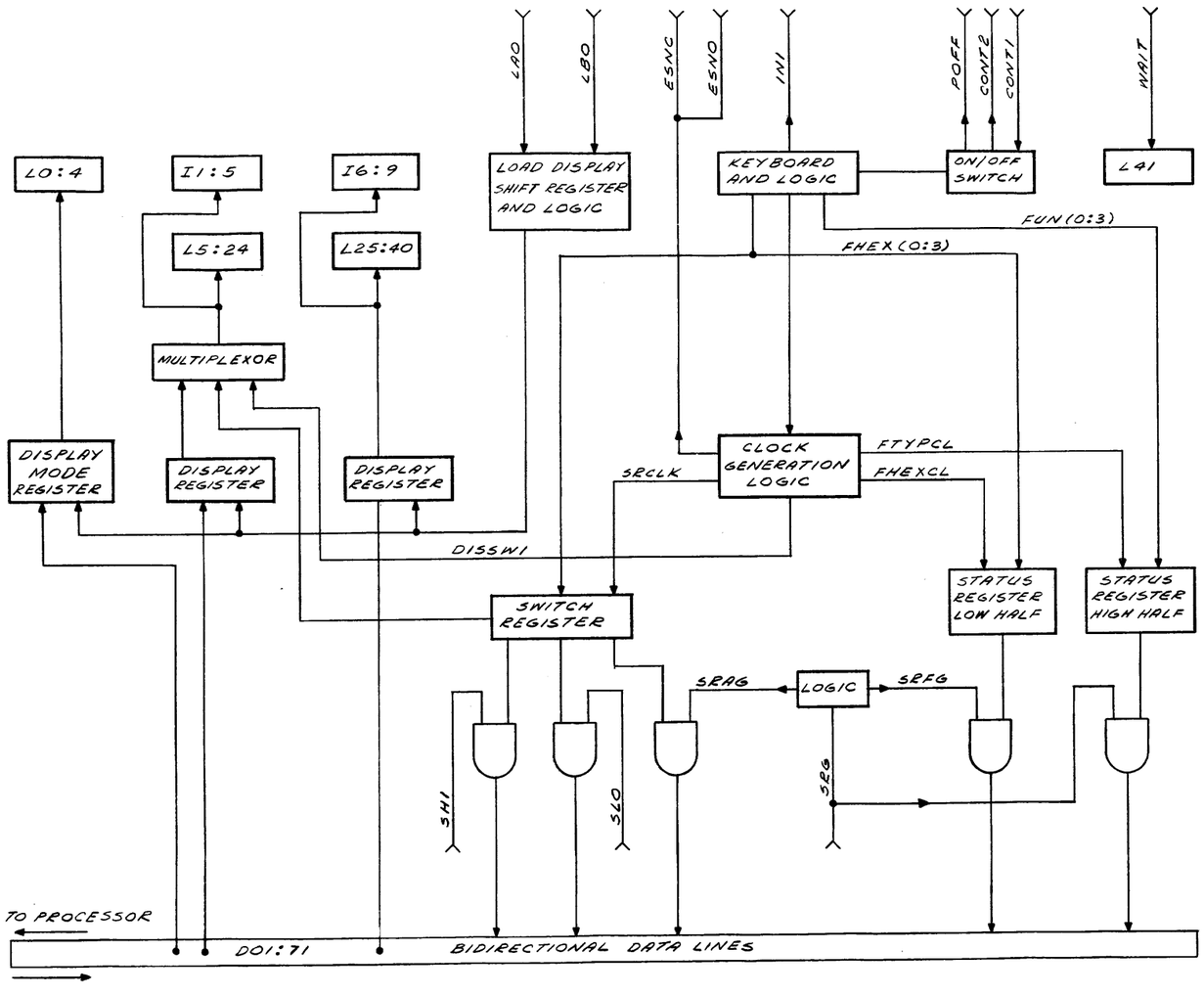
TITLE FUNCTIONAL SCHEMATIC — TEST AID

TASK NO. 03047 — DWG NO 02-276 R01D08 — SHEET OF 1 - 1

BRUNING 44-231 16042

INTERDATA®

REVISIONS				
RELEASED FOR PRODUCTION MFG. ENG. [illegible] DATE 2/14/74				
REVISED SHTS 2 & 3				
W WEA	2323	-	1-31-75	R01
REVISED SHTS 2 & 3				
WS	F	2635	-	12-10-75	R02



BLOCK DIAGRAM

CONN-3		
TERM	ROW 1	ROW 2
00	GND	SHIO
01	INITO	GND
02	WAITI	D41
03	ESNCO	LAO
04	ESNOO	D51
05	POFFO	D61
06	SSGLI	SLOO
07	SCLRO	
08	GND	D71
09	D01	
10	D11	
11	D21	
12	D31	GND
13	SRGO	CONT3
14	LBO	

REVISION LEVEL OF THIS SHEET IS CONSIDERED THE REVISION LEVEL OF THE DOCUMENT

SHEET INDEX				
SHEET	REV	2	2	0
INDEX	SHT	2	3	4

NOTES

NAME	TITLE	DATE
N. MATTER	DRAFT	1-28-74
N. MATTER	CHK	1-28-74
S. MESSINA	ENGR	1-31-74
L. JOHMANN	TEST	1-31-74
	DIR ENG	

TITLE: FUNCTIONAL SCHEMATIC HEXADECIMAL DISPLAY

TASK NO. 03081
DWG NO. 09-065 R02 D08
SHEET 1 OF 4

BRUNING 44-231 16042

INTERDATA®

REVISIONS				
AREA L1: CONNECTIONS 21, 22, 23 WERE DIRECTY CONNECTED TO 1W, 5W, & 9W RESP, CROSS REF ALL CONN 3 PIN NOS. TO SHEET 3. AREA G8: C7 WAS 4.7uF. C8 WAS 15uF				
P/C	WR# 2323	/	1-31-75	R01
AREA K1: ADDED JUMPER BETWEEN POINTS 03 & 05 AREA L6-L8, A61 02 & 04 WERE TO A61 10 & 13				
WS	# 2635	/	12-10-75	R02

SH0 SH1 SH2 SH3 SDA INIT
R47 220
R55 220
A29 19-015 HG
INITO 3A3
SDAO 4A2
R51 220
SH4 SH5 SH6 SH7 SRG
SH8 SH9 SHA SHB SFL
SHC SHD SHE SHF SFN
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25 D26 D27 D28 D29 D30 D31 D32 D33 D34 D35 D36 D37 D38 D39 D40 D41 D42
ALL DIODES 23-001
R54 220
R45 R46 R44 R49 220 (TYP)
SAD SRD SWR SRN SSL
R48 R36 R50 R35 220 (TYP)
R53 220
SSGLI 3A2
SSLI 3F1
R52 220
SSLO 3D1
SRNO
SORI 3F1
SORO 3E1
FKEYI
C7 2.2uF
C8 15uF NOT EQUIPPED
R84 10K P5
C9 100 PF 500 nS
R85 10K P5
A60 19-042 ONE SHOT
STRB1
HKEYI
XRPI
R82 1K P5
A48 19-018 HG
A59 19-016 HG
A37 19-025 HA
FUN10 FUN20 FUN00 FUN30
HEX31 HEX21 HEX11 HEX01
3H1, 4A1 3J, 4A2 3H1, 4A1 3G, 4A1
3D1 3D1 3D1 3E1

1W R86 22Ω 2W LP5
POFFO 3B3
CONT2 3B2
R83 1K P5
OFF ON LOCK CONT1 3A2
FROO1 3B3
SRGI 3G3
SRGO 3A3
SRFG1 3G3
SRAG1 4M3
SHIO 3A4
SHI1 4G3
SLOO 3A4
SLO1 4B3
A36 19-115 HA
A38 19-015 HG

XRPI 4N4, 3A5
A58 19-030
INPUT A B C D
OUTPUT A B C D
SHR SHL SER IN MODE CONT 4BIT SHIFT R.
LDB1 3F5
LDC1 4B5
LDD1 4L5
LDE1 4N4, 3L4
A47 19-115 HA
LAI 3A5
LAO 3A4
LBO 3A4
R67 330
R77 470
R66 330
R76 470
LAOA 3M4
A29 19-015 HG
A38 19-015 HG

WAIT1 3A3
A7 19-109 HG0
L41 L42 L0
R42 150
R43 150
R1 150 LP5
A39 19-015 HG
A50 19-016 HG
DISSW1 4R7
A61 19-089
SRENB1
SRENB0
SRCLK0 4A2
A49 19-017 HG
ESNC0 3A3
ESNO0 3A3
FTYPCLO 3E2
FHEXCLO 3J2
A59 19-016 HG

NOTES
1. L0 THRU L42 ARE 33-027

NAME	TITLE	DATE	TITLE FUNCTIONAL SCHEMATIC
P. EDWARDS	DRAFT	12-5-73	HEXADECIMAL DISPLAY
	CHK		
	ENGR		
	DIR ENG		TASK NO. 03081 SHEET OF 2-4 DWG NO. 09-065R02 D08

BRUNING 44-231 16042

INTERDATA®

REVISIONS				
AREA A1-A4, B1-B4: ADDED CROSS REF. FROM SHT. 2.				
PE	VAH	2323	—	1-31-75	R01
AREA B2, ADDED SCLRO REF. FROM SHT. 2				
WS	JK	2635	—	12-11-75	R02

DB1-C3 CONT3
213-3 TP
214-3 TP
DB1-C2 23 CONT2 2J1
DB1-C1 CONT1 2L2
106-3 14 SSGL1 2J6
107-3 9 SCLRO J1,2J6
105-3 22 POFFO 2J1
101-3 12 INITO 2H1
103-3 15 ESNCO 2S7
104-3 16 ESNOO 2S7
113-3 17 SRGO 2L2
102-3 10 WAITI 2M5
2063 18 SLOO 2L3
2003 20 SHIO 2L3
114-3 19 LBO 2L5
203-3 13 LAO 2K5
208-3 D71
205-3 D61
204-3 D51
202-3 D41
112-3 D31
111-3 D21
110-3 D11
109-3 D01
2L3 XRPI
2L4 LAI

FUN00 2D9
FUN10 2C9
SSLO 2G7
FUN20 2C9
SORO 2K7
FUN30 2D9
FTYPCLO 2N7
SCLRO J1
SORI 2J7
SSLI 2G7

A57 19-043 HGO
A46 19-071
R81 1K P5
R80 1K P5
2M2 FROO1
2M2 FROOO
2M2 SRG1

HEX01 2B9
HEX11 2B9
HEX21 2A9
HEX31 2A9
FHEXCLO 2N8
SCLRO B2
R78 1K P5 E1
A56 19-071
2R2 SRFG1
A45 19-036 HPO
A35 19-036 HPO

A1 19-071
A8 19-109 HGO
L1 L2 L3 L4
R2 R3 R4 R7 150
LP5
LAOA 2N5
LDE1 2R4

R64 R63 R65 R62 R61 R60 R59 R58 330 (TYP.) P5
R68 R69 R70 R71 R72 R73 R74 R75 330 (TYP.)
R79 1K P5
2R4 LDBI

A26 4 BIT SHIFT REG. 19-030
A25 19-030 4 BIT SHIFT REG.
A24 19-030 4 BIT SHIFT REG.
A23 19-030 4 BIT SHIFT REG
A7 A6 A5 19-109 HGO
L40 L39 L38 L37 L36 L35 L34 L33 L32 L31 L30 L29 L28 L27 L26 L25
R38 R39 R41 R40 R34 R35 R37 R36 R30 R31 R33 R32 R26 R27 R29 R28 150
LP5 4A8

A17 33-029 HEX DISPLAY
A16 33-029 HEX DISPLAY
A15 33-029 HEX DISPLAY
A14 33-029 HEX DISPLAY

LP5 — L GND
33MF, 10V
C1 & C2

P5 — GND
33MF, 10V
C3 TO C6

P5 — L GND
0.1MF, 30V
C10 TO C14

P5 — GND
0.1MF, 30V
C15 TO C39

DECOUPLING CAPACITORS

NOTES

NAME	TITLE	DATE	TITLE FUNTIONAL SCHEMATIC
P. EDWARDS	DRAFT	12-3-73	HEXADECIMAL DISPLAY
	CHK		
	ENGR		
	DIR ENG		TASK NO. 03081
			DWG NO. 09-065R02 D08
			SHEET OF 3-4

BRUNING 44-231 16042

INTERDATA®

REVISIONS

2B9 HEX01 · 2B9 HEX11 · 2A9 HEX21 · 2A9 HEX31 · 2M7 SRCLK0 · 2H2 SDA0 · 2N3 SL01 · 2N2 SHI1 · 2R2 SRAS1 · 3R4 D71 · 3R4 D61 · 3R5 D51 · 3R5 D41 · 3R5 D31 · 3R5 D21 · 3R5 D11 · 3R5 D01 · 2R4 LDC1 · LDD1 2R4 · LDE1 2R3 · XRP1 2L3 · 3L8 LP5 · DISSWI 2N6

SW161 SW171 SW181 SW191 SW121 SW131 SW141 SW151 SW081 SW091 SW101 SW111 SW041 SW051 SW061 SW071 SW001 SW011 SW021 SW031

A55 A54 A53 A52 A51 19-071 D FLIP-FLOP

A44 A43 A42 A41 A40 19-036 HPO / HGO

A34 A33 A32 A31 A30 19-030 4 BIT SHIFT REG (D C B A SHR SHL SER IN MODE CONT)

A22 A21 A20 A19 A18 19-053 2:1 MUX. (ENB SEL)

A5 A4 A4 A4 A4 A4 A3 A3 A3 A3 A3 A3 A3 A3 A2 A2 A2 A2 A2 A8 19-109 HGO

L24 L23 L22 L21 L20 L19 L18 L17 L16 L15 L14 L13 L12 L11 L10 L9 L8 L7 L6 L5

R23 R24 R25 R22 R19 R18 R20 R21 R16 R15 R14 R17 R12 R11 R10 R13 R8 R9 R6 R5 150

A13 A12 A11 A10 A9 33-029 HEX DISPLAY (A B C D LP5)

NOTES

NAME	TITLE	DATE
P.EDWARDS	DRAFT	12-3-73
	CHK	
	ENGR	
	DIR ENG	

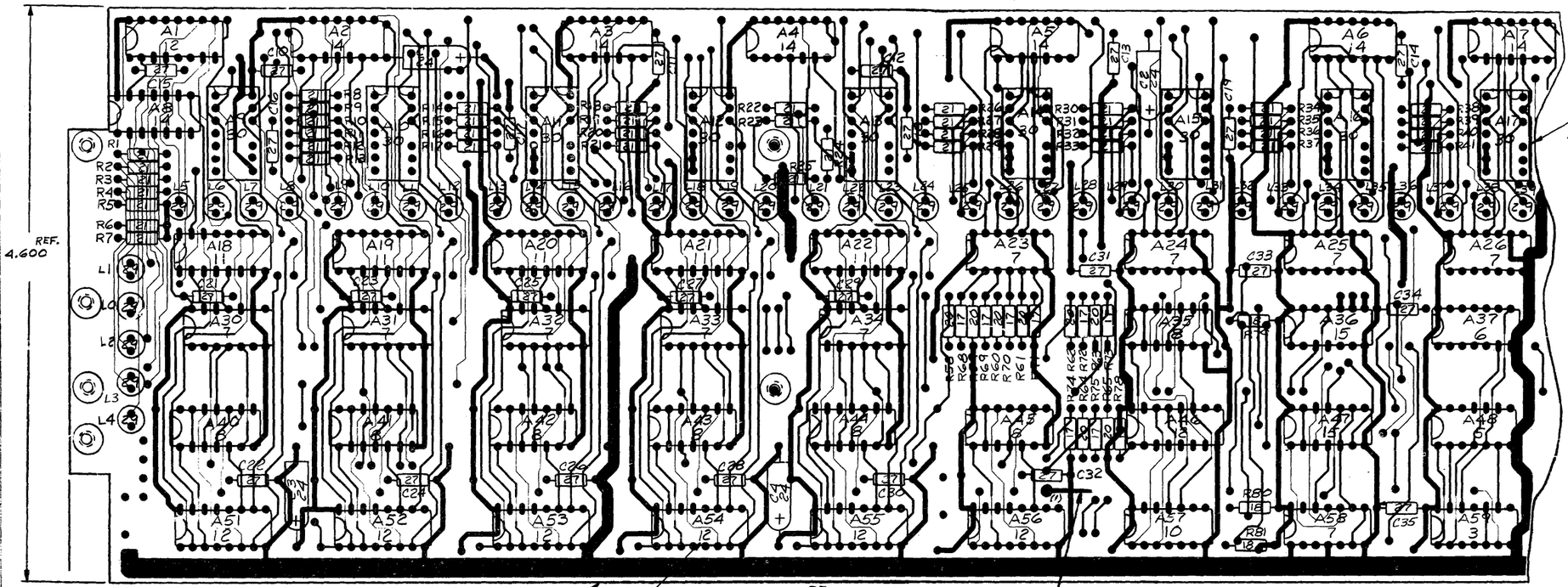
TITLE FUNCTIONAL SCHEMATIC HEXADECIMAL DISPLAY

TASK NO. 03081 · DWG NO. 09-065 D08 · SHEET 4 OF 4

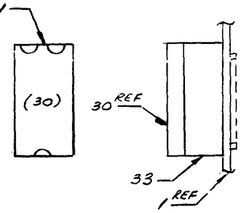
BRUNING 44-231 16042

INTERDATA

RELEASED FOR PRODUCTION			
MFG. ENG. JMB	DATE 3-20-74		
REVISED TO REFLECT F02 COPPER			
PC	VM	2152	V 15-74	R01
CHANGED: ORIENTATION NOTE FOR LED'S DID NOT SHOW FLAT SIDE			
JM	VM	2074	VM	5-28-74	R02
REVISED R86, WAS IN HORIZONTAL POSITION AREA K8.			
JM	VM	2261	-	9-5-74	R03
REVISED CIRCUITRY TO REFLECT NEW COPPER, STRAP #1 WAS NOT SPEC'D (AREAS H4, L9)			
WS	T	2635	-	12-11-75	R04



DISPLAY TO BE INSERTED IN SOCKET WITH NOTCHES AS SHOWN



DETAIL A
FOR USE ON F02 ONLY

COLORED DOT OR FLAT SIDE OF LED INDICATES CATHODE END. (TYPICAL)

BASE OF LEDS MUST BE PARALLEL TO P.C. BOARD TO ACHIEVE PERPENDICULARITY BEFORE & DURING FLOW SOLDER.

SLEEVING (THIS END)

F02	AS SHOWN
F01	LESS ITEMS 30 & 33
VARIATION INFORMATION	

NOTES:
1. UNSPECIFIED COMPONENTS ARE ITEM 28.

NAME	TITLE	DATE
P.EDWARDS	DRAFT	1-16-74
H.MATTER	CHK	1-16-74
S.MESSINA	ENGR	2-15-74
S.MESSINA	MGR.	2-15-74

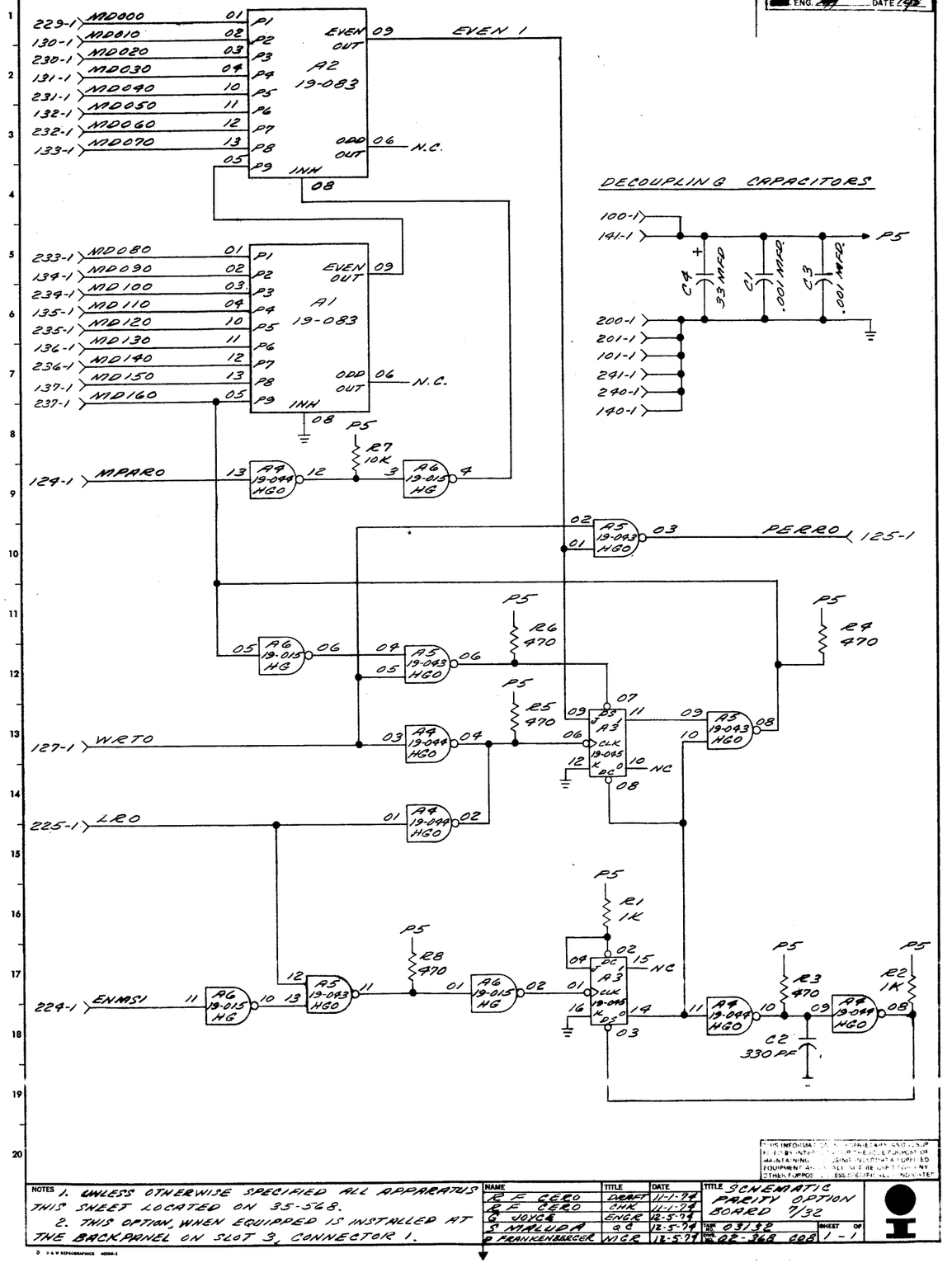
TITLE ASS'Y PRT. CKT. HEXIDECIMAL DISPLAY

DWG NO. 03081 REV. 04

SIZE B

INTERDATA

RELEASED FOR PRODUCTION
ENG. DATE



NOTES
1. UNLESS OTHERWISE SPECIFIED ALL APPARATUS THIS SHEET LOCATED ON 35-568.
2. THIS OPTION, WHEN EQUIPPED IS INSTALLED AT THE BACKPANEL ON SLOT 3, CONNECTOR 1.

NAME	TITLE	DATE
R F CERO	DRAFT	11-1-74
G F CERO	CHK	11-1-74
G JOYCE	ENGR	12-5-74
S MALUDA	QC	12-5-74
D FRANKENBERGER	MGR	12-5-74

TITLE SCHEMATIC PARITY OPTION BOARD 7/32
DWG NO. 03132 SHEET OF
PART NO. 02-368 C08 1 - 1

NOTES:
1. STIFFENER BAR (ITEM 3) SHALL BE SOLDERED TO GND BUS AT 2 END POINTS AND CENTER POINT.
2. CONNECTOR PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.

15.380 REF

14.880 REF

SEE NOTE 1

62 SEE NOTE 2

REVISIONS			
RELEASED FOR PRODUCTION			
MFG ENG. [illegible] DATE [illegible]			
REVISED COPPER TO REFLECT 25-473 R02, A93 ITEM WAS 11			
[illegible]	2484	- 9/14/73	R01
ADDED CONN FROM A74 PIN 2 TO GND			
[illegible]	2525	- 9-27-73	R02
REVISED COPPER TO REFLECT 25-473 R05. ADDED R78 (ITEM 42.)			
[illegible]	2540	- 11-6-73	R03
REVISED TO REFLECT R04 COPPER.			
[illegible]	2551	- 12-8-73	R04
REVISED TO REFLECT R07 COPPER STRAP #1 AND ADT SPEC 10.			
[illegible]	2580	- 1-29-75	R07

10
2 REF.
8
6

6 MOUNT ON SOLDER SIDE 2 PLACES

64

5 2 PLACES

4 2 PLACES

1

3 SEE NOTE 1

A A

3
9
.530 MAX
.062 REF.
.125 MAX.
7

PARTIAL VIEW A-A

63 32 PLACES

66

62 SEE NOTE 2

COMPONENT	REF DESIGNATION
CAPACITOR	C1 THRU C70
RESISTOR	R1, R2, R6, THRU R10
	R27 THRU R29, R33, R36
	E37 THRU E93
	R52, R53, R60, R61
	R63 THRU R78
I.C.	A2 THRU A10, A14 THRU A20
	A23 THRU A26, A31 THRU A39, A77 THRU A80
	A87, A88, A97, R93 A90, A93 THRU A96
	A101 THRU A106, A108 THRU A115, A132, A138,
	A140, A141, A142 AND THRU A149, A151 AND A154

NAME:	TITLE	DATE
W. FREIDEL	DRAFT	7-30-75
E. CLARO	CHK.	7-16-75
R. BACKUS	ENG.	
R.H. BACKER	A.C.	
D. FRANKENBERGER	M&P.	

TITLE: PART. ASSY. ASSY. DIRECT MEMORY ACCESS CONTROL BOARD

03142
35-328 M01/R03

1 OF 1

C-01

NOTES:

1. STIFFENER BAR (ITEM 3) SHALL BE SOLDERED TO GND BUS AT 2 END POINTS AND CENTER POINT.
2. CONNECTOR PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.

15.380 REF

14.880 REF

26-423 REV

MEMORY ACCESS CONTROL BOARD

SEE NOTE 1

62 SEE NOTE 2

63 32 PLACES

66

64

60 MOUNT ON SOLDER SIDE 2 PLACES

5 2 PLACES

4 2 PLACES

1

3 SEE NOTE 1

A

A

10

2 REF.

8

6

3

9

.530 MAX

.062 REF.

.125 MAX.

7

PARTIAL VIEW A-A

REVISIONS

	ECO	PROJECT NO.	
MFG ENG.		DATE	
REVISED COPPER TO REFLECT 25-473 ROB, A93 ITEM WAS 11			
2384	—	11/14/74	ROI
ADDED CONN. FROM A74 PIN 2 TO GND			
2505	—	9/27/74	ROF
REVISED COPPER TO REFLECT 25-473 ROB. ADDED 378 (ITEM 48.)			
2540	—	11/27/1802	
REVISED TO REFLECT ROI COPPER.			
3283	—	12-8-75	ROH
REVISED TO REFLECT ROJ COPPER. STAKE # 51 WAS NOT STAKED.			
3280	—	12-26-75	ROJ
REVISED CIRCUITRY TO REFLECT ROJ COPPER. ADDED A79 (ITEM 49.) C C71 (ITEM 50.) NEAR A74 PIN 2.			
3063	—	11-25-76	

COMPONENT	REF DESIGNATION
CAPACITOR	C1 THRU C71
RESISTOR	R1, R2, R6 THRU R10
	R12, R14 THRU R22
	R27 THRU R29, R31 THRU R36
	R31, R32, R43
	R52, R53, R60, R61
	R63 THRU R79
	R80 THRU R90, R94 THRU R100
I.C.	R2 THRU R4, R6 THRU R14, R17 THRU R20
	R82, R85, R87, R89, R90, R93 THROUGH
	R61 THRU R72, R95 THRU R105, R107 THROUGH
	R140, R141, R142 AND R143 AND R27 AND R28

	NAME:	TITLE	DATE
DRAWN	V. PEPPI	DRFT	7-30-75
CHKD	A. CORO	ENG	8-12-75
APPD	J. BACKUS	ENG	
	R. H. BARKER	M.E.	
	D. FRANKENBERGER	MGR.	

TITLE: REF. CKT. ASSY DIRECT MEMORY ACCESS CONTROL BOARD

03142

35-328 MOTHER 203

1 OF 1